General Description

The LTP3559 is a high voltage, low power consumption and high performance LDO. The family uses an advanced CMOS process and a P-MOSFET pass device to achieve fast start-up, with high output voltage accuracy. The LTP3559 is stable with a 1.0μF~10μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations.

Features

- Wide Input Voltage Range : up to 45V
- Output Current : 350mA
- Standard Fixed Output Voltage Options : 1.8V, 2.5V, 3.0V, 3.3V, 3.6V, and 5.0V
- More Output Voltage Options Available on Request
- Low IQ : 2.5μA Typically
- Low Dropout Voltage
- Short current protection:150mA
- Excellent Load and Line Transient Response
- Line Regulation : 0.01%/V Typically
- Normal Version Available in SOT23-3L, SOT23-5L and SOT89 Packages
- Shutdown Version Available in SOT23-5L and Tiny DFN1×1-4L Packages

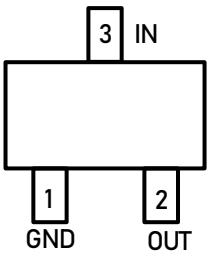
Order Information

Model	Package	Ordering Number Note1	Packing Option
LTP3559	SOT23-3L	LTP3559-xxXT3	Tape and Reel, 3000
	SOT23-5L	LTP3559-xxNXT5	Tape and Reel, 3000
	SOT23-5L	LTP3559-xxXT5	Tape and Reel, 3000
	SOT89-3	LTP3559-xxXT4	Tape and Reel, 1000
	SOT89-3R	LTP3559-xxRXT4	Tape and Reel, 1000
	DFN1×1-4L	LTP3559-xxNXF4	Tape and Reel, 10000

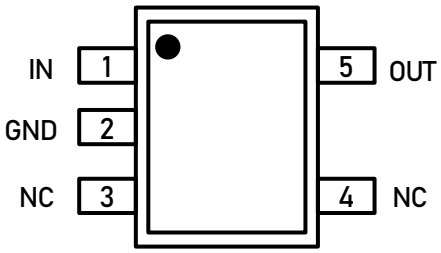
Note1: xx stands for output voltage, e.g. if xx = 18, the output voltage is 1.8V; if xx = 30, the output voltage is 3.0V. The device with suffix "N" is shutdown version with enable control input.

Pin Description

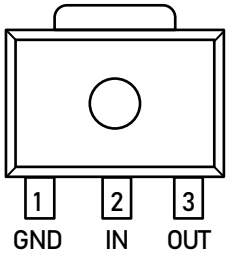
Normal Version Without Enable (Top View)



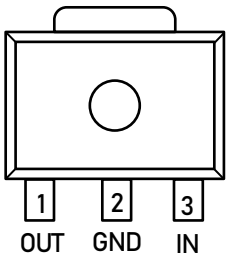
SOT23-3L



SOT23-5L

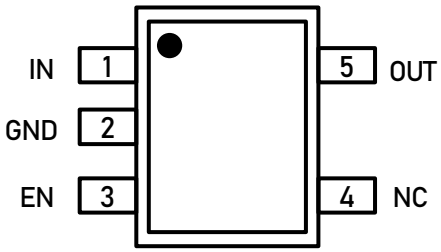


SOT89-3

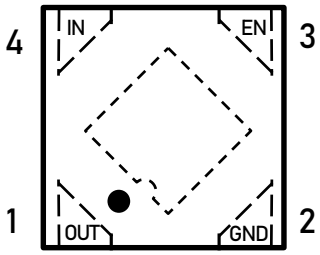


SOT89-3R

Shuntdown Version With Enable (Top View)



SOT23-5L

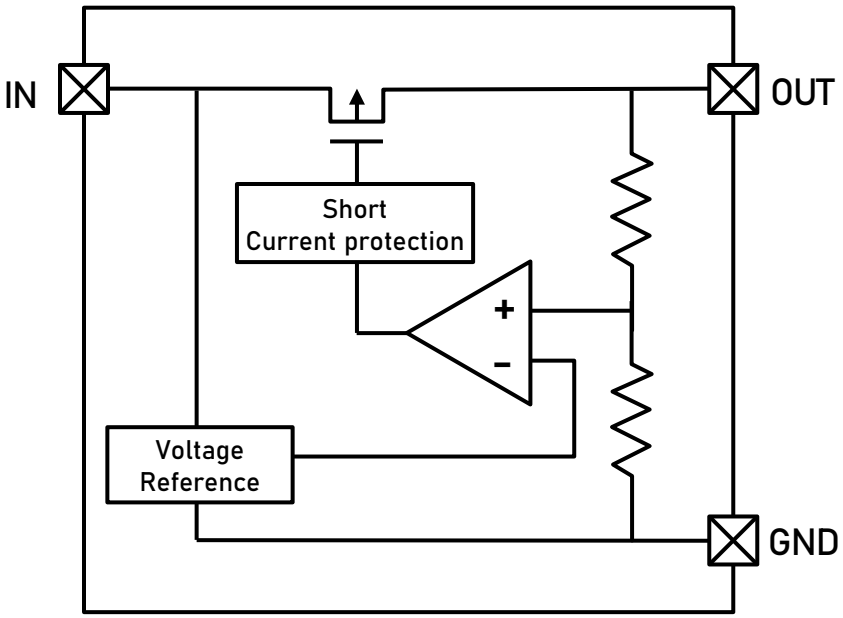


DFN1×1-4L

Pin Function

Pin No.						Pin Name	Pin Function
SOT23-3L	SOT23-5L	SOT89-3	SOT89-3R	SOT23-5L	DFN1×1-4L		
LTP3559-xxXT3	LTP3559-xxXT5	LTP3559-xxXT4	LTP3559-xxRXT4	LTP3559-xxNXT5	LTP3559-xxNXF4		
1	2	1	2	2	2	GND	Ground.
2	1	2	3	1	4	IN	Supply input pin.
3	5	3	1	5	1	OUT	Output pin.
				3	3	EN	Enable control input, active high.
	3 , 4			4		NC	No connection.

Block Diagram



Functional Description

Input Capacitor

A 1µF-10µF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1µF to 10µF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Low Quiescent Current

The LTP3559, consuming only around 2.5µA for all input range and output loading, provides great power saving in portable and low power applications.

Short Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the short current limit protection will be triggered and clamp the output current to approximately 100mA to prevent over-current and to protect the regulator from damage due to overheating.

Absolute Maximum Ratings

Parameter	Rating		Unit
IN pin to GND pin	−0.3 to 48		V
OUT pin to GND pin	−0.3 to 6		V
Thermal Resistance (Junction to Ambient)	SOT-89	135	℃/W
	SOT23-5L	250	
	SOT23-3L	360	
	DFN1×1-4L	250	
Operating Junction Temperature	−40 to 125		℃
Storage Temperature	−65 to 150		℃
Lead Temperature (Soldering, 10 sec)	300		℃
ESD (HBM mode)	ESDA/JEDEC JS-001-2017		±2000V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Electrical Characteristics

(V_{IN} = V_{OUT} + 2V; I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1.0µF, unless otherwise noted. Typical values are at T_A = +25°C.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage				45	V
$Line_{REG}$	Line Regulation	2.5V ≤ VIN ≤36V, I_{OUT} = 10mA		0.01	0.04	%/V
V_{DROP}	Dropout Voltage	V_{OUT}= 3.0V, I_{OUT} = 100mA		330		mV
		V_{OUT}= 3.0V, I_{OUT} = 200mA		690		
$Load_{REG}$	Load Regulation	1mA ≤ I_{OUT} ≤ 300mA, V_{IN} =V_{OUT}+2V			40	mV
I_{OUT}	Maximum Output Current	V_{IN} = V_{OUT} +1V	350			mA
I_Q	Quiescent Current	I_{OUT} = 0mA		2.5	4	µA
I_{Q_OFF}	Standby Current	V_{EN} = 0V, TA = 25°C		0.1	1	µA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”			0.4	V
I_{EN}	EN Pin Current	V_{EN}=0-36V		1		µA
PSRR	Power Supply Rejection Ratio V_{IN} = V_{OUT}+1V I_{OUT} = 20mA	f = 1 kHz		60		dB
e_N	Output Noise Voltage	V_{IN} = V_{OUT}+2V, I_{OUT} = 1mA, f = 10Hz to 100KHz, (V_{OUT} =3V) C_{OUT} = 1µF		100		µVrms
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_A=+25°C		155		℃
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling From TSD		20		℃

TYPICAL PERFORMANCE CHARACTERISTICS

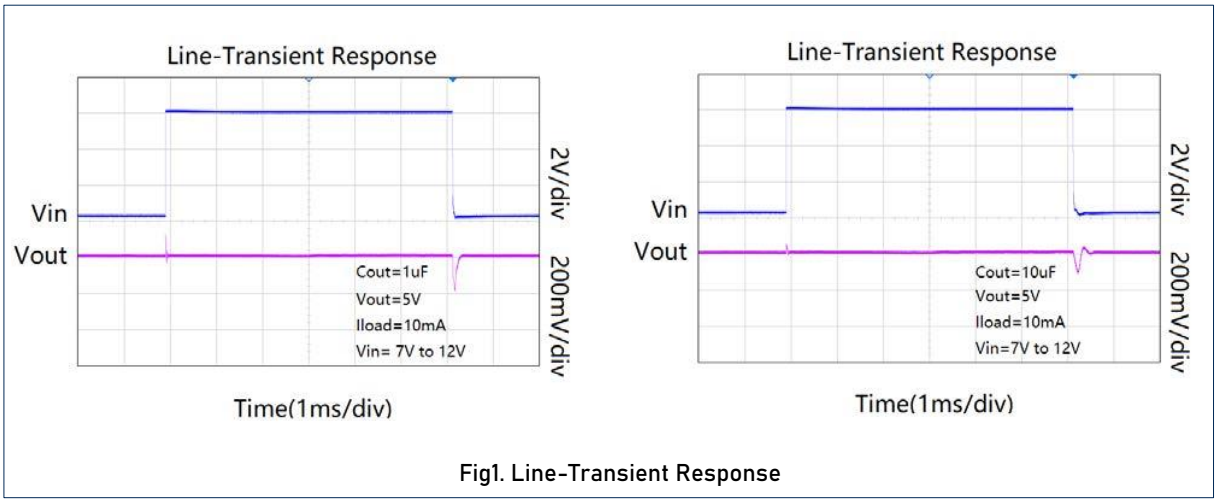


Fig1. Line-Transient Response

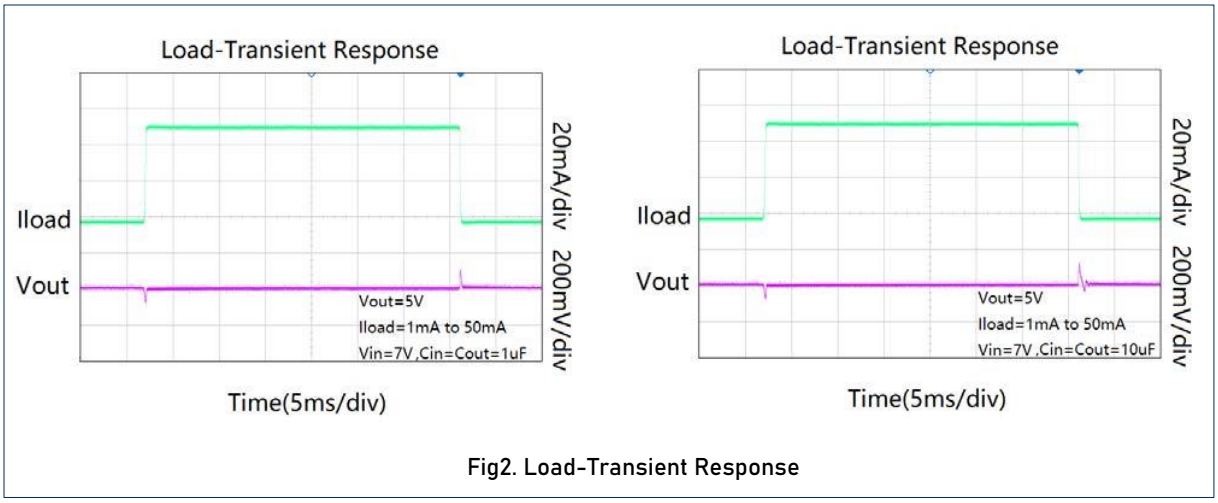


Fig2. Load-Transient Response

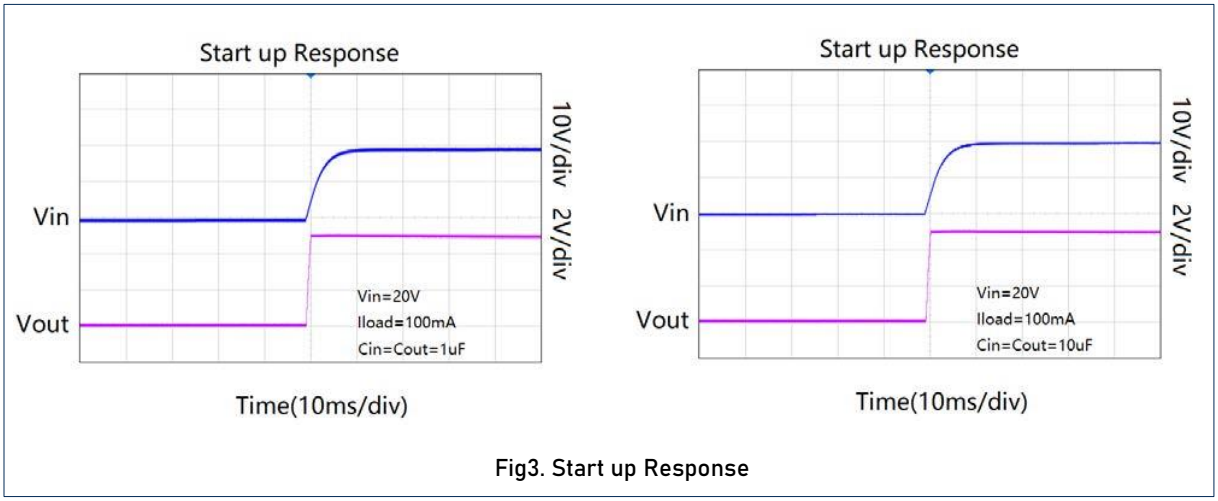


Fig3. Start up Response

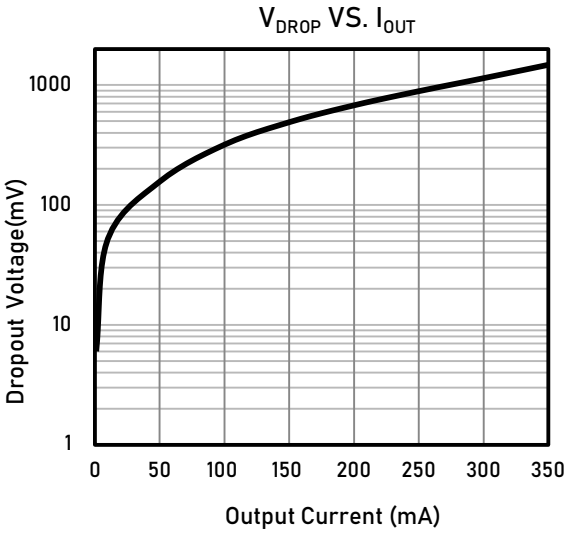


Fig4. Dropout Voltage VS Output Current

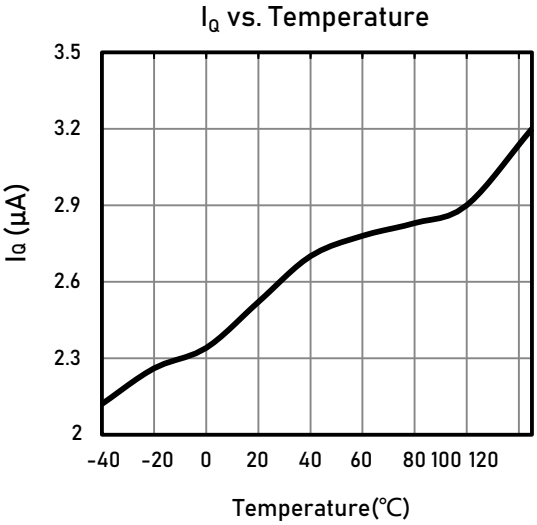
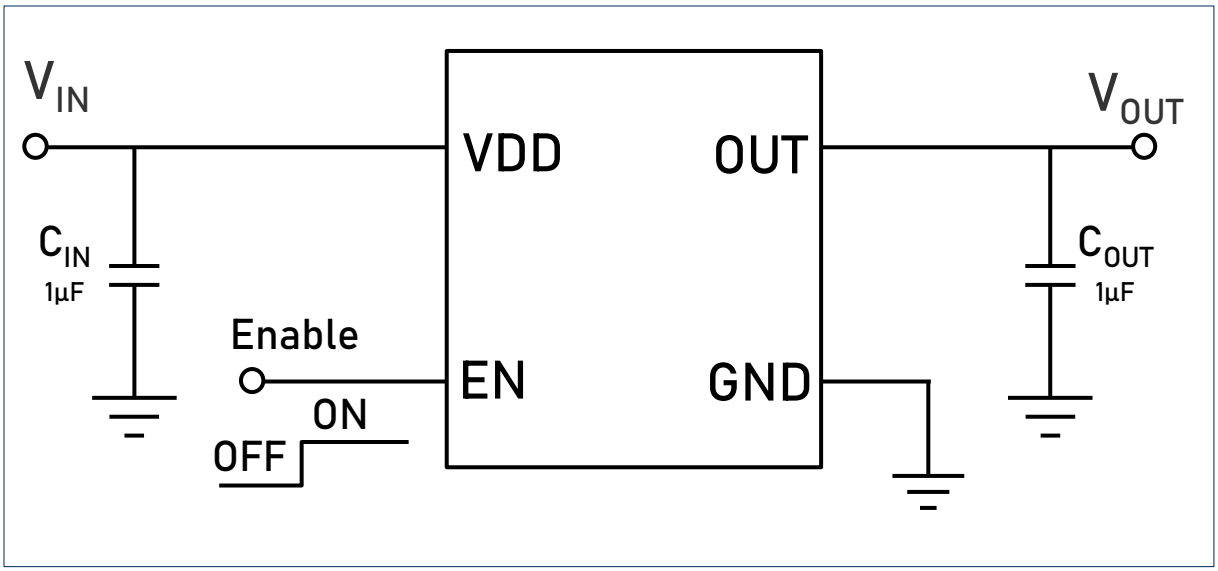


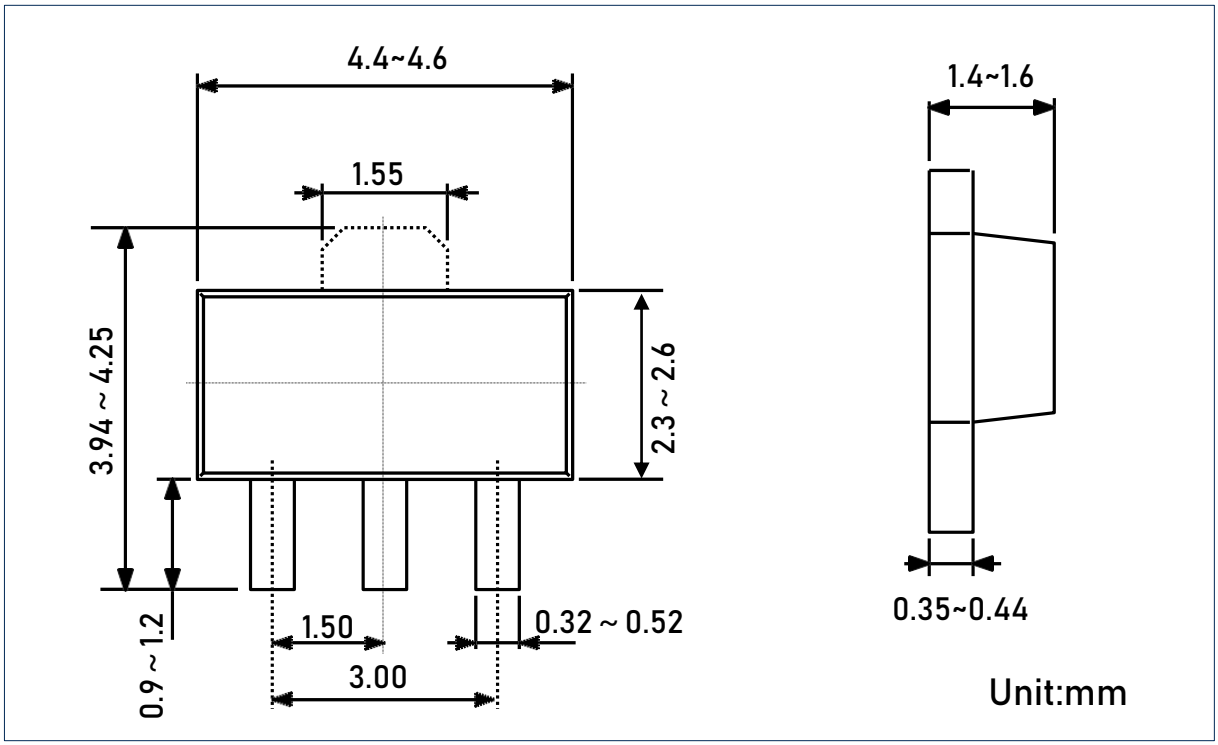
Fig5. I_Q VS Temperature

Application Circuits

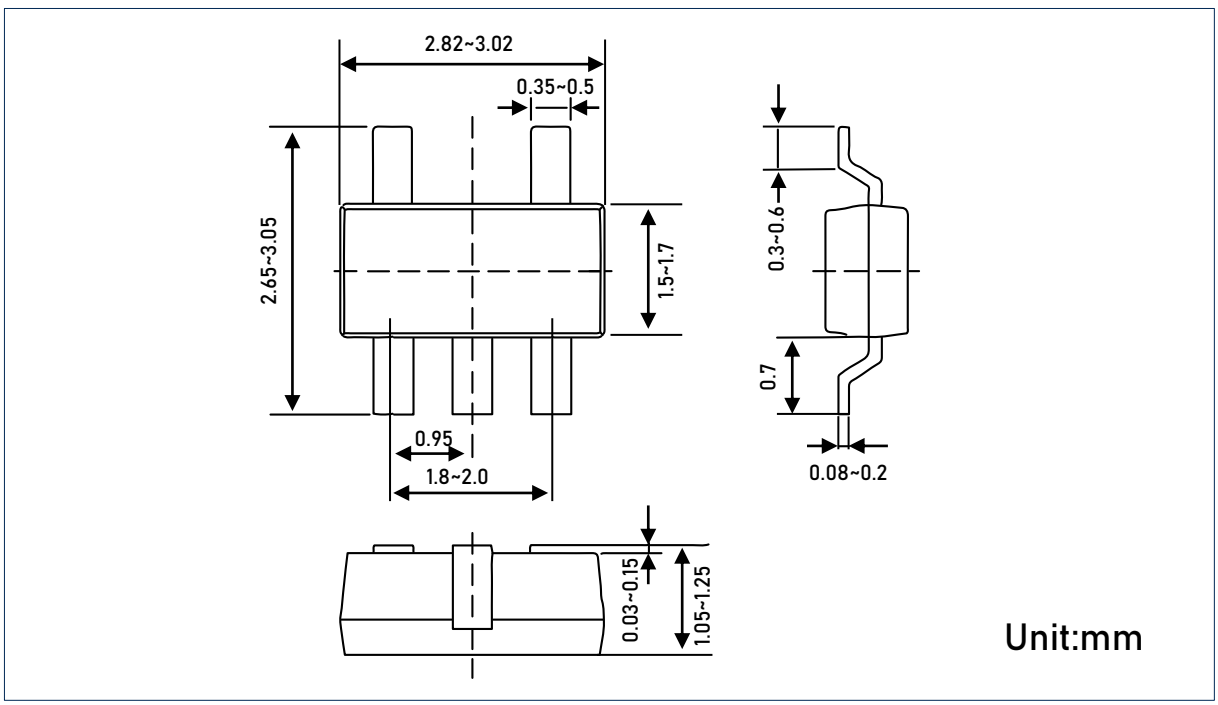


Package Dimension

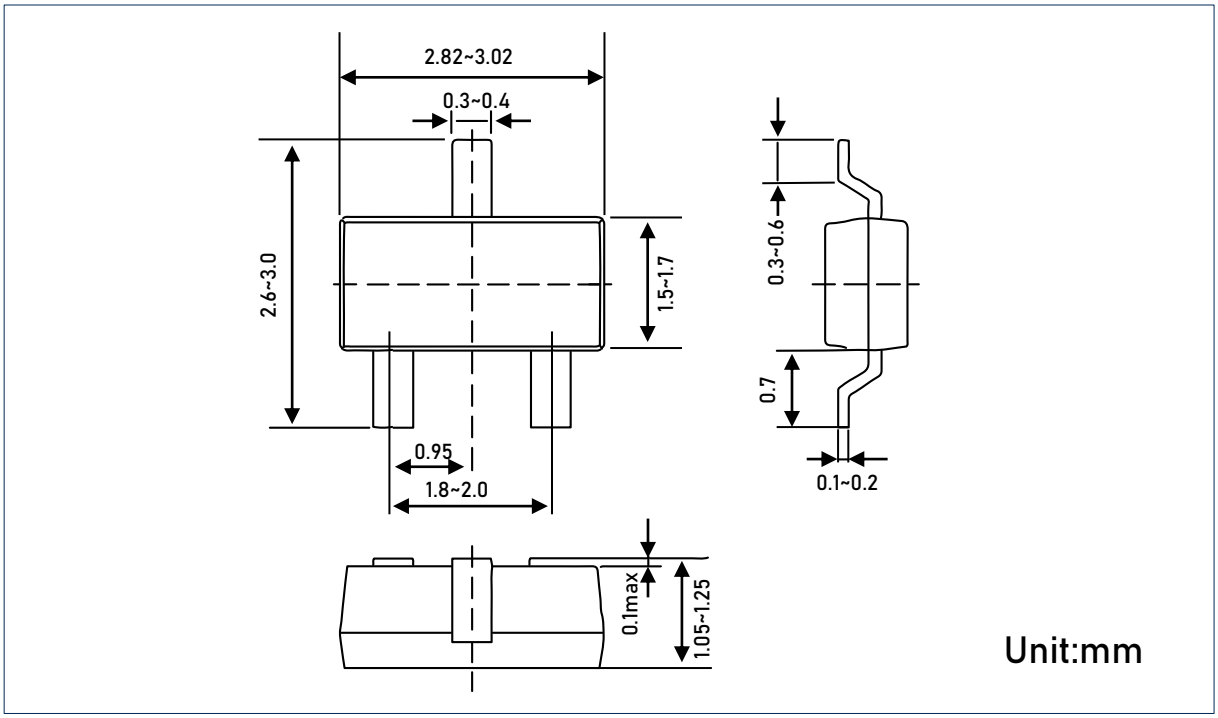
SOT-89



SOT23-5L



SOT23-3L



DFN1×1-4