

NTB25P06, NVB25P06

MOSFET – P-Channel, D²PAK -60 V, -27.5 A

Designed for low voltage, high speed switching applications and to withstand high energy in the avalanche and commutation modes.

Features

- AEC Q101 Qualified – NVB25P06
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- PWM Motor Controls
- Power Supplies
- Converters
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	-60	V
Gate-to-Source Voltage	V _{GS}	± 15	V
– Continuous	V _{GS}	± 15	V
– Non-Repetitive (t _p ≤ 10 μs)	V _{GSM}	± 20	Vpk
Drain Current	I _D	27.5	A
– Continuous @ T _A = 25°C	I _{DM}	80	Apk
– Single Pulse (t _p ≤ 10 μs)			
Total Power Dissipation @ T _A = 25°C	P _D	120	W
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 25 V, V _{GS} = 10 V, I _{L(pk)} = 20 A, L = 3 mH, R _G = 25 Ω)	E _{AS}	600	mJ
Thermal Resistance			°C/W
– Junction-to-Case	R _{θJC}	1.25	
– Junction-to-Ambient (Note 1)	R _{θJA}	46.8	
– Junction-to-Ambient (Note 2)	R _{θJA}	63.2	
Maximum Lead Temperature for Soldering Purposes, (1/8" from case for 10 s)	T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

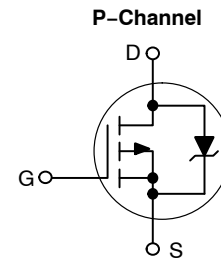
1. When surface mounted to an FR4 board using 1" pad size (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu Area 0.412 in²).



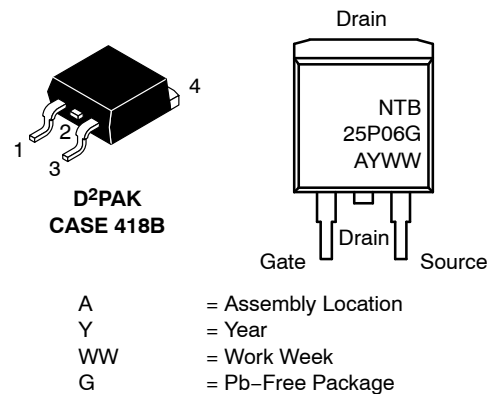
ON Semiconductor®

<http://onsemi.com>

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
-60 V	65 mΩ @ -10 V	-27.5 A



MARKING DIAGRAM & PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTB25P06T4G	D ² PAK (Pb-Free)	800 / Tape & Reel
NVB25P06T4G	D ² PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 V, I _D = -250 μA) (Positive Temperature Coefficient)	V _{(BR)DSS}	-60 -	- 64	- -	V mV/°C
Zero Gate Voltage Drain Current (V _{GS} = 0 V, V _{DS} = -60 V, T _J = 25°C) (V _{GS} = 0 V, V _{DS} = -60 V, T _J = 150°C)	I _{DSS}	- -	- -	-10 -100	μA
Gate-Body Leakage Current (V _{GS} = ±15 V, V _{DS} = 0 V)	I _{GSS}	-	-	±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = -250 μA) (Negative Threshold Temperature Coefficient)	V _{GS(th)}	-2.0 -	-2.8 6.2	-4.0 -	V mV/°C
Static Drain-Source On-State Resistance (V _{GS} = -10 V, I _D = -12.5 A) (V _{GS} = -10 V, I _D = -25 A)	R _{DS(on)}	- -	0.065 0.070	0.075 0.082	Ω
Forward Transconductance (V _{DS} = -10 V, I _D = -12.5 A)	g _{FS}	-	13	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = -25 V, V _{GS} = 0 V, F = 1.0 MHz)	C _{iss}	-	1200	1680	pF
Output Capacitance		C _{oss}	-	345	480	
Reverse Transfer Capacitance		C _{rss}	-	90	180	

SWITCHING CHARACTERISTICS (Notes 3 & 4)

Turn-On Delay Time	(V _{DD} = -30 V, I _D = -25 A, V _{GS} = -10 V R _G = 9.1 Ω)	t _{d(on)}	-	14	24	ns
Rise Time		t _r	-	72	118	ns
Turn-Off Delay Time		t _{d(off)}	-	43	68	ns
Fall Time		t _f	-	190	320	ns
Gate Charge	(V _{DS} = -48 V, I _D = -25 A, V _{GS} = -10 V)	Q _T	-	33	50	nC
		Q ₁	-	6.5	-	
		Q ₂	-	15	-	

BODY-DRAIN DIODE RATINGS (Note 3)

Diode Forward On-Voltage (I _S = -25 A, V _{GS} = 0 V) (I _S = -25 A, V _{GS} = 0 V, T _J = 150°C)	V _{SD}	- -	-1.8 -1.4	-2.5 -	V
Reverse Recovery Time	t _{rr}	-	70	-	ns
	t _a	-	50	-	
	t _b	-	20	-	
Reverse Recovery Stored Charge	Q _{RR}	-	0.2	-	μC

3. Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

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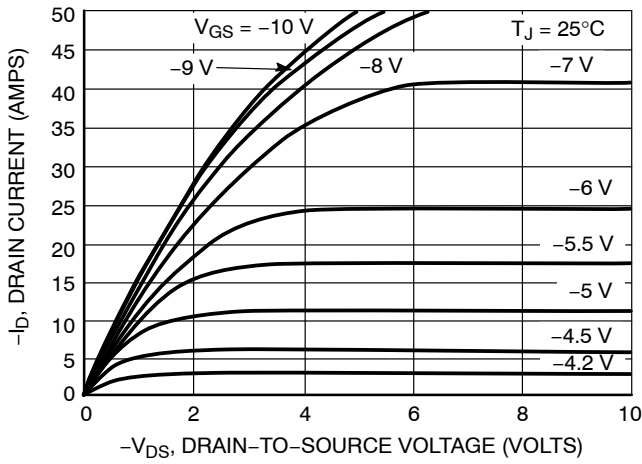


Figure 1. On-Region Characteristics

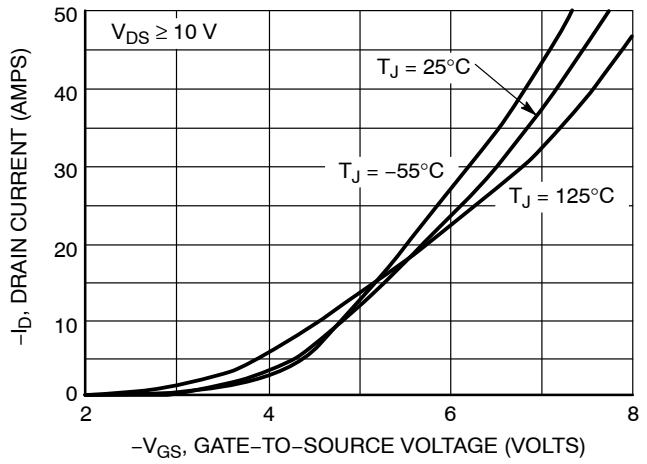


Figure 2. Transfer Characteristics

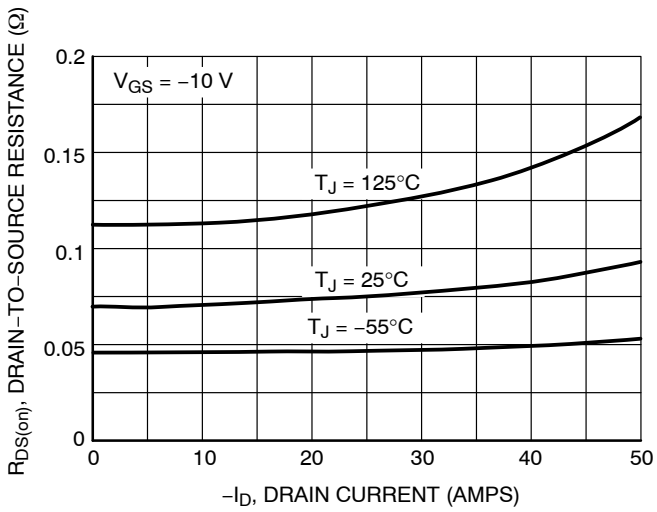


Figure 3. On-Resistance vs. Drain Current and Temperature

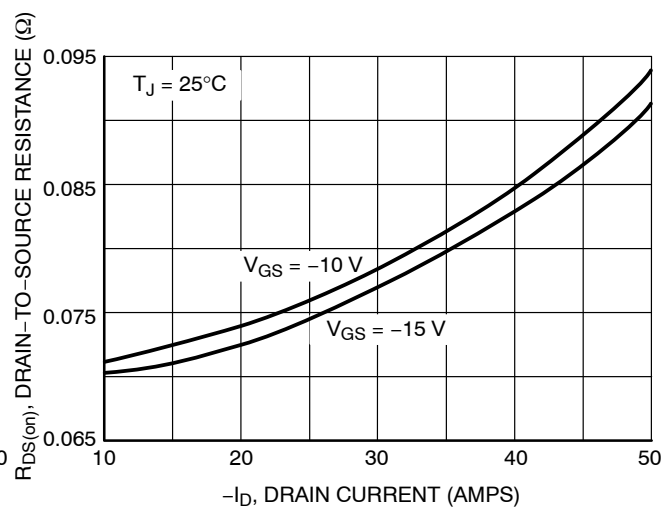


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

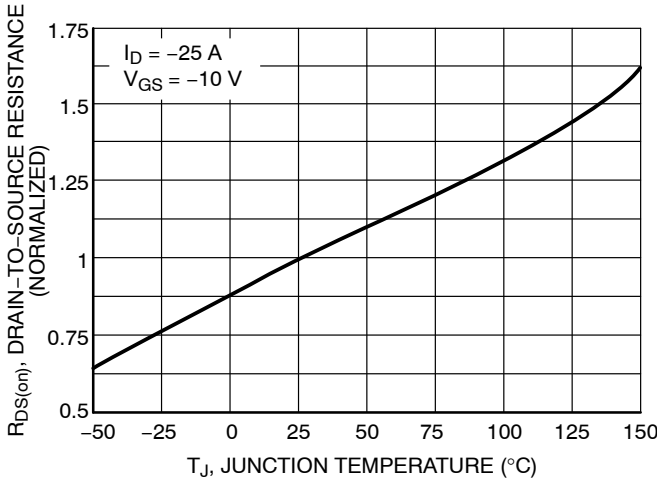


Figure 5. On-Resistance Variation with Temperature

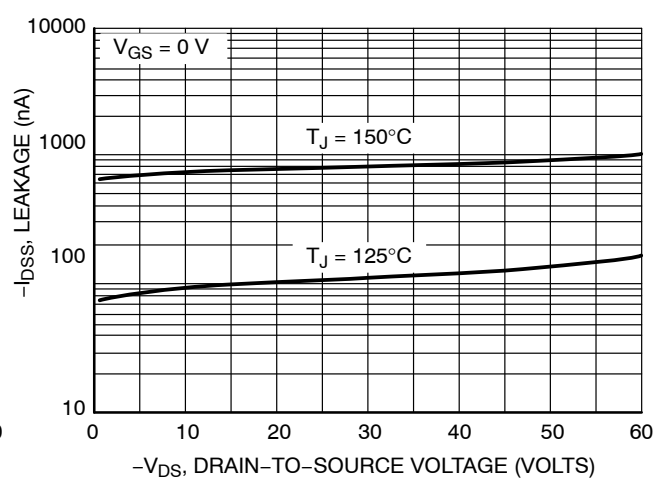


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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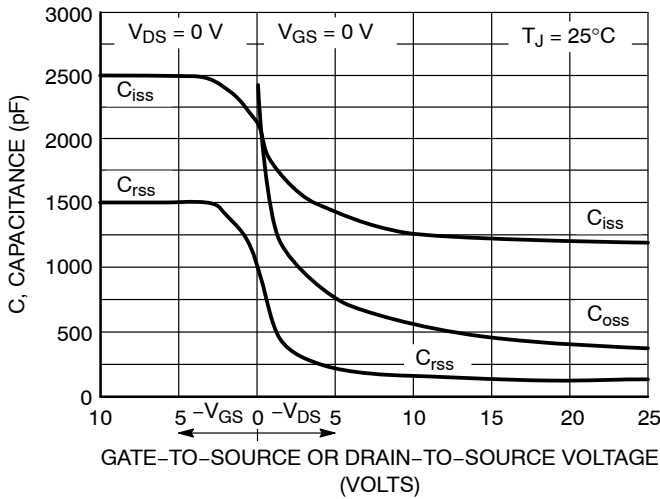


Figure 7. Capacitance Variation

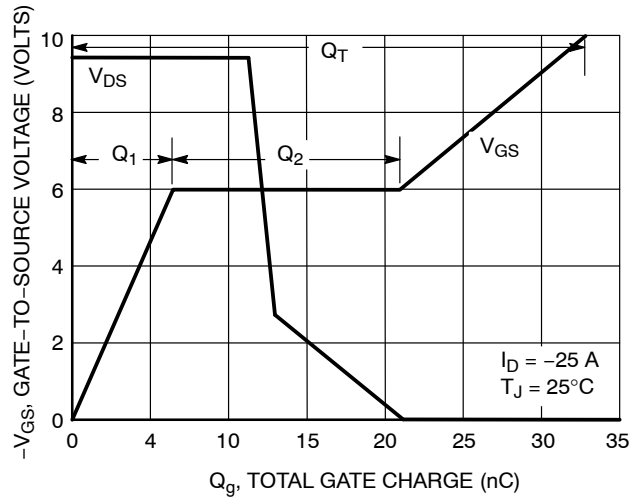


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

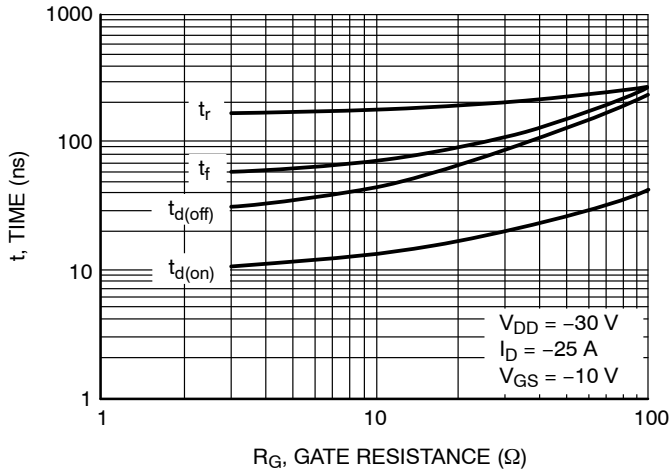


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

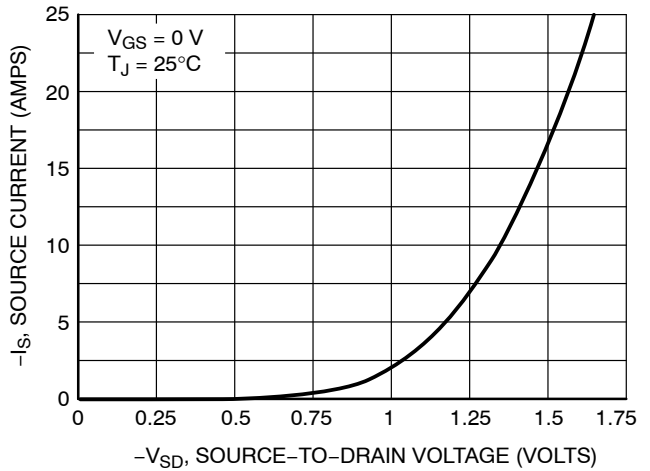


Figure 10. Diode Forward Voltage vs. Current

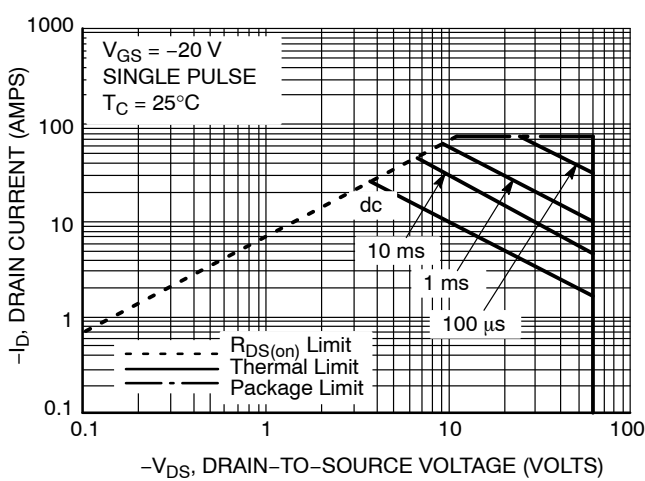


Figure 11. Maximum Rated Forward Biased Safe Operating Area

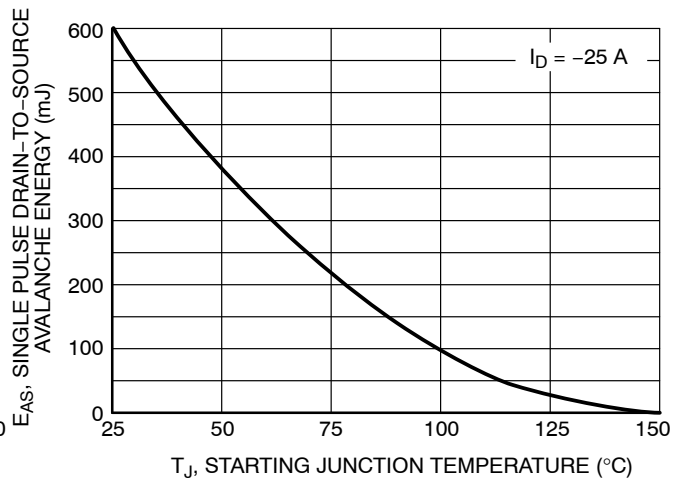


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

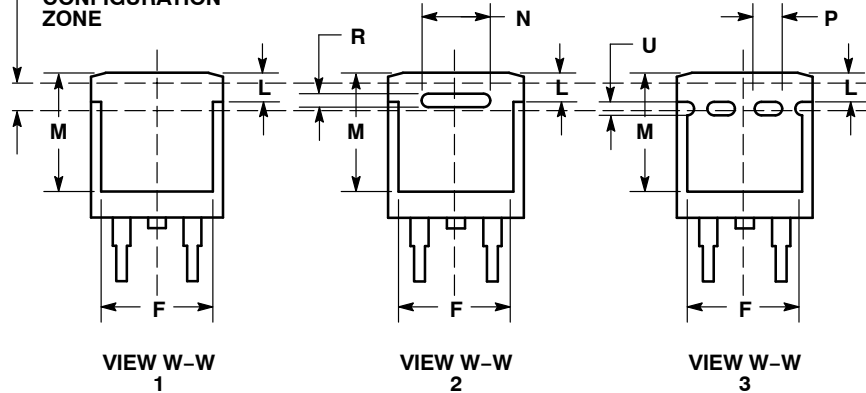
SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



- | | | | | | |
|---|--|--|---|--|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE | STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE |
|---|--|--|---|--|---|

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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

**GENERIC
MARKING DIAGRAM***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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