NTHD3102C

MOSFET – Power, Complementary, ChipFET
20 V, +5.5 A /-4.2 A

ON Semiconductor®

http://onsemi.com

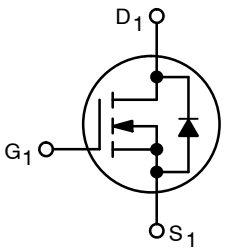
Features

- Complementary N−Channel and P−Channel MOSFET
- Small Size, 40% Smaller than TSOP−6 Package
- Leadless SMD Package Provides Great Thermal Characteristics
- Leading Edge Trench Technology for Low On Resistance
- Reduced Gate Charge to Improve Switching Response
- This is a Pb−Free Device

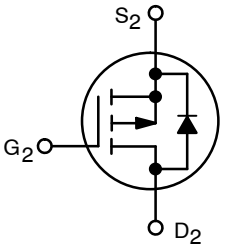
Applications

- DC−DC Conversion Circuits
- Load/Power Switching
- Single or Dual Cell Li−Ion Battery Supplied Devices
- Ideal for Power Management Applications in Portable, Battery Powered Products

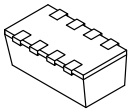
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX (Note 1)
N−Channel 20 V	29 mΩ @ 4.5 V	5.5 A
	37 mΩ @ 2.5 V	
	48 mΩ @ 1.8 V	
P−Channel −20 V	64 mΩ @ 4.5 V	−4.2 A
	83 mΩ @ 2.5 V	
	105 mΩ @ 1.8 V	



N−Channel MOSFET



P−Channel MOSFET



ChipFET
CASE 1206A
STYLE 2

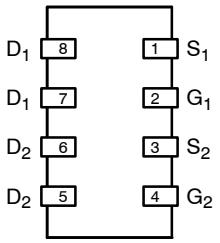
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage	N−Ch		V_{GS}	±8.0	V
	P−Ch			±8.0	
N−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	4.0	A
		T_A = 85°C		2.9	
	t ≤ 5 s	T_A = 25°C		5.5	
P−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	3.1	A
		T_A = 85°C		2.2	
	t ≤ 5 s	T_A = 25°C		4.2	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.1	W
	t ≤ 5 s			2.1	
Gate−to−Source ESD Rating − (Human Body Model, Method 3015)			ESD	100	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

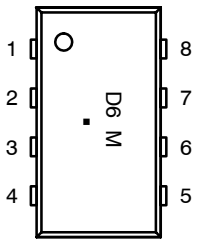
1. Surface−mounted on FR4 board using 1 in sq pad size (Cu. area = 1.127 in sq [1 oz] including traces).

PIN CONNECTIONS



(Bottom View)

MARKING DIAGRAM



(Top View)

D6 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

MAXIMUM RATINGS (continued) (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
N−Channel Continuous Drain Current (Note 3)	Steady State	T_A = 25°C	I_D	3.0	A
		T_A = 85°C		2.2	
P−Channel Continuous Drain Current (Note 3)	Steady State	T_A = 25°C	I_D	2.3	A
		T_A = 85°C		1.7	
Power Dissipation (Note 3)		T_A = 25°C	P_D	0.6	W
Pulsed Drain Current	N−Ch	tp = 10 μs	I_{DM}	16	A
	P−Ch			12.6	
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	1.7	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	110	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 2)		60	
Junction−to−Ambient − Steady State (Note 3)		195	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage (Note 4)	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	20			V
		P		I_D = −250 μA	−20			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	N				20.2		mV/°C
		P				16.2		
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25 °C			1.0	μA
		P	V_{GS} = 0 V, V_{DS} = −16 V				−1.0	
		N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 85 °C			5.0	
		P	V_{GS} = 0 V, V_{DS} = −16 V				−5.0	
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	nA
		P	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
3. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq).
4. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	I_D = 250 μA	0.4		1.2	V
		P		I_D = −250 μA	−0.4		−1.2	
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V , I_D = 4.4 A			29	45	mΩ
		P	V_{GS} = −4.5 V , I_D = −3.2 A			64	80	
		N	V_{GS} = 2.5 V , I_D = 4.1 A			37	50	
		P	V_{GS} = −2.5 V, I_D = −2.5 A			83	110	
		N	V_{GS} = 1.8 V , I_D = 1.9 A			48	70	
		P	V_{GS} = −1.8 V, I_D = −0.6 A			105	150	
Forward Transconductance	g_{FS}	N	V_{DS} = 10 V, I_D = 4.4 A			7.7		S
		P	V_{DS} = −10 V , I_D = −3.2 A			5.9		
CHARGES, CAPACITANCES AND GATE RESISTANCE								
Input Capacitance	C_{ISS}	N	f = 1.0 MHz, V_{GS} = 0 V	V_{DS} = 10 V		510		pF
		P		V_{DS} = −10 V		650		
Output Capacitance	C_{OSS}	N		V_{DS} = 10 V		100		
		P		V_{DS} = −10 V		100		
Reverse Transfer Capacitance	C_{RSS}	N		V_{DS} = 10 V		50		
		P		V_{DS} = −10 V		50		
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 4.4 A			5.8	7.9	nC
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −3.2 A			6.6	8.9	
Threshold Gate Charge	$Q_{G(TH)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 4.4 A			0.96		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −3.2 A			0.98		
Gate−to−Source Charge	Q_{GS}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 4.4 A			1.2		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −3.2 A			1.4		
Gate−to−Drain Charge	Q_{GD}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 4.4 A			1.56		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −3.2 A			1.64		
SWITCHING CHARACTERISTICS (Note 6)								
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 4.4 A, R_G = 2.5 Ω			7.2		ns
Rise Time	t_r					15.9		
Turn−Off Delay Time	$t_{d(OFF)}$					15.7		
Fall Time	t_f					4.6		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −3.2 A, R_G = 2.5 Ω			6.4		
Rise Time	t_r					16.9		
Turn−Off Delay Time	$t_{d(OFF)}$					16.4		
Fall Time	t_f					15.0		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, T_J = 25 °C	I_S = 1.7 A		0.68	1.2	V
		P		I_S = −1.7 A		−0.7	−1.2	
Reverse Recovery Time	t_{RR}	N	V_{GS} = 0 V, dI_S / dt = 100 A/μs	I_S = 1.7 A		13.5		ns
		P		I_S = −1.7 A		12.6		
Charge Time	t_a	N		I_S = 1.7 A		8.6		
		P		I_S = −1.7 A		8.4		
Discharge Time	t_b	N		I_S = 1.7 A		4.9		
		P		I_S = −1.7 A		4.2		
Reverse Recovery Charge	Q_{RR}	N		I_S = 1.7 A		7.0		nC
		P		I_S = −1.7 A		6.0		

TYPICAL N−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

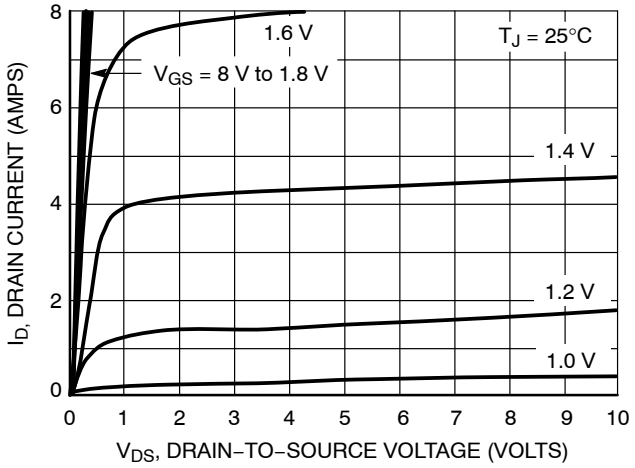


Figure 1. On−Region Characteristics

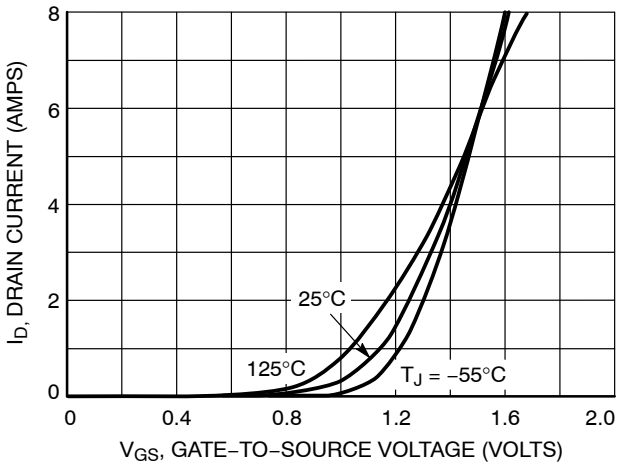


Figure 2. Transfer Characteristics

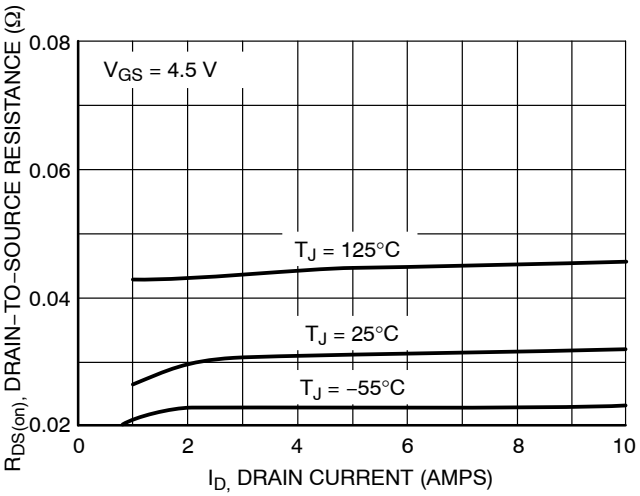


Figure 3. On−Resistance vs. Drain Current

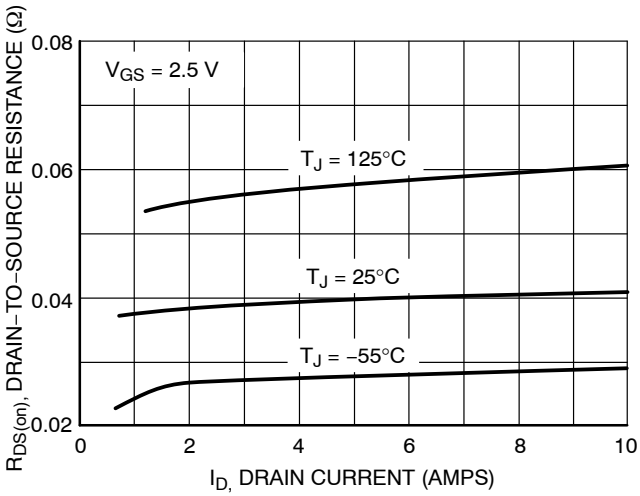


Figure 4. On−Resistance vs. Drain Current and Temperature

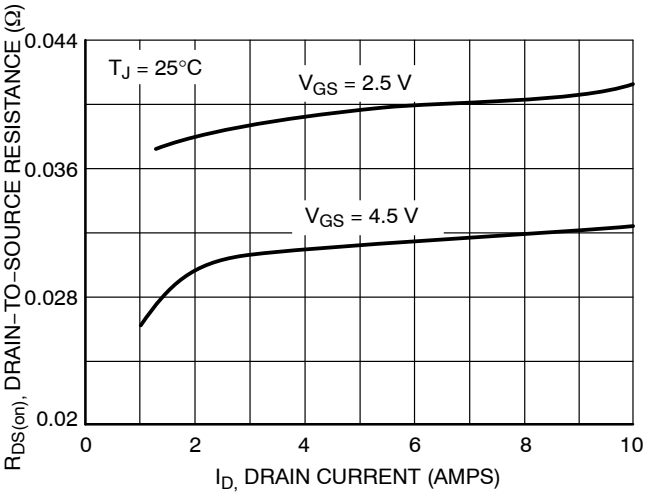


Figure 5. On−Resistance vs. Drain Current

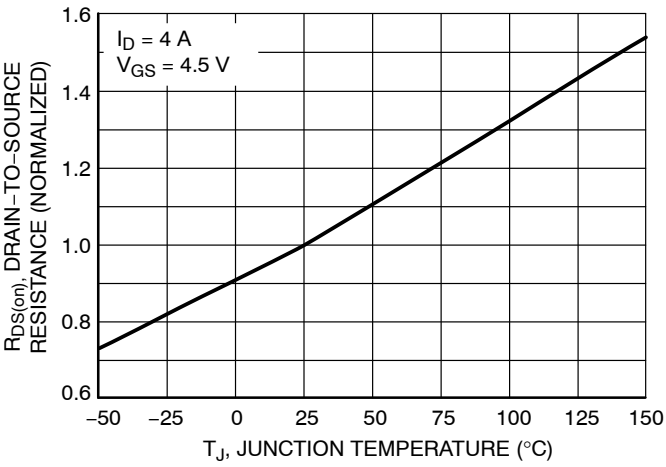


Figure 6. On−Resistance Variation with Temperature

TYPICAL N−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

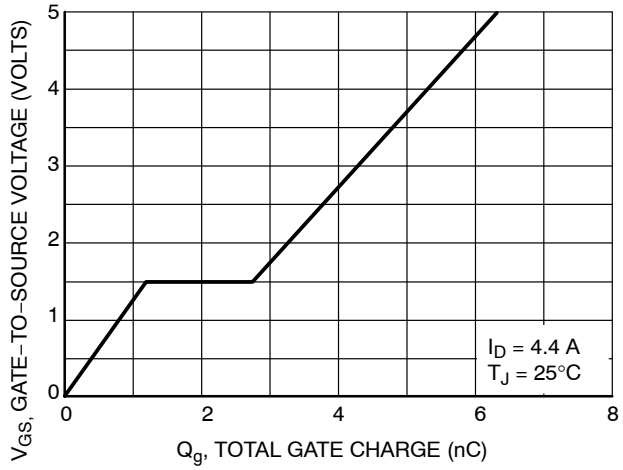


Figure 7. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

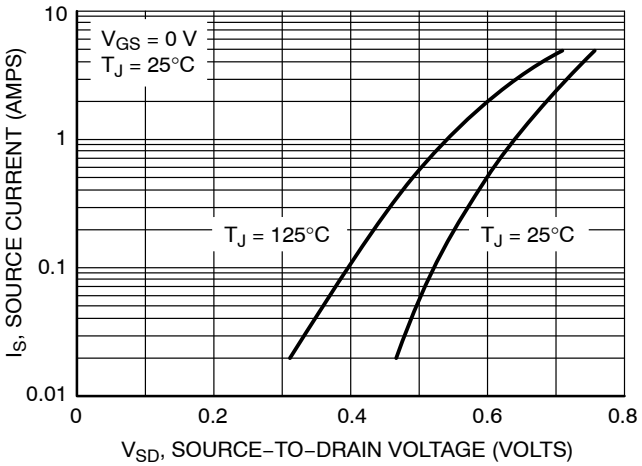


Figure 8. Diode Forward Voltage vs. Current

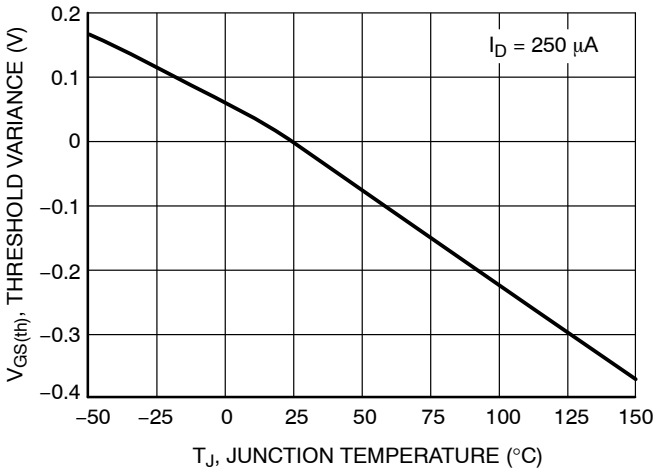


Figure 9. Threshold Voltage

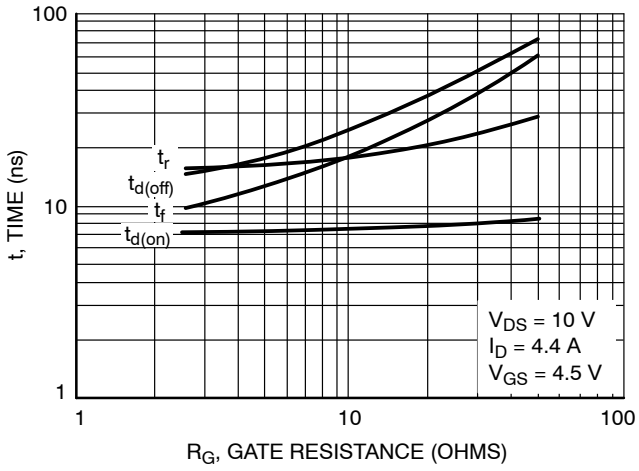


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

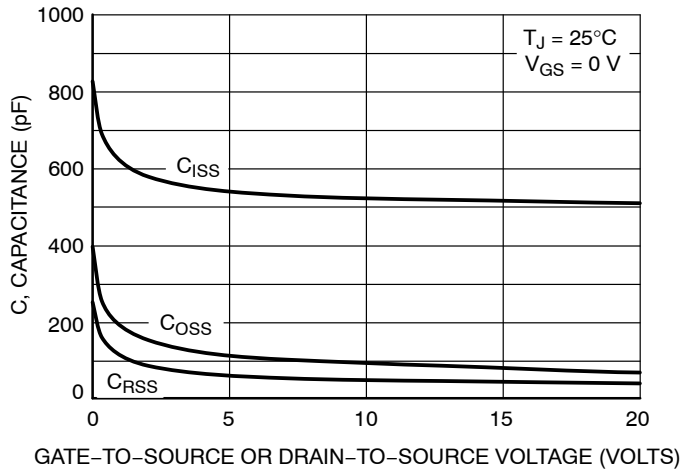


Figure 11. Capacitance Variation

TYPICAL P−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

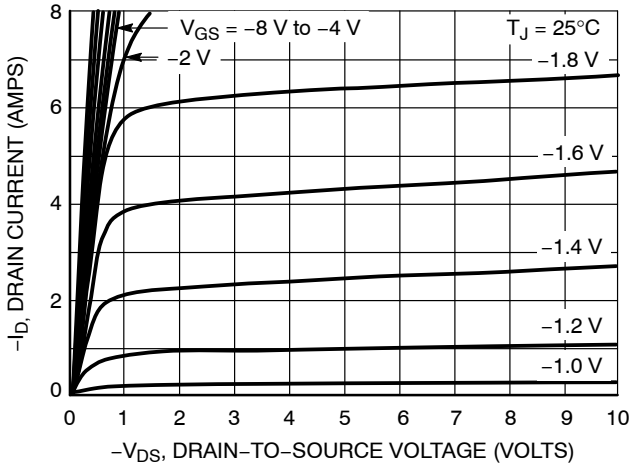


Figure 12. On−Region Characteristics

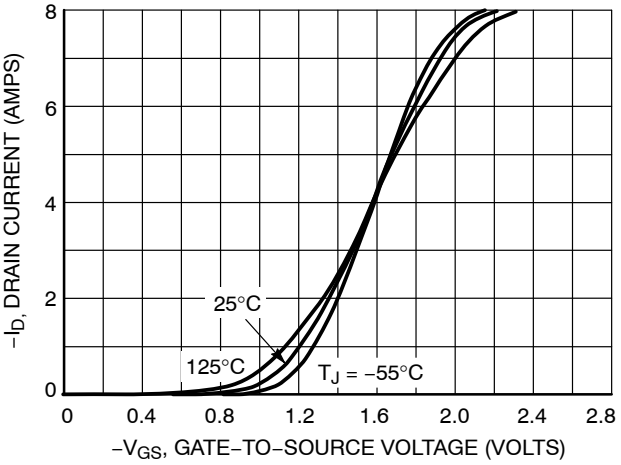


Figure 13. Transfer Characteristics

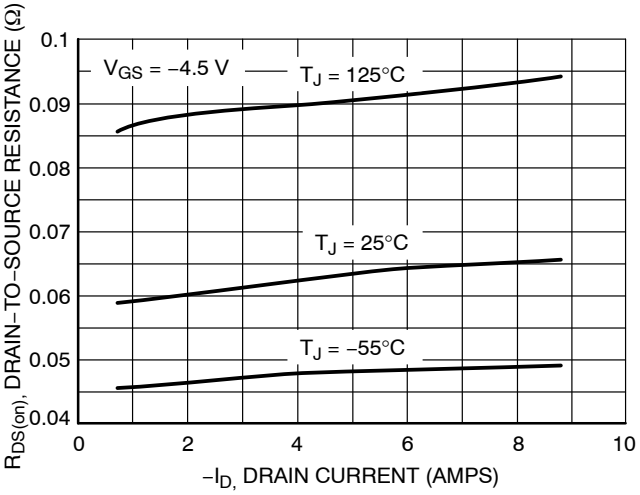


Figure 14. On−Resistance vs. Drain Current

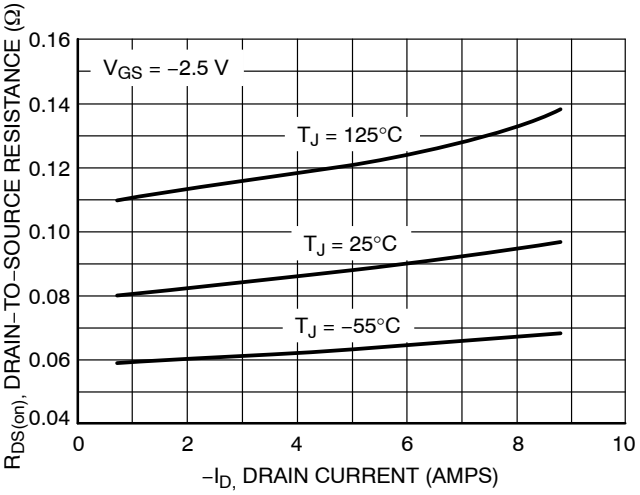


Figure 15. On−Resistance vs. Drain Current and Temperature

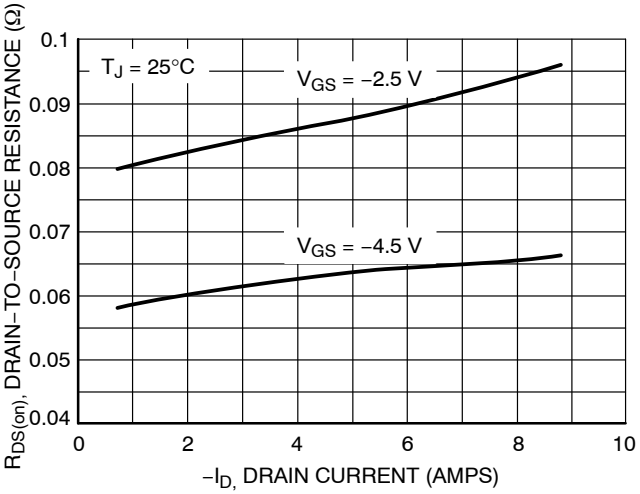


Figure 16. On−Resistance vs. Drain Current

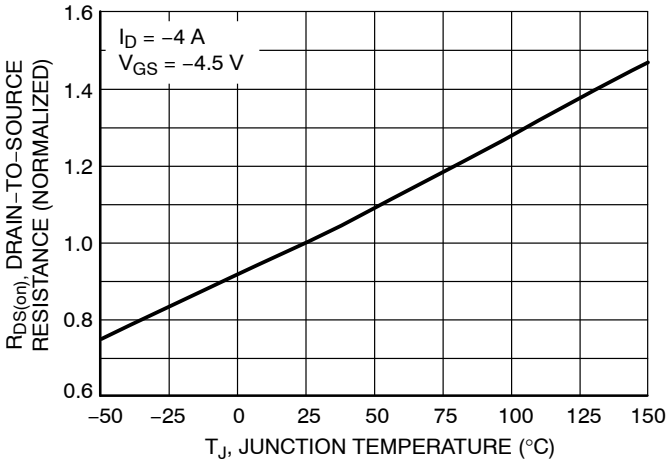


Figure 17. On−Resistance Variation with Temperature

TYPICAL P−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

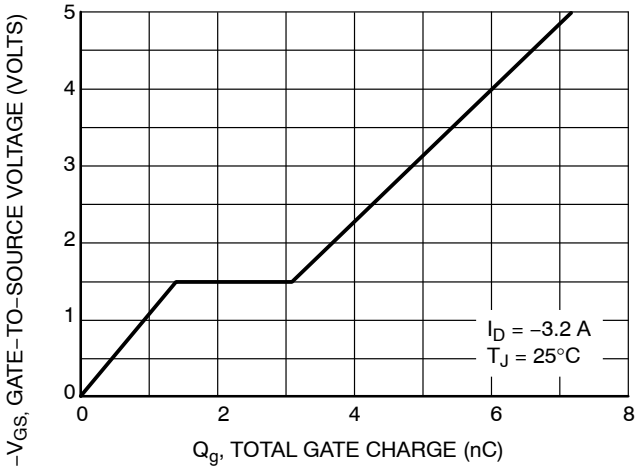


Figure 18. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

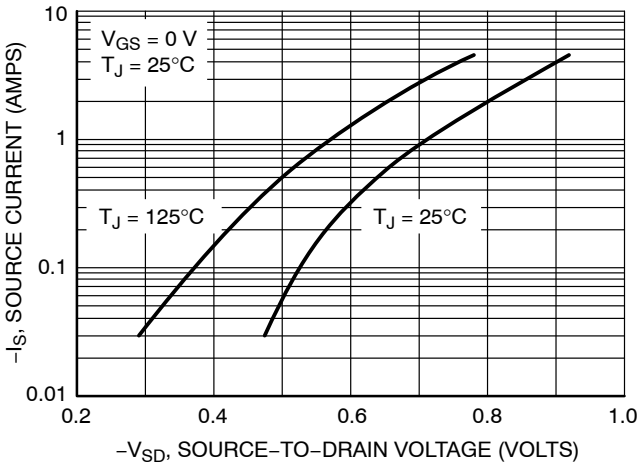


Figure 19. Diode Forward Voltage vs. Current

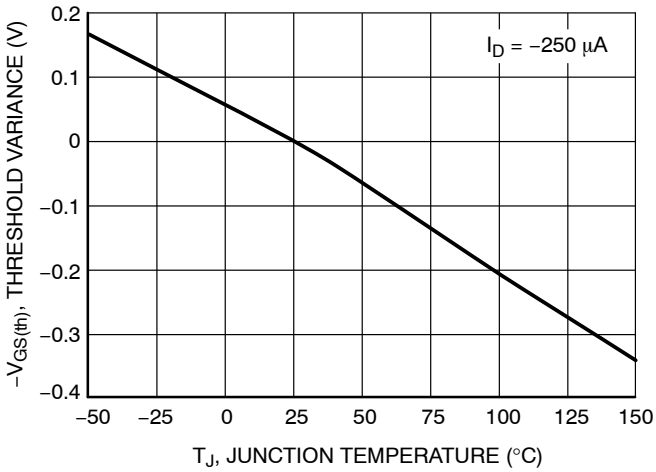


Figure 20. Threshold Voltage

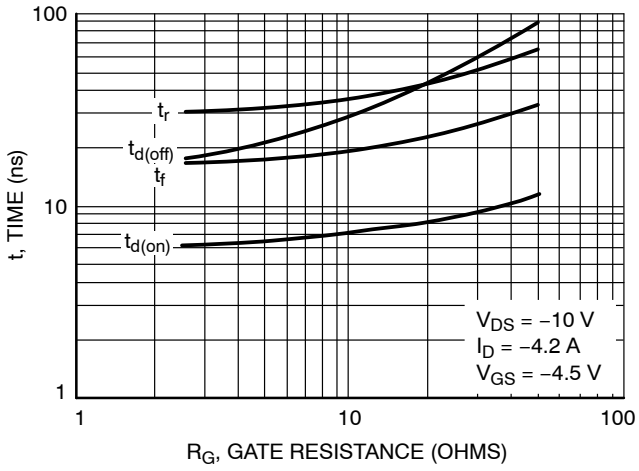


Figure 21. Resistive Switching Time Variation vs. Gate Resistance

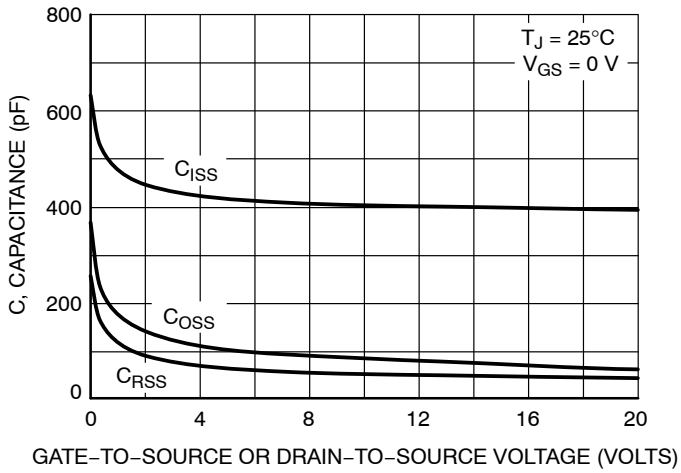


Figure 22. Capacitance Variation

TYPICAL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

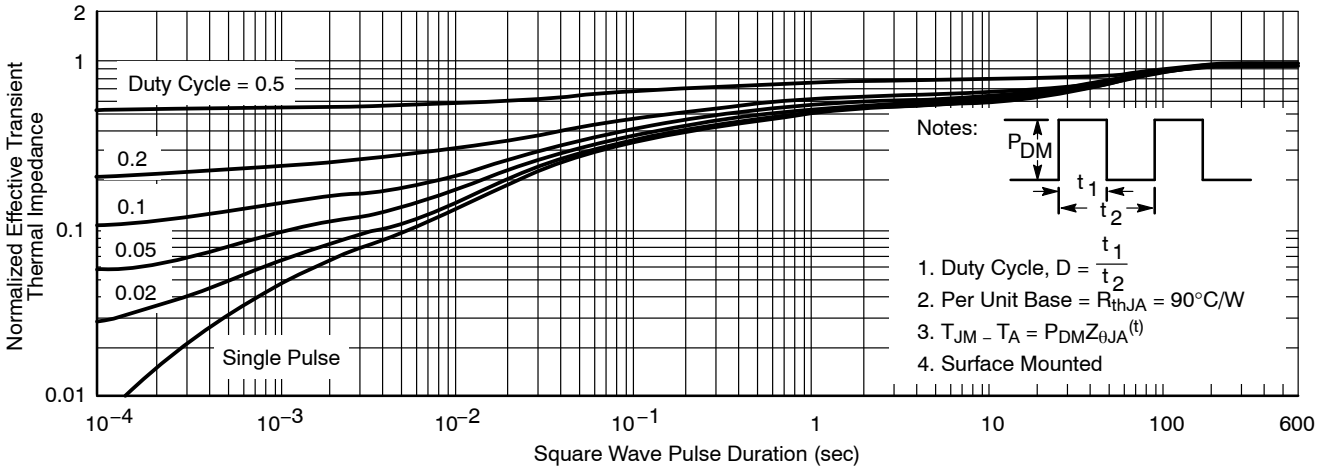


Figure 23. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping†
NTHD3102CT1G	ChipFET (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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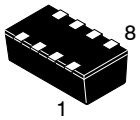
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

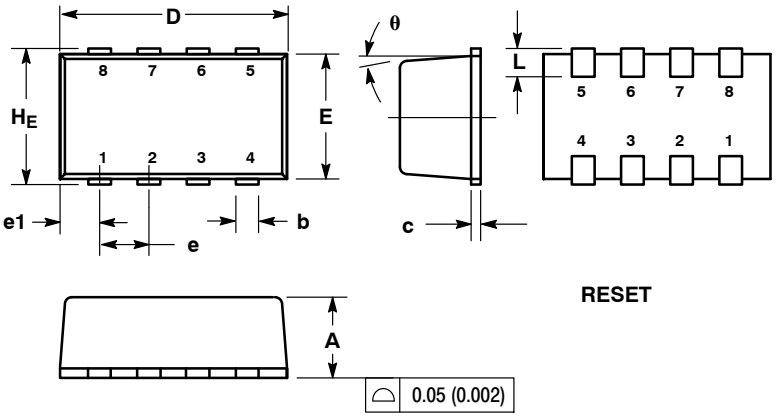
ON Semiconductor®

ChipFET™
CASE1206A−03
ISSUE K

DATE 19 MAY 2009



SCALE 1:1



RESET

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

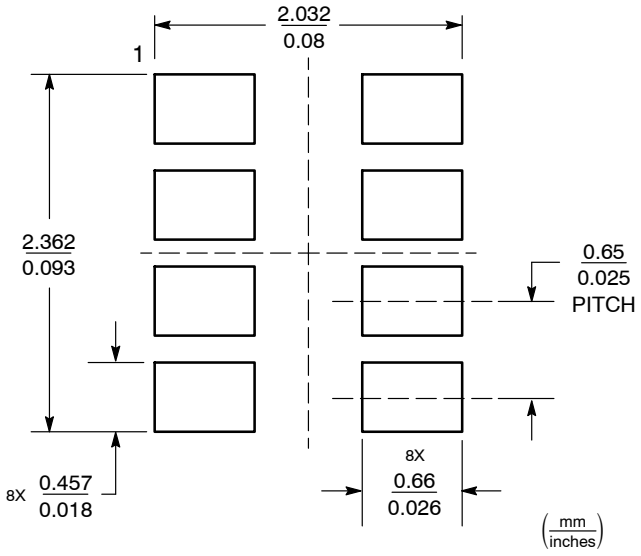
STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

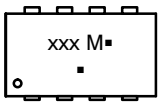
STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



xxx = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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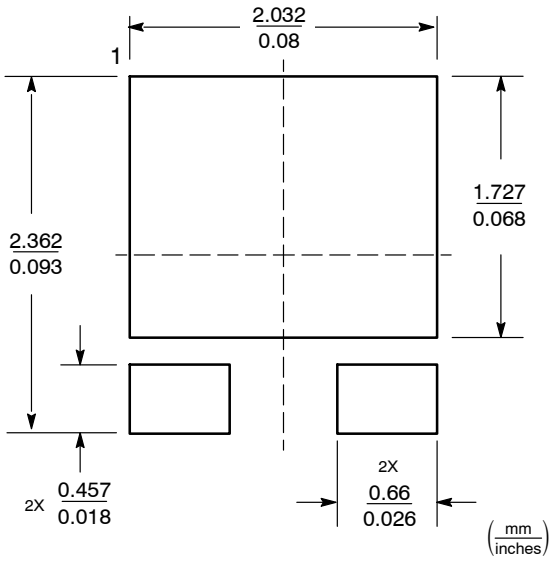
DESCRIPTION:	**ChipFET**	**PAGE 1 OF 2**

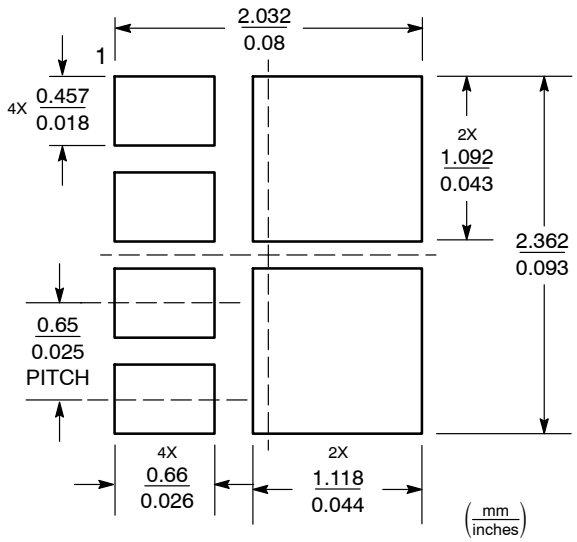
ChipFET™
CASE 1206A−03
ISSUE K

DATE 19 MAY 2009

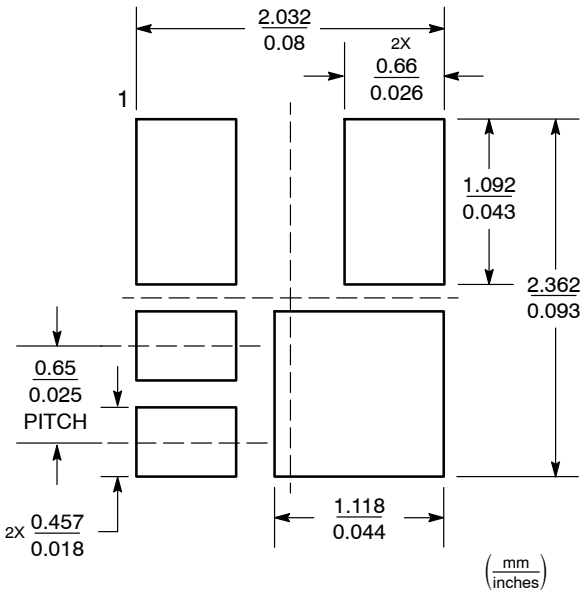
ADDITIONAL SOLDERING FOOTPRINTS*



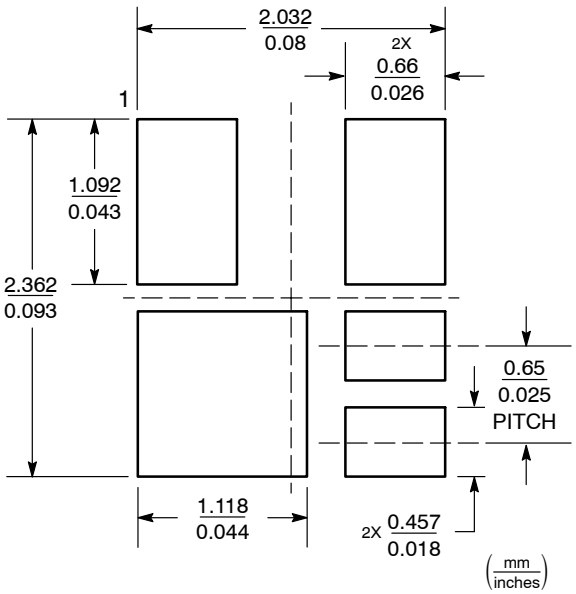
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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