

大电流、高侧与低侧、栅极驱动 IC

FAN7392

说明

FAN7392 是单片高侧和低侧栅极驱动 IC，可以驱动工作电压最高达 +600 V 的高速 MOSFET 和 IGBT。它具有缓冲输出级，且所有 NMOS 晶体管设计为具有高脉冲电流驱动能力和最低交叠导通。飞兆的高压工艺和共模噪声消除技术可使高侧驱动器在高 dv/dt 噪声环境下稳定运行。先进的电平转换电路，能使高侧栅极驱动器的工作电压在 $V_{BS} = 15\text{ V}$ 时 V_S 达到 -9.8 V (典型值)。逻辑输入与兼容标准 CMOS 或 LSTTL 输出，低至 3.3 V 逻辑。UVLO 电路可防止 V_{CC} 和 V_{BS} 低于指定的阈值电压时发生故障。大电流和低输出压降的特性，使得该器件适合半桥和全桥转换器，如开关电源和大功率 DC-DC 转换器应用。

特性

- 浮动通道可实现高达+600 V 的自举运行
- 3 A/3 A 的典型源电流 / 灌电流驱动能力
- 共模 dv/dt 噪声消除电路
- 兼容 3.3 V 逻辑输入电平
- 单独逻辑供电 (V_{DD})，范围为 3.3 V 至 20 V
- V_{CC} 和 V_{BS} 欠压锁定
- 逐周期边沿触发关闭逻辑
- 适用于两个通道的匹配传播延迟
- 输出与输入信号同相
- 采用 14-DIP 和 16-SOP (宽) 封装
- This is a Pb-Free Device

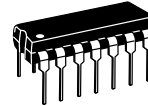
应用

- 高速功率 MOSFET 和 IGBT 栅极驱动器
- 服务器电源
- 不间断电源 (UPS)
- 电信系统电源
- 分布式电源
- 电机驱动变频器

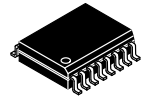


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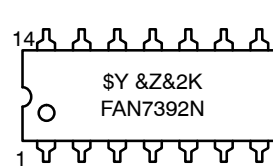


PDIP-14
14-PDIP
CASE 646-06

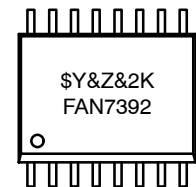


SOIC-16
16-SOP
CASE 751BH-01

MARKING DIAGRAM



FAN7392N



FAN7392MX

FAN7392N = Device Code
FAN7392

&Z = Assembly Plant Code
&2 = 2-Digit Date Code
&K = 2-Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

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典型应用电路图

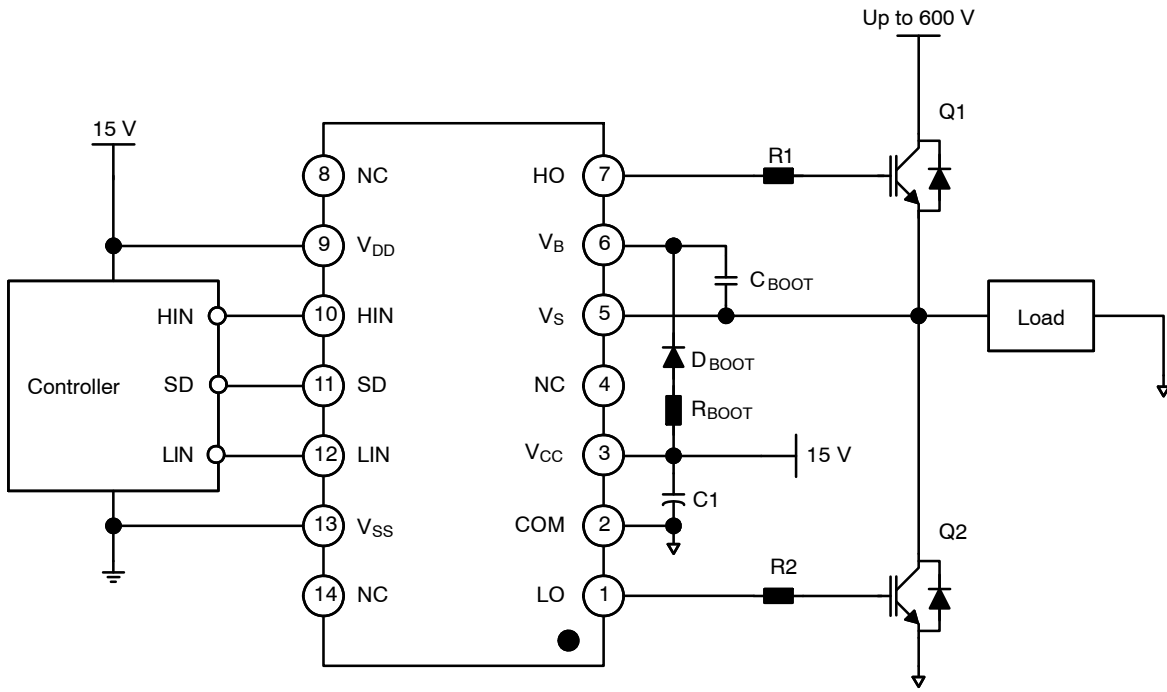


图 1. 典型应用电路 (参考 14-DIP)

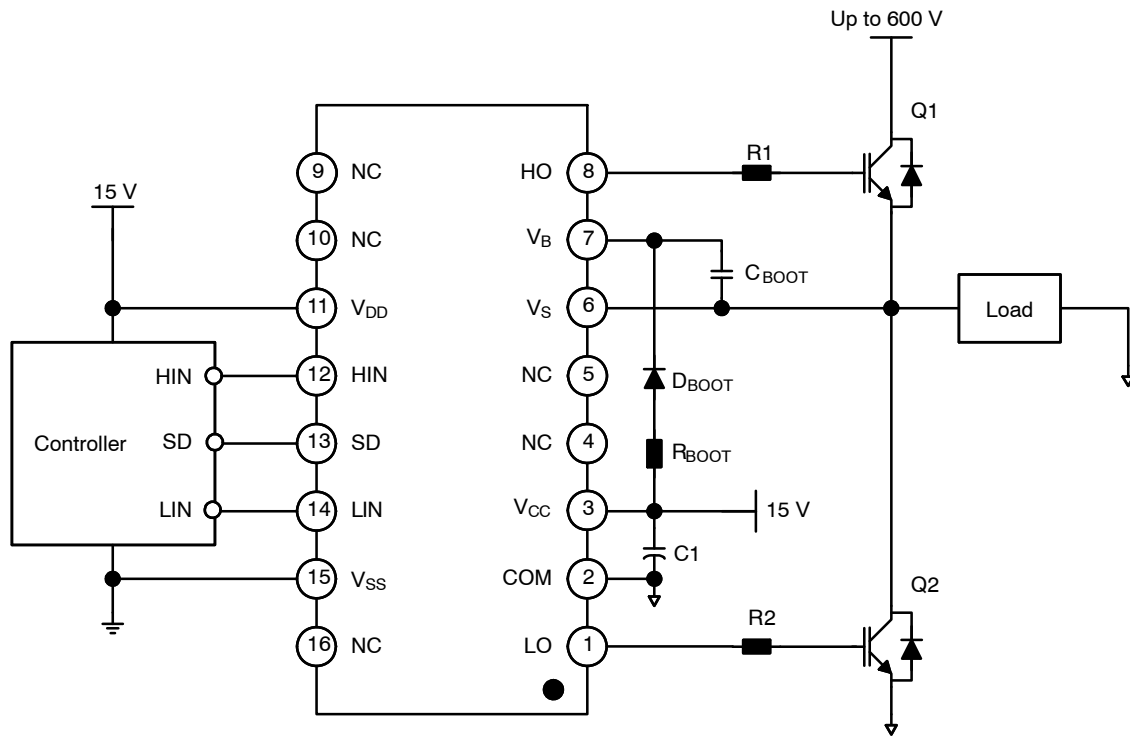


图 2. 典型应用电路 (参考 16-SOP)

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内部框图

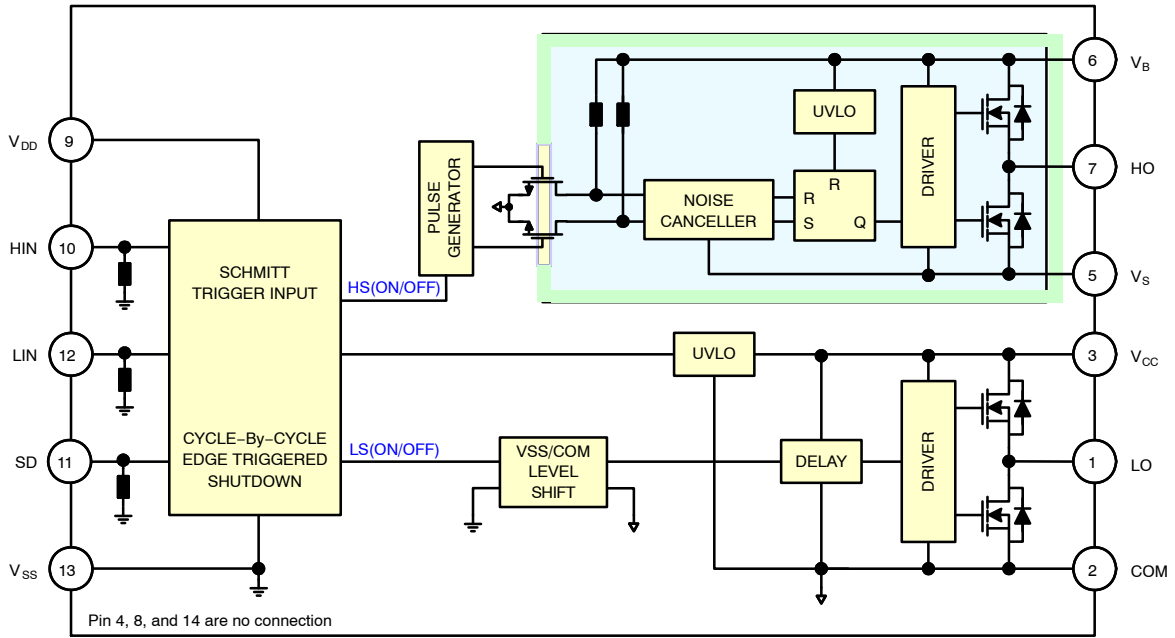


图 3. 功能框图 (参考 14 引脚)

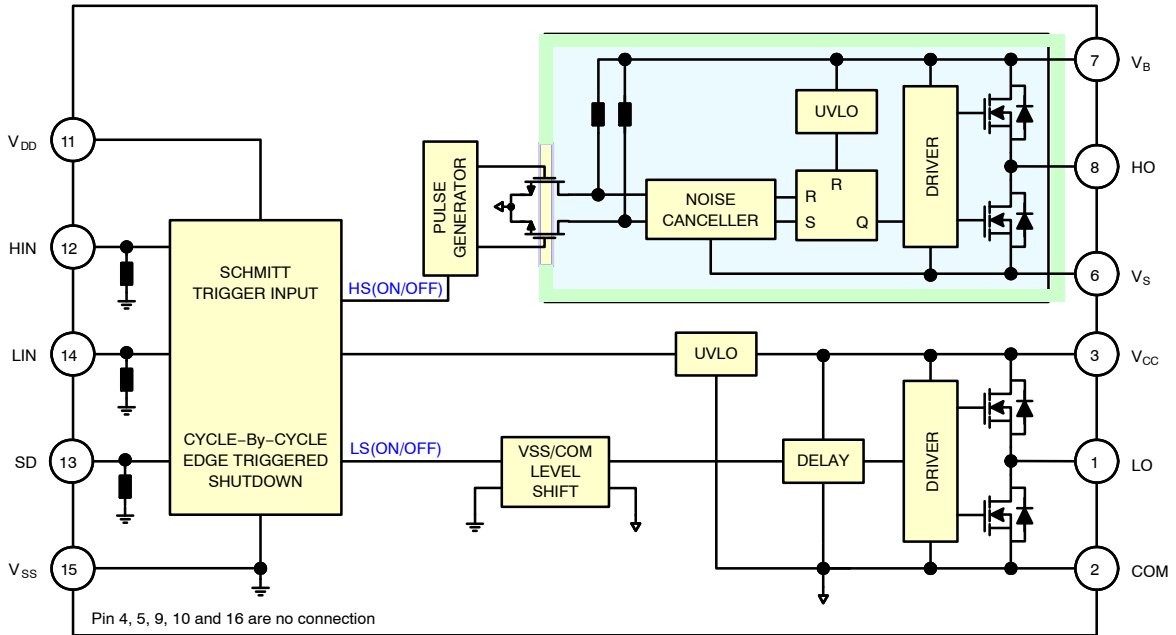


图 4. 功能框图 (参考16-SOP)

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引脚布局

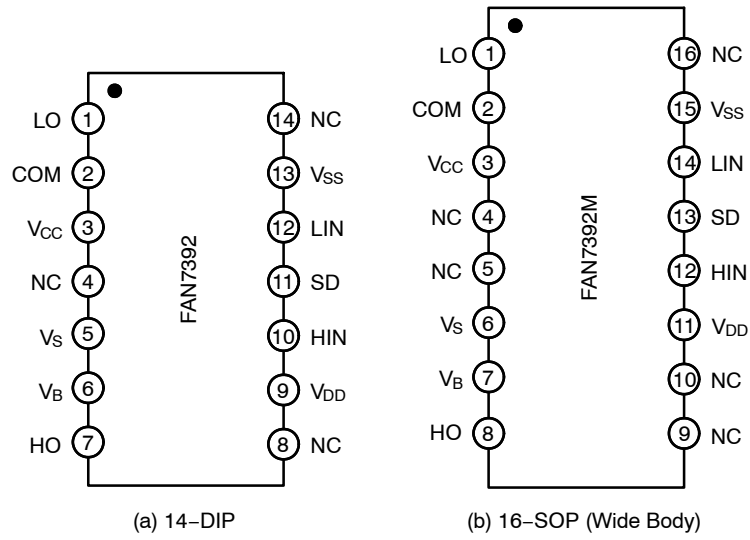


图 5. 引脚布局 (俯视图)

引脚定义

14 引脚	16 引脚	名称	说明
1	1	LO	低侧栅极输出
2	2	COM	低侧返回
3	3	V _{CC}	低侧电源电压
5	6	V _S	高侧浮动电源电压返回
6	7	V _B	高侧浮动电源
7	8	HO	高侧驱动输出
9	11	V _{DD}	逻辑电源电压
10	12	HIN	高侧栅极驱动器输出的逻辑输入
11	13	SD	关闭功能逻辑输入
12	14	LIN	低侧栅极驱动器输出的逻辑输入
13	15	V _{SS}	逻辑地
4, 8, 14	4, 5, 9, 10, 16	NC	未连接

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绝对最大额定值 (除非另有说明, $T_A = 25^\circ\text{C}$ 。)

符号	特性	最小值	最大值	单位	
V_B	高侧浮动电源电压	-0.3	625.0	V	
V_S	高侧浮动偏置电压	$V_B - 25.0$	$V_B + 0.3$	V	
V_{HO}	高侧浮动输出电压	$V_S - 0.3$	$V_B + 0.3$	V	
V_{CC}	低侧电源电压	-0.3	25.0	V	
V_{LO}	低侧浮动输出电压	-0.3	$V_{CC} + 0.3$	V	
V_{DD}	逻辑电源电压	-0.3	$V_{SS} + 25.0$	V	
V_{SS}	逻辑电源偏置电压	$V_{CC} - 25.0$	$V_{CC} + 0.3$	V	
V_{IN}	逻辑输入电压 (HIN、LIN 和 SD)	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V	
dV_S/dt	允许的偏置电压变化速率	-	± 50	V/ns	
P_D	功耗 (注意 1, 2, 3)	14-PDIP	-	1.6	W
		16-SOP	-	1.3	
θ_{JA}	热阻	14-PDIP	-	75	$^\circ\text{C}/\text{W}$
		16-SOP	-	95	
T_J	最大结温	-	+150	$^\circ\text{C}$	
T_{STG}	存储温度	-55	+150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

(参考译文)

如果电压超过最大额定值表中列出的值范围, 器件可能会损坏。如果超过任何这些限值, 将无法保证器件功能, 可能会导致器件损坏, 影响可靠性。

1. 安装到 76.2 x 114.3 x 1.6 mm PCB 板 (FR-4 环氧玻璃材料)。
2. 参考下列标准:
JESD51-2: 集成电路热测试方法环境条件 - 自然通风和
JESD51-3: 含铅表面贴装封装的低有效导热系数测试板
3. 任何情况下都不得超过功耗 (P_D)。

推荐工作条件

符号	参数	最小值	最大值	单位
V_B	高侧浮动电源电压	$V_S + 10$	$V_S + 20$	V
V_S	高侧浮动电源偏置电压	$6 - V_{CC}$	600	V
V_{HO}	高侧输出电压	V_S	V_B	V
V_{CC}	低侧电源电压	10	20	V
V_{LO}	低侧输出电压	0	V_{CC}	V
V_{DD}	逻辑电源电压	$V_{SS} + 3$	$V_{SS} + 20$	V
V_{SS}	逻辑电源偏置电压	-5	5	V
V_{IN}	逻辑输入电压	V_{SS}	V_{DD}	V
T_A	工作环境温度	-40	+125	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

(参考译文)

高于推荐工作范围表格中所列电压时, 不保证能够正常运行。长时间在推荐工作范围表格中规定范围以外的电压下运行, 可能会影响器件的可靠性。

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电气特性 (除非另有说明, V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15.0 V, $V_{SS} = COM = 0$ V, $T_A = 25^\circ\text{C}$ 。 V_{IH} 、 V_{IL} 和 I_{IN} 参数以 V_{SS} 为参考点, 并适用于相应的输入引脚: HIN、LIN 和 SD。 V_O 和 I_O 参数以 V_S 和 COM 点, 并适用于相应的输出引脚: HO 和 LO。)

符号	特性	测试条件	最小值	典型值	最大值	单位
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低侧电源部分

I_{QCC}	V_{CC} 静态电源电流	$V_{IN} = 0$ V 或 V_{DD}	-	40	80	μA
I_{QDD}	V_{DD} 静态电源电流	$V_{IN} = 0$ V 或 V_{DD}	-	-	10	μA
I_{PCC}	V_{CC} 工作电源电流	$f_{IN} = 20$ kHz (均方根), $V_{IN} = 15$ V _{PP}	-	430	-	μA
I_{PDD}	V_{DD} 工作电源电流	$f_{IN} = 20$ kHz (均方根), $V_{IN} = 15$ V _{PP}	-	300	-	μA
I_{SD}	关闭电源电流	$S_D = V_{DD}$	-	120	-	μA
V_{CCUV+}	V_{CC} 电源欠压正向阈值电压	$V_{IN} = 0$ V, $V_{CC} =$ 扫描	7.7	8.8	9.9	V
V_{CCUV-}	V_{CC} 电源欠压负向阈值电压	$V_{IN} = 0$ V, $V_{CC} =$ 扫描	7.3	8.4	9.5	V
V_{CCUVH}	V_{CC} 电源欠压锁定滞回电压回差	$V_{IN} = 0$ V, $V_{CC} =$ 扫描	-	0.4	-	V

自举电源部分

I_{QBS}	V_{BS} 静态电源电流	$V_{IN} = 0$ V 或 V_{DD}	-	60	130	μA
I_{PBS}	V_{BS} 工作电源电流	$f_{IN} = 20$ kHz (均方根值)	-	500	-	μA
V_{BSUV+}	V_{BS} 电源欠压正向阈值电压	$V_{IN} = 0$ V, $V_{BS} =$ 扫描	7.7	8.8	9.9	V
V_{BSUV-}	V_{BS} 电源欠压负向阈值电压	$V_{IN} = 0$ V, $V_{BS} =$ 扫描	7.3	8.4	9.5	V
V_{BSUVH}	V_{BS} 电源欠压锁定滞回电压回差	$V_{IN} = 0$ V, $V_{BS} =$ 扫描	-	0.4	-	V
I_{LK}	偏置漏电流	$V_B = V_S = 600$ V	-	-	50	μA

输入逻辑部分 (HIN、LIN 和 SD)

V_{IH}	逻辑“1”输入阈值电压	$V_{DD} = 3$ V	2.4	-	-	V
		$V_{DD} = 15$ V	9.5	-	-	V
V_{IL}	逻辑“0”输入阈值电压	$V_{DD} = 3$ V	-	-	0.8	V
		$V_{DD} = 15$ V	-	-	4.5	V
I_{IN+}	逻辑输入高偏置电流	$V_{IN} = V_{DD}$	-	20	40	μA
I_{IN-}	逻辑输入低电平偏置电流	$V_{IN} = 0$ V	-	-	3	μA
R_{IN}	逻辑输入下拉电阻		375	750	-	k Ω

栅极驱动器输出部分

V_{OH}	高电平输出电压 ($V_{BIAS} - V_O$)	空载 ($I_O = 0$ A)	-	-	1.5	V
V_{OL}	低电平输出电压	空载 ($I_O = 0$ A)	-	-	200	mV
I_{O+}	输出高电平、短路脉冲电流 (注 4)	$V_O = 0$ V, $PW \leq 10$ μs	2.5	3.0	-	A
I_{O-}	输出低电平、短路脉冲电流 (注 4)	$V_O = 15$ V, $PW \leq 10$ μs	2.5	3.0	-	A
V_{SS}/COM	$V_{SS}-COM/COM-V_{SS}$ 电压承受		-5.0	-	5.0	V
$-V_S$	IN 信号传播到 HO 时允许的 V_S 引脚负电压		-	-9.8	-7.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(参考译文)

除非另有说明, “电气特性”表格中列出的是所列测试条件下的产品性能参数。如果在不同条件下运行, 产品性能可能与“电气特性”表格中所列性能参数不一致。

4. 这些参数由设计保证。

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动态电气特性 (除非另有说明, V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15.0 V, V_{SS} = COM = 0 V, C_{LOAD} = 1000 pF, T_A = 25°C。)

符号	特性	测试条件	最小值	典型值	最大值	单位
t_{on}	导通传播延迟时间	$V_S = 0$ V	-	130	180	ns
t_{off}	关断传播延迟时间	$V_S = 0$ V	-	150	200	ns
t_{sd}	关闭传播延迟时间 (注 5)		-	130	180	
t_r	导通上升时间		-	25	50	
t_f	关断下降时间		-	20	45	
MT	延迟匹配, HO 和 LO 开启 / 关断		-	-	35	

5. 这些参数由设计保证。

典型特性

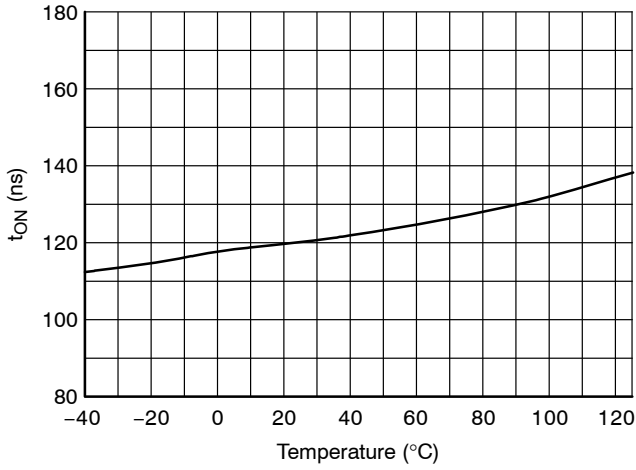


图 6. 导通传播延时与温度的关系

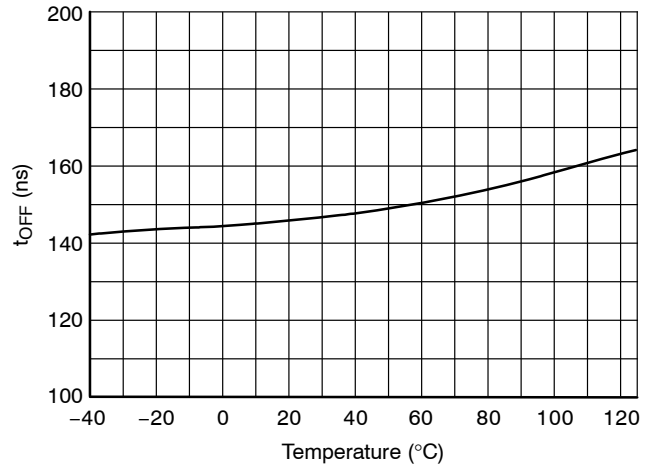


图 7. 关断传播延迟与温度的关系

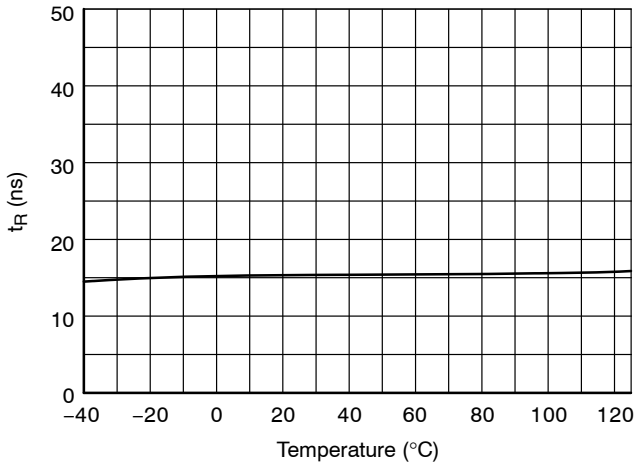


图 8. 导通上升时间与温度的关系

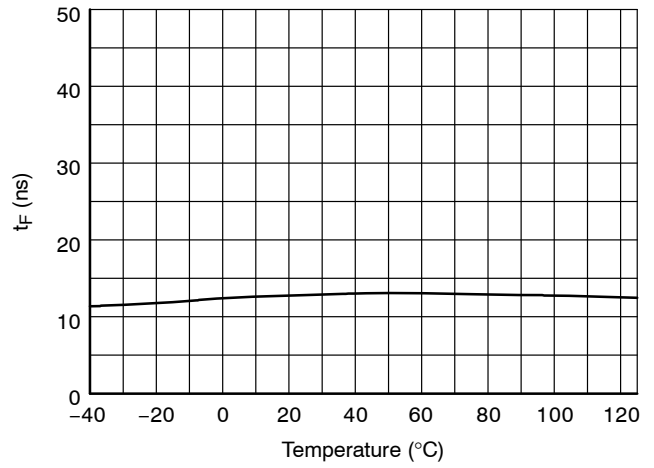


图 9. 关断下降时间与温度的关系

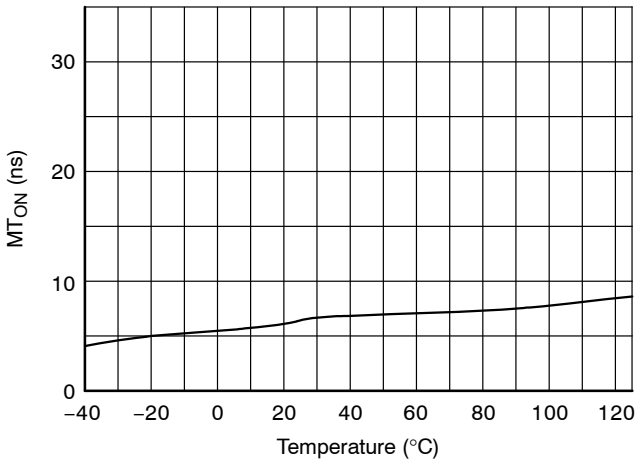


图 10. 开启延迟匹配与温度的关系

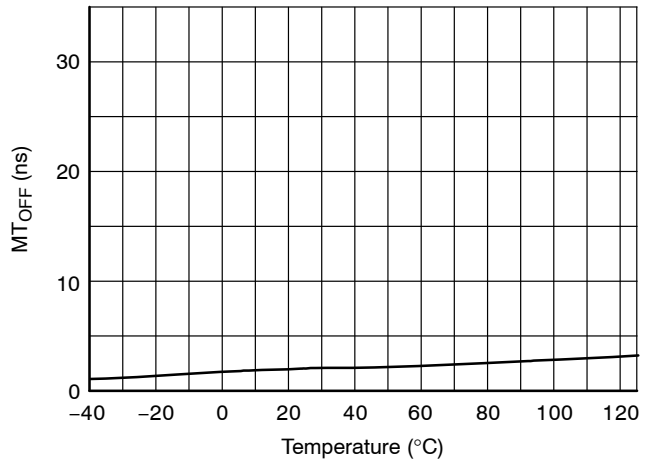


图 11. 关断延迟匹配与温度的关系

典型特性 (续)

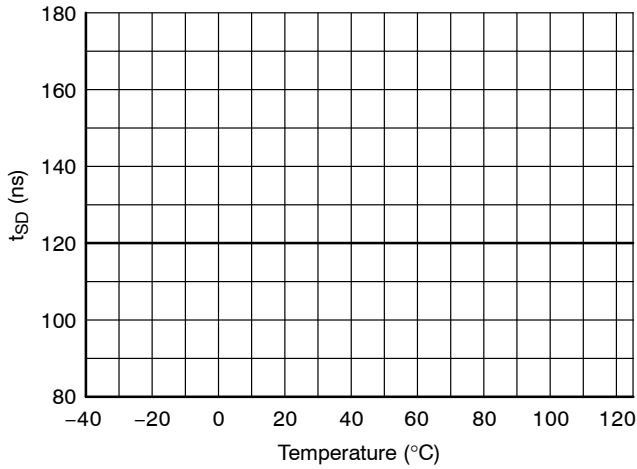


图 12. 关闭传播延迟与温度的关系

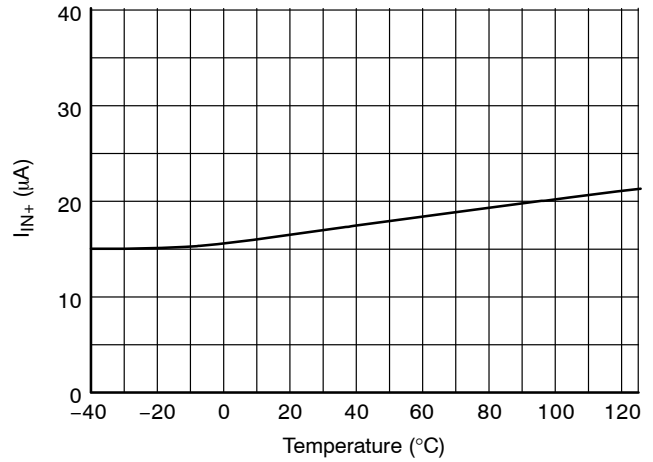


图 13. 逻辑输入高电平偏置电流与温度的关系

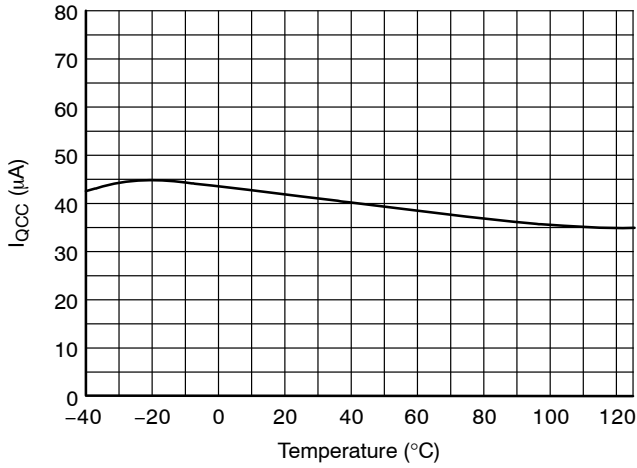


图 14. V_{CC} 静态电源电流与温度的关系

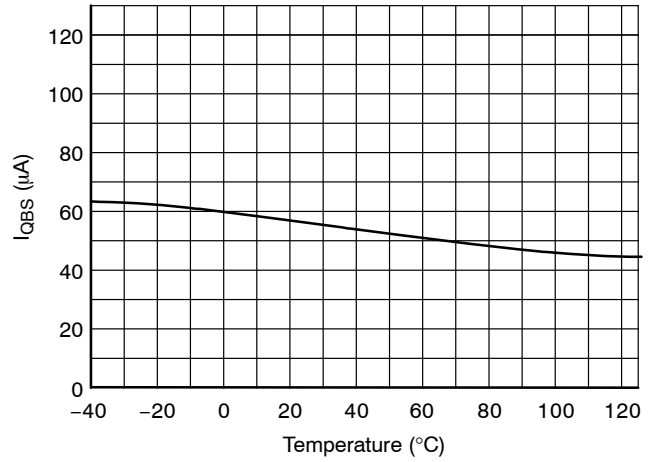


图 15. V_{BS} 静态电源电流与温度的关系

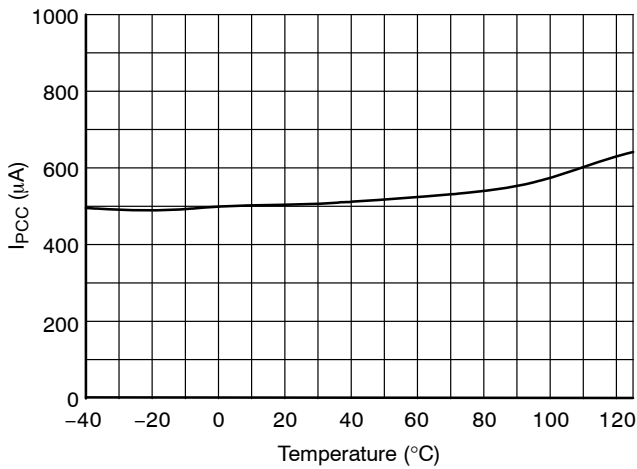


图 16. V_{CC} 工作电源电流与温度的关系

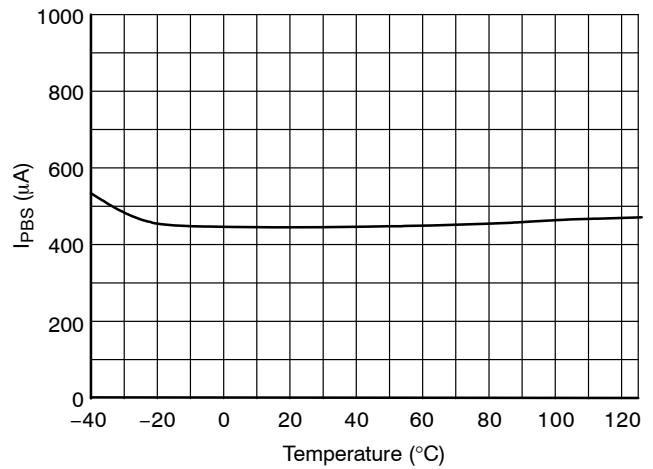


图 17. V_{BS} 工作电源电流与温度的关系

典型特性 (续)

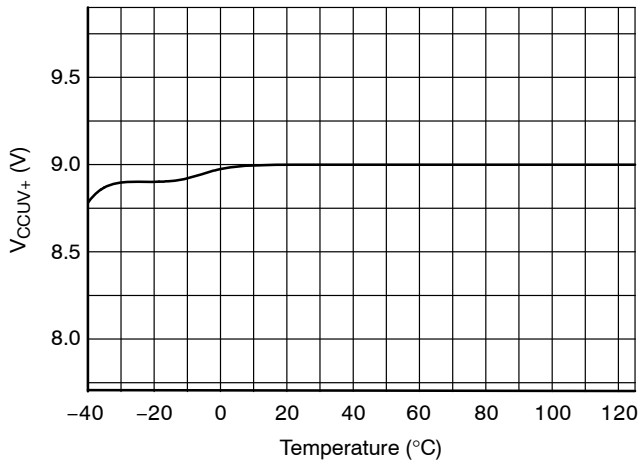


图 18. V_{CC} UVLO+ 与温度的关系

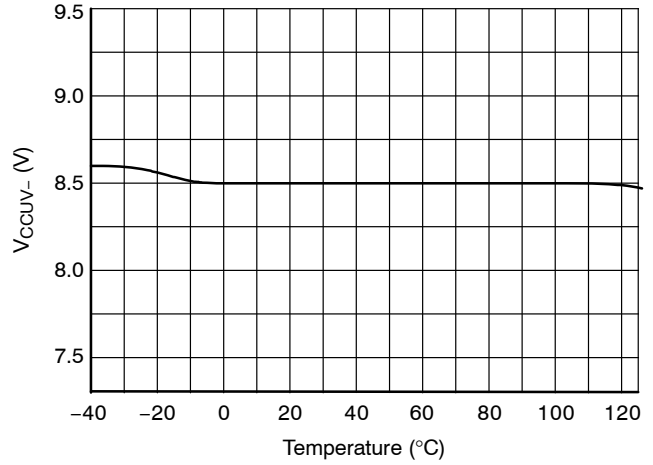


图 19. V_{CC} UVLO- 与温度的关系

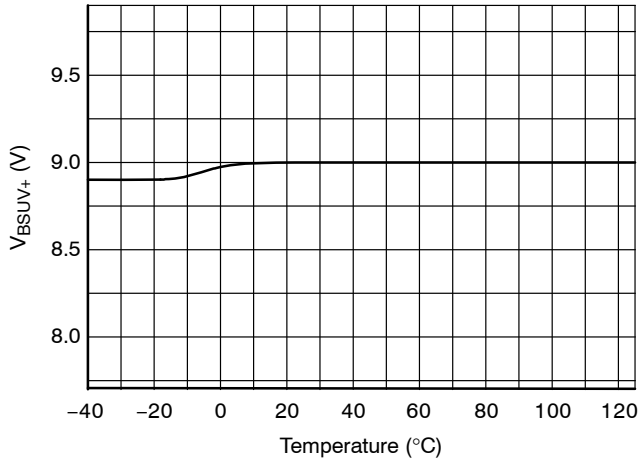


图 20. V_{BS} UVLO+ 与温度的关系

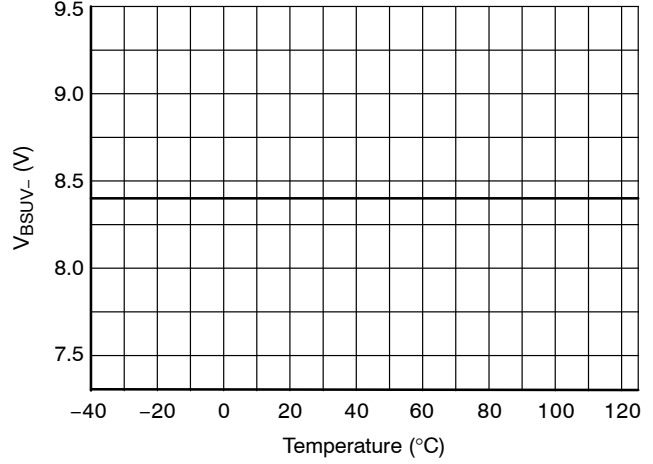


图 21. V_{BS} UVLO- 与温度的关系

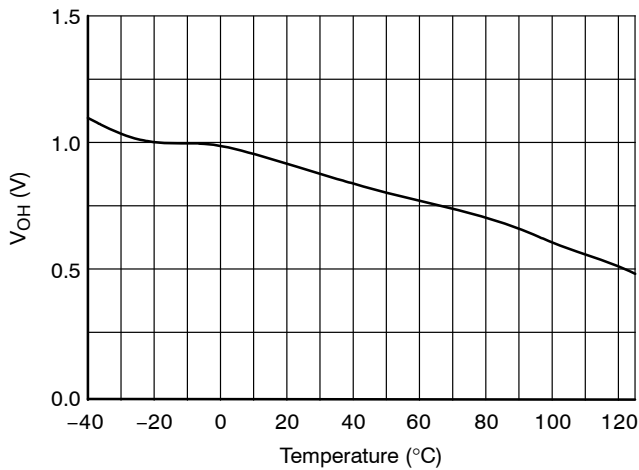


图 22. 高电平输出电压与温度的关系

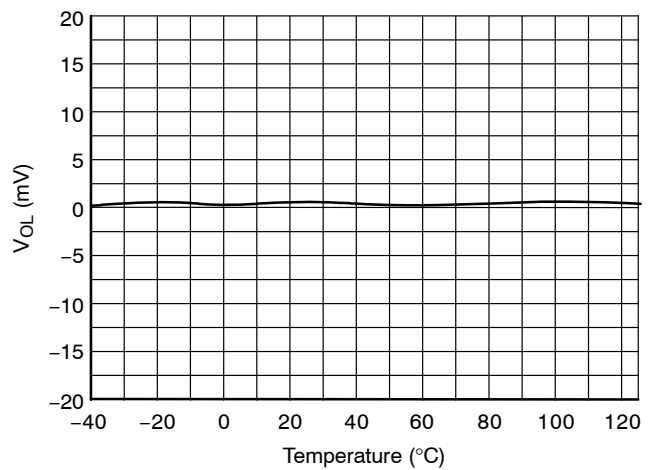


图 23. 低电平输出电压与温度的关系

典型特性 (续)

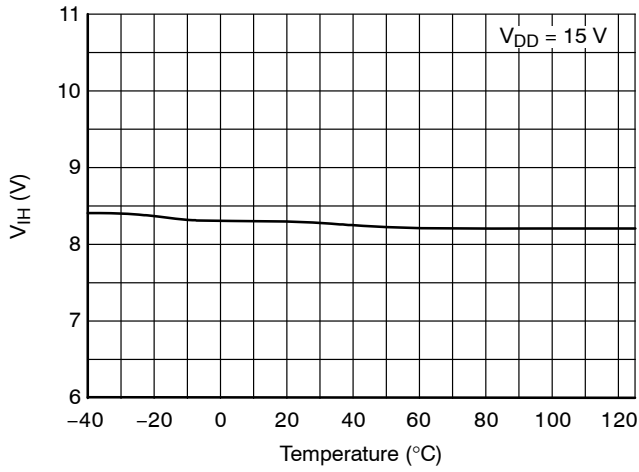


图 24. 逻辑高输入电压与温度的关系

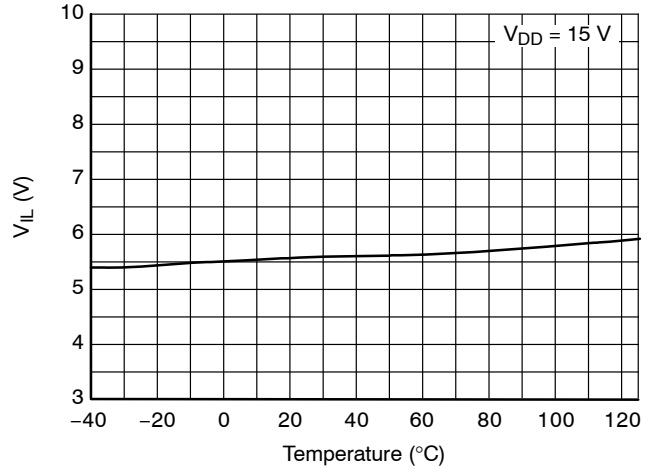


图 25. 逻辑低输入电压与温度的关系

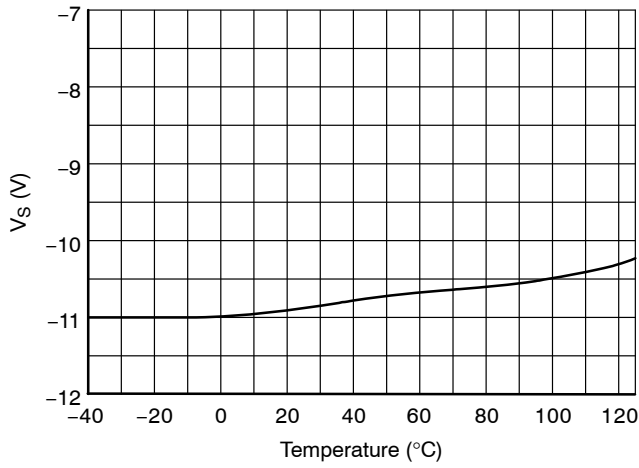


图 26. 允许的负 VS 电压与温度的关系

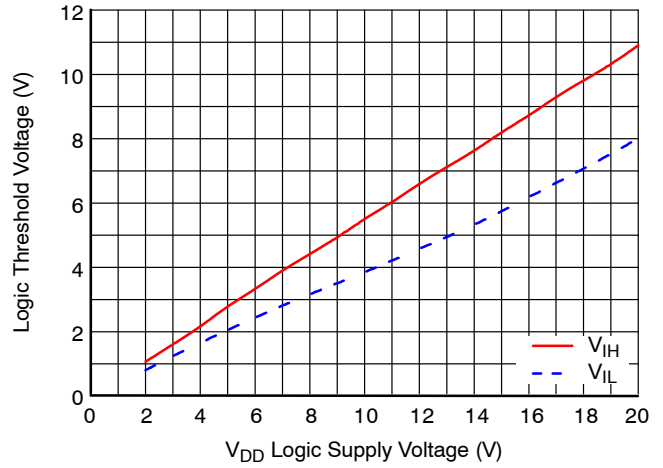


图 27. 输入逻辑 (HIN 和 LIN) 阈值电压与 VDD 电源电压的关系

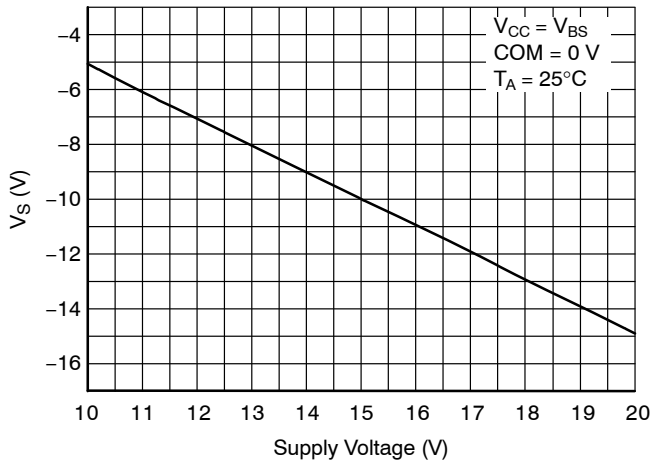


图 28. HIN 信号传播至高侧允许的 VS 负电压与电源电压的关系

FAN7392

开关时间定义

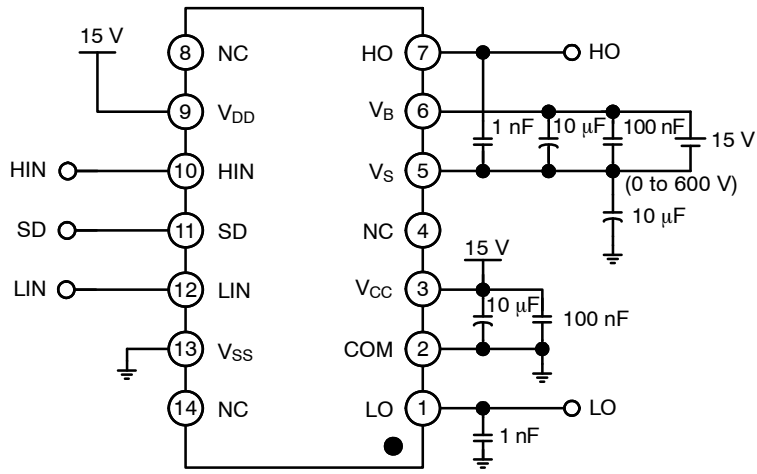


图 29. 开关时间测试电路 (参考14-DIP)

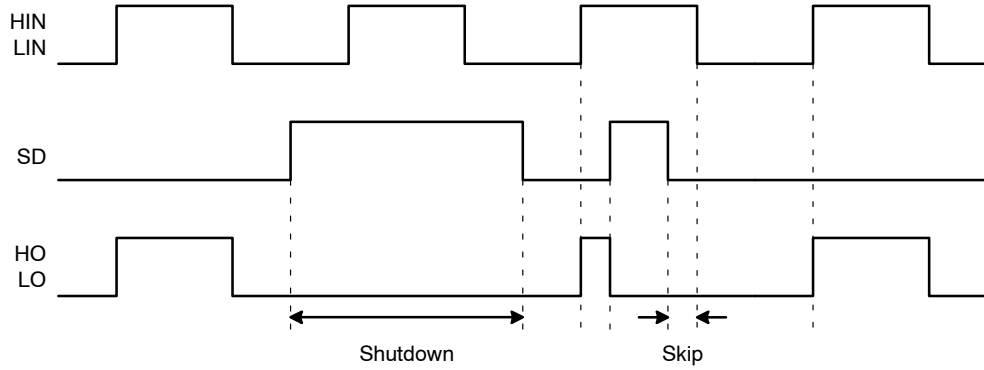


图 30. 输入 / 输出时序图

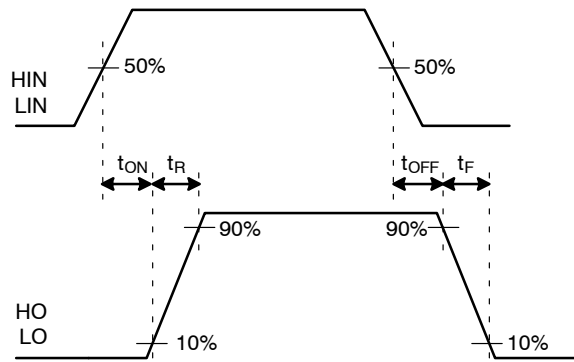


图 31. 开关时间波形定义

开关时间定义 (续)

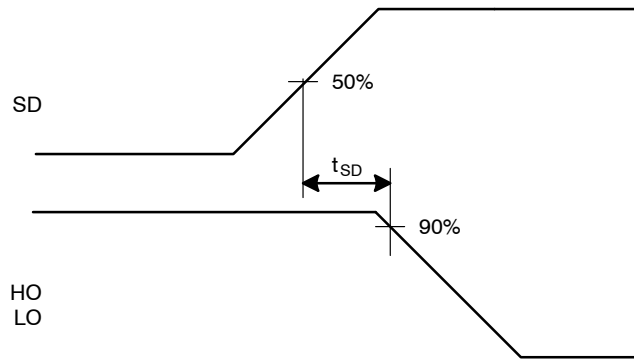


图 32. 关闭波形定义

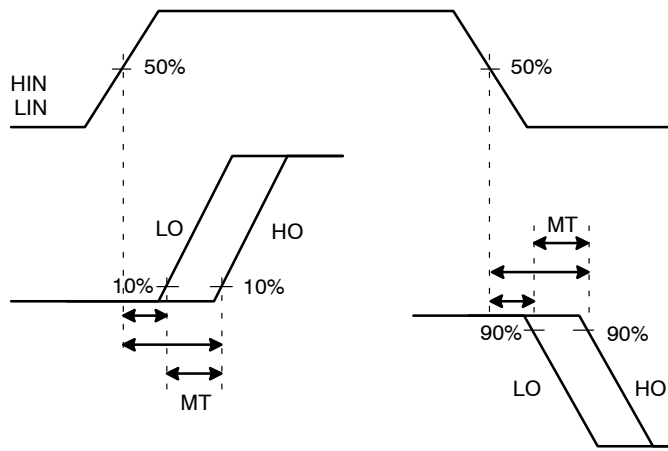


图 33. 开关匹配波形定义

应用信息

瞬变 V_S 负电压

自举式电路具有简单和低成本的优点，但是，它也有一些局限。此电路的最大难题是，在半桥应用中，高侧的开关器件关断时在其发射极存在负电压。

如果高侧开关 $Q1$ 关断，同时负载电流流向电感负载；从高侧开关 $Q1$ 至二极管 $D2$ (与同一逆变器桥臂的低侧开关并联) 出现电流转移。然后，负电压出现在高侧开关器件的发射极，在续流二极管开始箝位前，负载电流突然流向低侧续流二极管 $D2$ ，如图 34 所示。

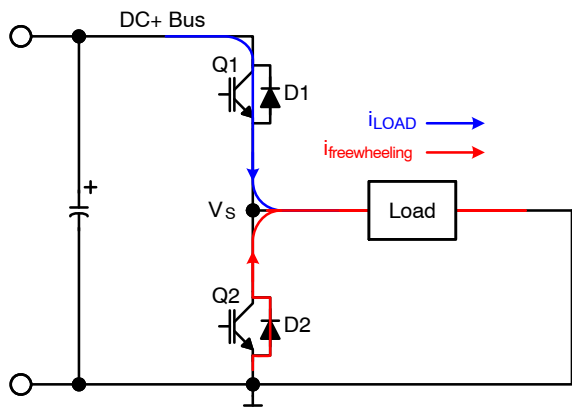


图 34. 半桥应用电

此负电压给栅极驱动器输出时带来麻烦。很可能产生自举电容过压的情况，输入信号丢失以及闭锁问题，因为它直接影响栅极驱动器的电源 V_S 引脚，如图 35 所示。该下冲电压称为“瞬变 V_S 负电压”。

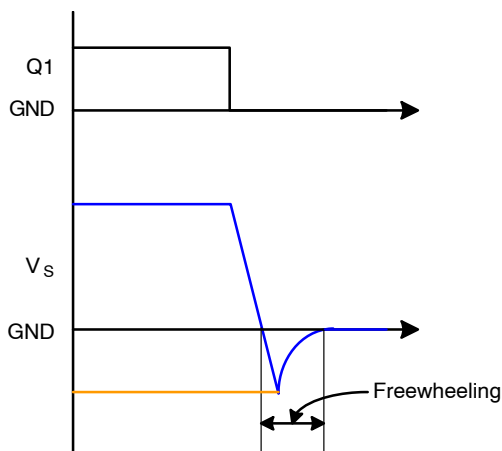


图 35. $Q1$ 和 $Q4$ 导通

图 36 和图 37 显示高侧开关 $Q1$ 和低侧续流二极管 $D3$ (同一逆变桥臂) 之间的负载电流换流。逆变电路中从芯片引脚绑定到 PCB 走线的寄生电感对于每个 IGBT 的就是 L_C 和 L_E 。当高侧开关 $Q1$ 和低侧开关 $Q4$ 导通后， V_{S1} 节点电压稍低于 $DC+$ 电压，压差与电路的功率开关以及寄生电感有关 (负载电流从 $Q1$ 和 $Q4$ 流出，如图 36 所示)。若高侧开关 $Q1$ 关断且 $Q4$ 保持导通状态，则负载电流流入低侧续流二极管 $D3$ (感性负载连接 $VS1$ ，如图 37 所示)。电流从地 (连接栅极驱动器的 COM 引脚) 流入负载，高侧开关器件的发射极为负电压。

这种情况下，栅极驱动器的 COM 引脚电位高于 V_S 引脚，因为续流二极管 $D3$ 有压降，寄生元件 L_{C3} 、 L_{E3} 也有压降。

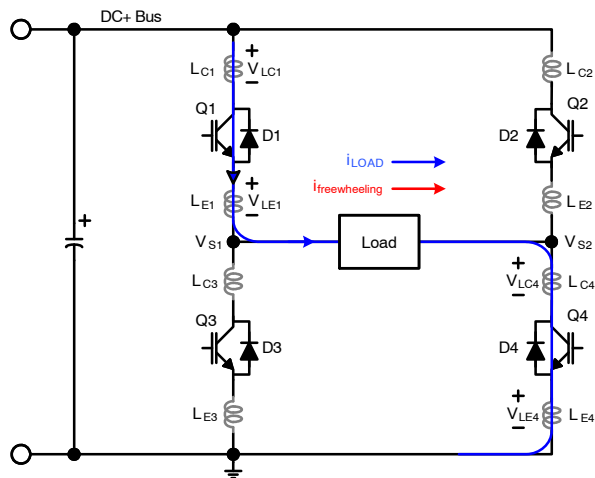


图 36. $Q1$ 和 $Q4$ 导通

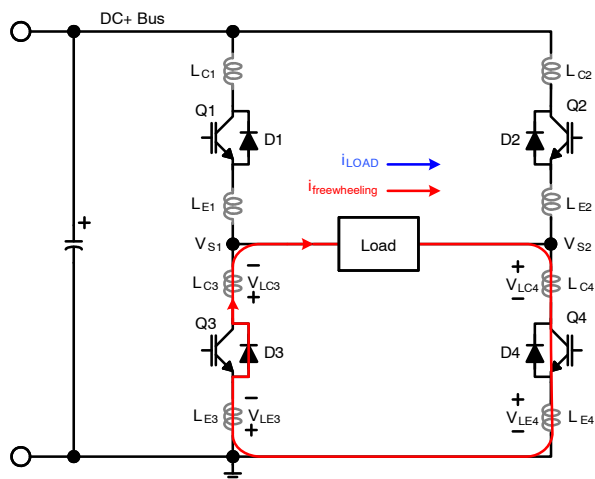


图 37. $Q1$ 关断和 $D3$ 导通

FAN7392 的瞬态 V_S 负电压曲线如图 38 所示。

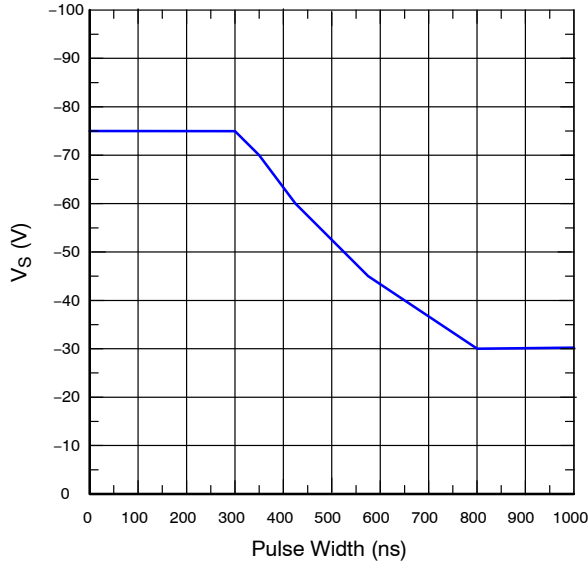


图 38. 瞬态 V_S 负电压特

虽然FAN7392 已表现出可处理这些瞬态 V_S 负电压条件的能力，仍然强烈建议电路设计人员谨慎进行PCB 布局，尽量限制负 V_S ，最大程度降低寄生元件的数值以及所用元器件的数量。负 V_S 电压幅度与寄生电感以及开关器件的关断速度 (di/dt) 成比例。

一般准则

印刷电路板布局

最大程度降低元件寄生特性的布局建议如下：

- 开关之间的走线没有回路或偏差。
- 避免互连链路。它会显著增加电感。
- 降低封装体距离 PCB 板的高度，以减少引脚电感效应。

- 考虑所有功率开关的配合放置，以减少走线长度。
- 若要尽可能减少噪声耦合，接地层不应放置在高侧浮动侧的下方，或位于高侧浮动侧附近。
- 若要减少EM耦合并改善功率开关的导通 / 关断性能，必须尽可能缩短栅极驱动环路。

元器件放置

元器件的位置与选型建议如下：

- 在 V_{DD} 和 V_{SS} 引脚之间放置一个旁路电容。1 μF 电容适用于大部分应用。该元件应尽可能靠近引脚放置，以便降低寄生元素。
- V_{CC} 和 COM 之间的旁路电容同时为低侧驱动器和自举电容的再充电供电。建议该电容值至少是自举电容的十倍以上。
- 在量化自举电阻和初次自举充电时的电流时，必须考虑自举电阻 R_{BOOT} 。若需要将电阻与自举二极管串联连接，请验证 V_B 不低于 COM (地)。建议使用典型 5~10 Ω ，可增加 V_{BS} 时间常数。如果自举电阻和二极管的压降过高，或电路拓扑不允许足够的充电时间，则可以使用快恢复或超快恢复二极管。
- 自举电容 C_{BOOT} 使用一个低ESR电容，比如陶瓷电容。

强烈建议元器件如下放置：

- 与浮动电压引脚 (V_B 和 V_S) 相连的元器件放置在器件以及 FAN7392 的对应高压部分附近。该封装中的 NC (未连接) 引脚使高压引脚和低压引脚之间的距离最大化 (见图 5)。
- 旁路电容和栅极电阻的布局和布线应尽可能靠近栅极驱动IC。
- 自举二极管 D_{BOOT} 应尽量靠近自举电容 C_{BOOT} 放置。
- 自举二极管必须使用较低的正向压降，为了快速恢复，开关时间必须尽可能短，如超快恢复二极管。

ORDERING INFORMATION

器件编号	工作 温度范围	封装	包装方法 [†]
FAN7392N	-40°C 至 125°C	PDIP-14 14-PDIP (Pb-Free)	1500 / 塑料管
FAN7392MX		SOIC-16 16-SOP (Pb-Free)	1000 / 卷带和卷盘

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

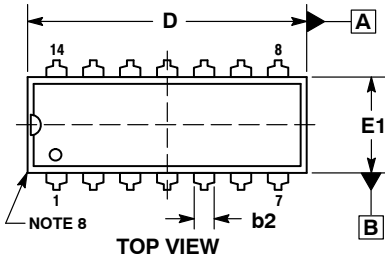
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

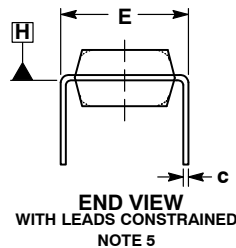


SCALE 1:1



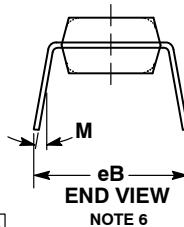
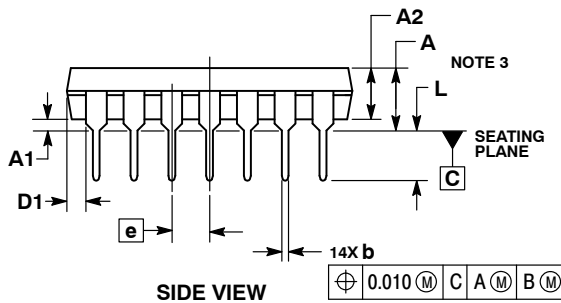
PDIP-14
CASE 646-06
ISSUE S

DATE 22 APR 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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CASE 646-06
ISSUE S

DATE 22 APR 2015

STYLE 1:
 PIN 1. COLLECTOR
 2. BASE
 3. EMITTER
 4. NO
CONNECTION
 5. EMITTER
 6. BASE
 7. COLLECTOR
 8. COLLECTOR
 9. BASE
 10. EMITTER
 11. NO
CONNECTION
 12. EMITTER
 13. BASE
 14. COLLECTOR

STYLE 2:
 CANCELLED

STYLE 3:
 CANCELLED

STYLE 4:
 PIN 1. DRAIN
 2. SOURCE
 3. GATE
 4. NO
CONNECTION
 5. GATE
 6. SOURCE
 7. DRAIN
 8. DRAIN
 9. SOURCE
 10. GATE
 11. NO
CONNECTION
 12. GATE
 13. SOURCE
 14. DRAIN

STYLE 5:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. NO CONNECTION
 5. SOURCE
 6. DRAIN
 7. GATE
 8. GATE
 9. DRAIN
 10. SOURCE
 11. NO CONNECTION
 12. SOURCE
 13. DRAIN
 14. GATE

STYLE 6:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 7:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON
 CATHODE

STYLE 8:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 9:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

STYLE 10:
 PIN 1. COMMON
 CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON
 CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 11:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 12:
 PIN 1. COMMON CATHODE
 2. COMMON ANODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. COMMON ANODE
 7. COMMON CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

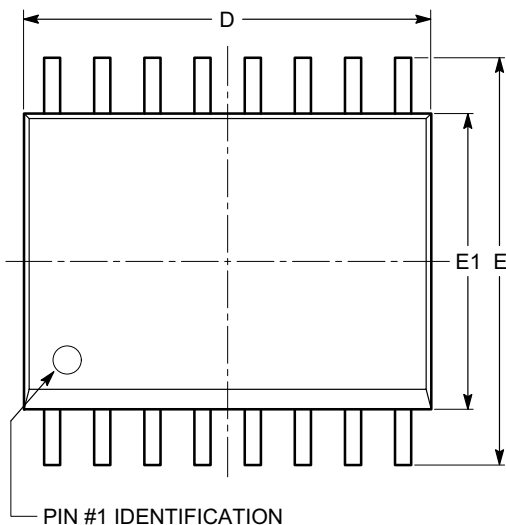
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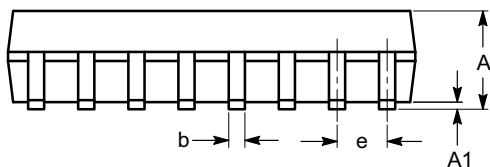
SOIC-16, 300 mils
CASE 751BH-01
ISSUE A

DATE 18 MAR 2009

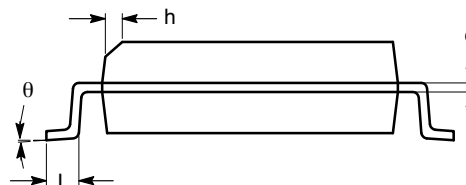


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
b	0.33	0.41	0.51
c	0.18	0.23	0.28
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e	1.27 BSC		
h	0.25		0.75
L	0.38	0.81	1.27
θ	0°		8°



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

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