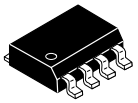
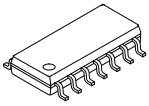
高侧和低侧栅极驱动器

FAN7382



SOIC8
CASE 751EG



SOIC14 N
CASE 751ER

FAN7382 为单片高侧和低侧栅极驱动 IC，用来驱动工作电压高达 +600 V 的 MOSFET 和 IGBT。安森美高压工艺和共模噪声消除技术可使高端驱动器在高 dv/dt 噪声环境下稳定运行。先进的电平转换电路允许高侧驱动器的工作偏置电压达 V_S = −9.8 V (典型值)，当 V_{BS} = 15 V 时. 输入逻辑电平与标准 TTL 系列逻辑栅极兼容。两个通道的欠压闭锁锁定电路在 V_{CC} 或 V_{BS} 低于指定阈值电压时，防止出现故障。输出驱动器通常提供 350 mA/650 mA 的源电流/灌电流，适合萤光灯镇流器、PDP 扫描驱动器和电机控制等。

特性

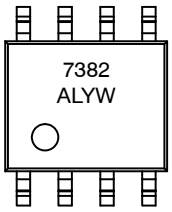
- 浮动通道专为高达 +600 V 的自举运行而设计
- 两个通道的源/ 灌电流驱动能力典型值为 350 mA/650 mA
- 共模 dv/dt 噪声消除电路
- 在 V_{CC} = V_{BS} = 15 V 时信号传输过程中，扩展允许负 V_S 摆幅低达 −9.8 V
- V_{CC} 和 V_{BS} 供电范围从 10 V 至 20 V
- 双通道的欠压锁定功能
- 兼容 TTL 的输入逻辑阈值电平
- 匹配传输延迟低于 50 ns
- 输出信号与输入信号同相位
- These are Pb−Free Devices

应用

- PDP 扫描驱动器
- 荧光灯镇流器
- SMPS
- 电动机驱动

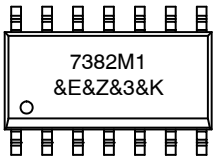
MARKING DIAGRAMS

SOIC8



7382 = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

SOIC14 N



7382M1 = Device Code
&E = Designates Space
&Z = Assembly Location
&3 = 3−Digit Date Code
&K = 2−Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

典型应用电路

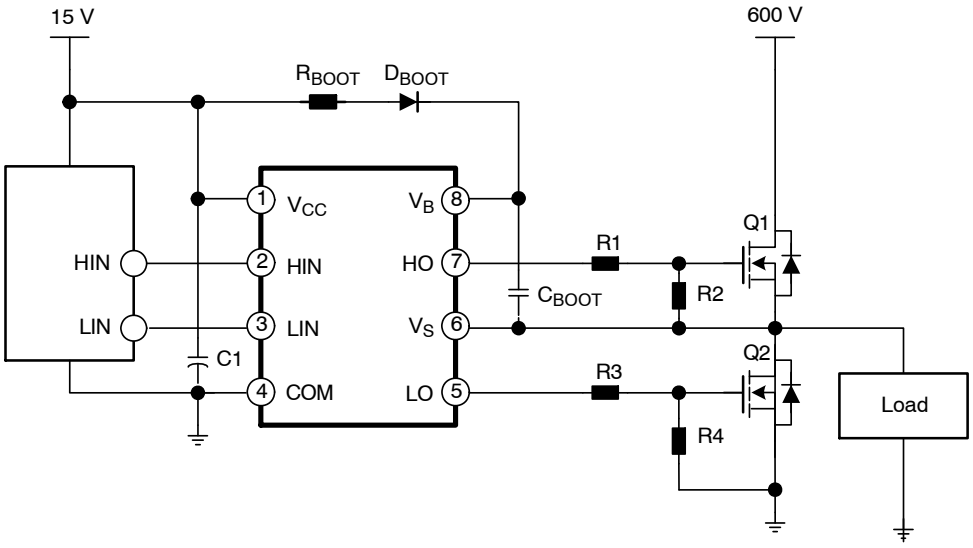


图 1. 半桥应用电路

内部框图

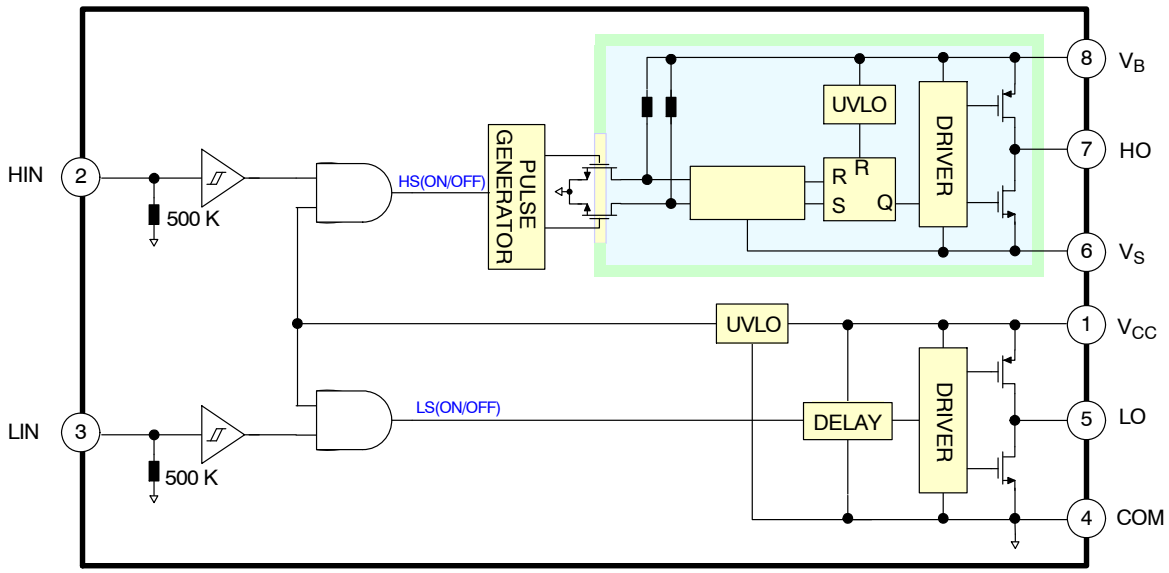


图 2. 功能框图

引脚配置

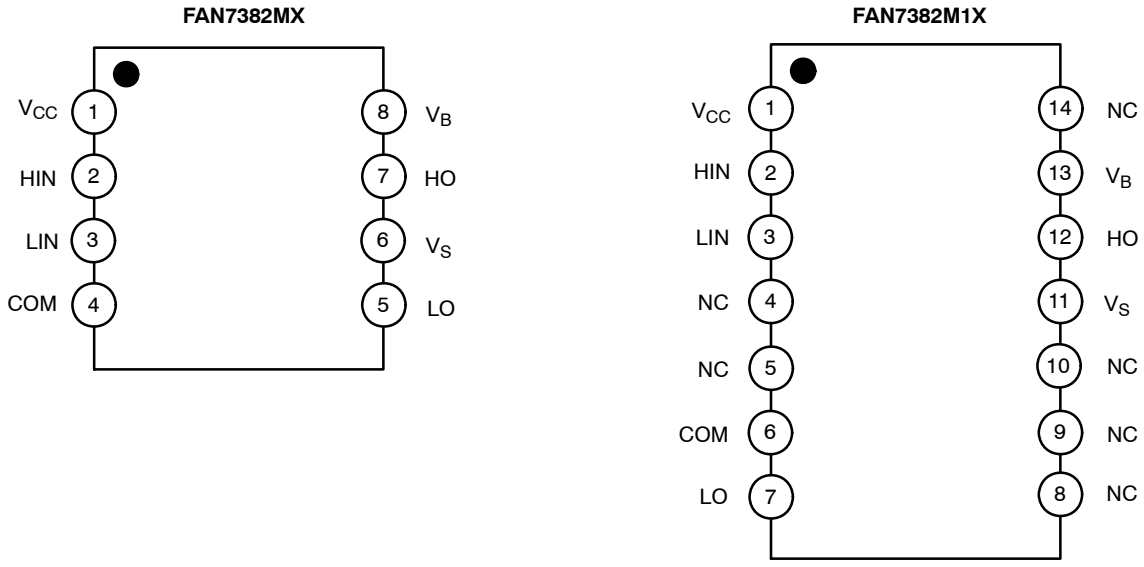


图 3. 引脚配置（俯视图）

引脚定义

名称	说明
V_{CC}	低侧电源电压
HIN	高侧栅极驱动器输出的逻辑输入
LIN	低侧栅极驱动器输出的逻辑输入
COM	逻辑地和低侧驱动器返回
LO	低侧栅极输出
V_S	高侧浮动电源电压返回
HO	高侧驱动输出
V_B	高侧浮动电源

绝对最大额定值

特性	符号	最小值	最大值	单位
高侧偏置电压	V_S	V_B – 25	V_B + 0.3	V
高侧浮动电源电压	V_B	–0.3	625	
高侧浮动输出电压 HO	V_{HO}	V_S – 0.3	V_B + 0.3	
低侧和固定逻辑电源电压	V_{CC}	–0.3	25	
低侧输出电压 LO	V_{LO}	–0.3	V_{CC} + 0.3	
逻辑输入电压 (HIN、LIN)	V_{IN}	–0.3	V_{CC} + 0.3	
逻辑地	COM	V_{CC} – 25	V_{CC} + 0.3	
允许的偏置电压变化速率	dV_S/dt		50	V/ns
功耗	P_D (说明 1, 2, 3)	SOIC8	0.625	W
		SOIC14 N	1.0	
结温	T_J		150	°C
存储温度	T_{STG}		150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
(参考译文)
如果电压超过最大额定值表中列出的值范围，器件可能会损坏。如果超过任何这些限值，将无法保证器件功能，可能会导致器件损坏，影响可靠性。

1. 安装到 76.2 x 114.3 x 1.6 mm PCB 板 (FR–4 环氧玻璃材料)。
2. 参考以下标准:
   JESD51–2: 集成电路热测试方法环境条件– 自然对流
   JESD51–3: 含铅表面贴装封装的低有效导热系数测试板
3. 在任何情况下，都不要超过 P_D。

热性能

特性	符号	最小值	最大值	单位
结至环境热阻	θ_{JA}	SOIC8	200	°C/W
		SOIC14 N	110	

推荐工作额定值

参数	符号	最小值	最大值	单位
高侧浮动电源电压	V_B	V_S + 10	V_S + 20	V
高侧浮动电源偏置电压	V_S	6 – V_{CC}	600	V
高侧 (HO) 输出电压	V_{HO}	V_S	V_B	V
低侧 (LO) 输出电压	V_{LO}	COM	V_{CC}	V
逻辑输入电压 (HIN, LIN)	V_{IN}	COM	V_{CC}	V
低侧电源电压	V_{CC}	10	20	V
环境温度	T_A	–40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
(参考译文)
高于推荐工作范围表格中所列电压时，不保证能够正常运行。长时间在推荐工作范围表格中规定范围以外的电压下运行，可能会影响器件的可靠性。

电气特性

除非另有说明，V_{BIAS} (V_{CC}, V_{BS}) = 15.0 V, T_A = 25°C。V_{IN} 和 I_{IN} 参数以 COM 为参考点。V_O 和 I_O 参数以 V_S 和 COM 为参考点，适用于相应的输出 HO 和 LO。

特性	测试条件	符号	最小值	典型值	最大值	单位
V_{CC} 和 V_{BS} 电源欠压正向阈值		V_{CCUV+} V_{BSUV+}	8.2	9.2	10.0	V
V_{CC} 和 V_{BS} 电源欠压负向阈值		V_{CCUV-} V_{BSUV-}	7.6	8.7	9.6	V
V_{CC} 电源欠压锁定滞回电压回差		V_{CCUVH} V_{BSUVH}		0.6		V
偏置电源漏电流	V_B = V_S = 600 V	I_{LK}			50	μA
V_{BS} 静态电源电流	V_{IN} = 0 V 或 5 V	I_{QBS}		45	120	μA
V_{CC} 静态电源电流	V_{IN} = 0 V 或 5 V	I_{QCC}		70	180	μA
V_{BS} 工作电源电流	f_{IN} = 20 kHz, rms 值	I_{PBS}			600	μA
V_{CC} 工作电源电流	f_{IN} = 20 kHz, rms 值	I_{PCC}			600	μA
逻辑 “1” 输入电压		V_{IH}	2.9			V
逻辑 “0” 输入电压		V_{IL}			0.8	V
高电平输出电压, V_{BIAS} − V_O	I_O = 20 mA	V_{OH}			1.0	V
低电平输出电压, V_O		V_{OL}			0.6	V
逻辑 “1” 输入偏置电流	V_{IN} = 5 V	I_{IN+}		10	20	μA
逻辑 “0” 输入偏置电流	V_{IN} = 0 V	I_{IN-}		1.0	2.0	μA
输出高电平短路脉冲电流	V_O = 0 V, V_{IN} = 5 V with PW < 10 μs	I_{O+}	250	350		mA
输出低电平短路脉冲电流	V_O = 15 V, V_{IN} = 0 V with PW < 10 μs	I_{O-}	500	650		mA
IN 信号传播到 HO 时允许的 V_S 引脚负电压		V_S		−9.8	−7.0	V

动态电气特性

除非另有说明, V_{BIAS} (V_{CC}, V_{BS}) = 15.0 V, V_S = COM, C_L = 1000 pF and, T_A = 25°C。

特性	测试条件	符号	最小值	典型值	最大值	单位
导通传输延时	V_S = 0 V	t_{on}	100	170	300	ns
关断传输延时	V_S = 0 V 或 600 V (说明 4)	t_{off}	100	200	300	ns
导通上升时间		t_r	20	60	140	ns
关断下降时间		t_f		30	80	ns
延时匹配, HS 与 LS 导通 / 关断		MT			50	ns

4. 该参数由设计保证。

典型特性

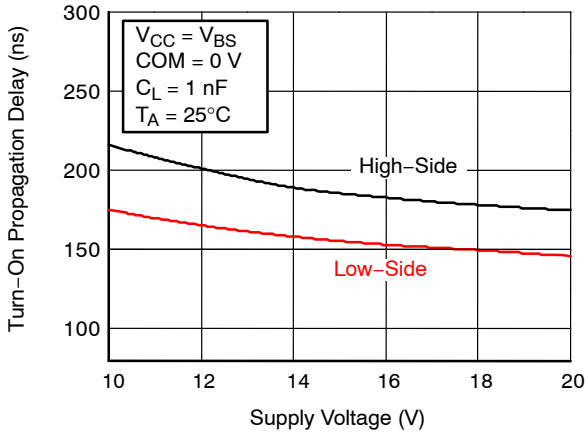


图 4. 导通传播延时与电源电压的关系

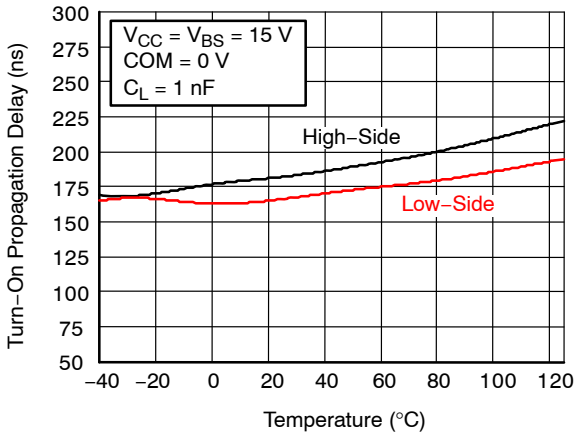


图 5. 导通传播延时与温度的关系

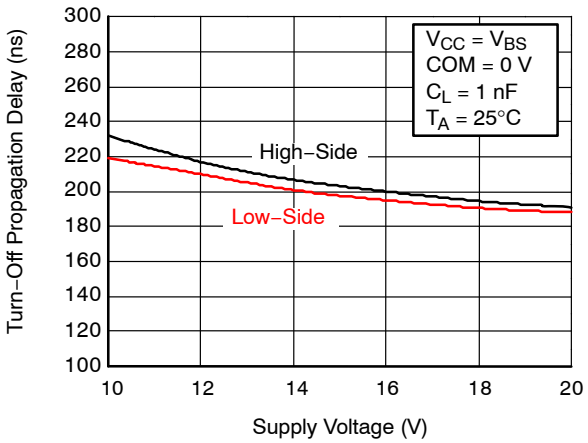


图 6. 关断传播延时与电源电压的关系

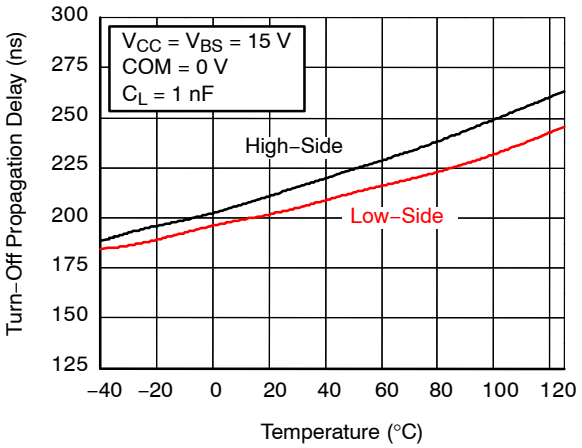


图 7. 关断传播延时与温度的关系

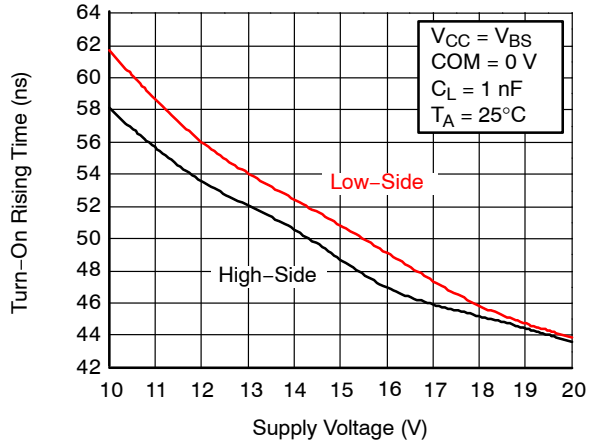


图 8. 导通上升时间与电源电压的关系

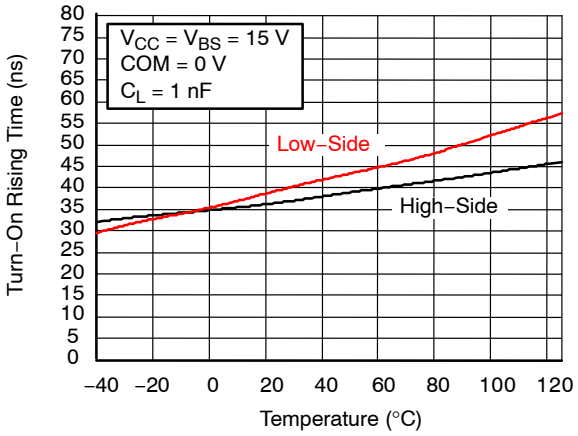


图 9. 导通上升时间与温度的关系

典型特性 (续)

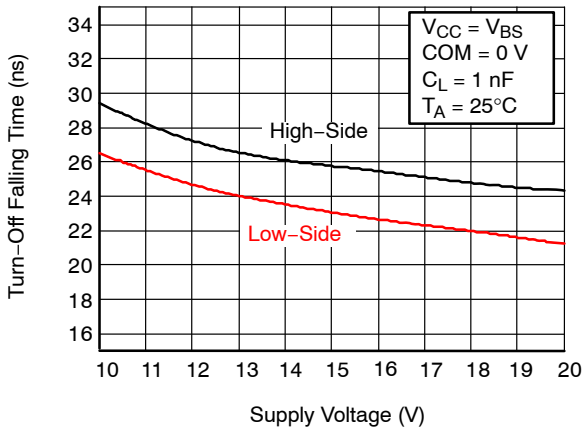


图 10. 关断下降时间与电源电压的关系

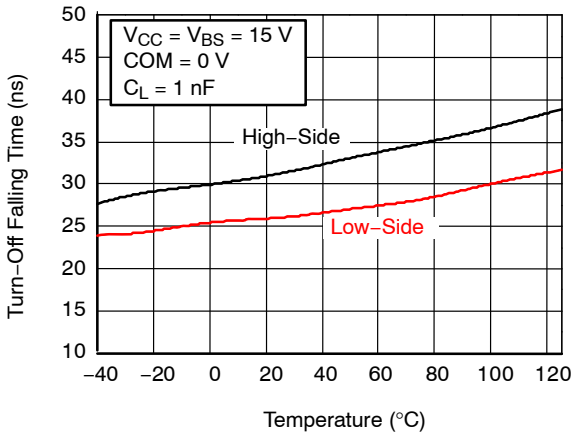


图 11. 关断下降时间与温度的关系

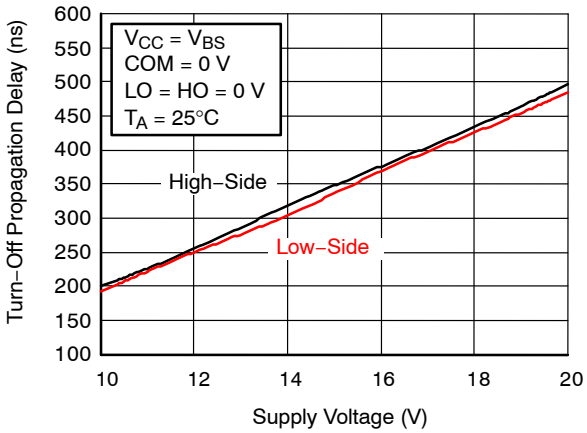


图 12. 输出源电流与电源电压的关系

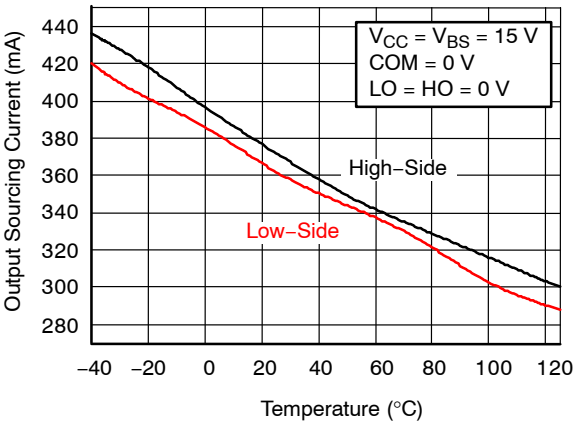


图 13. 输出源电流与温度的关系

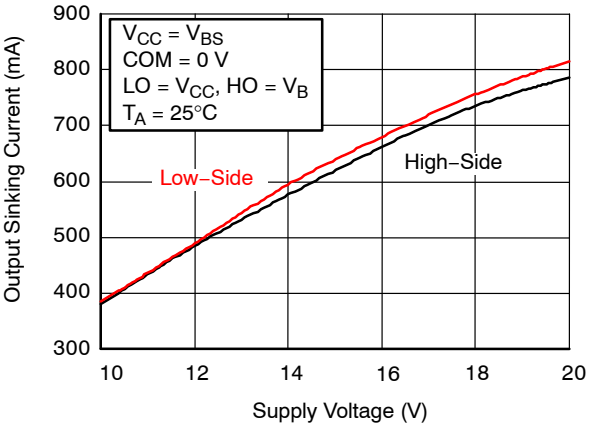


图 14. 输出灌电流与电源电压的关系

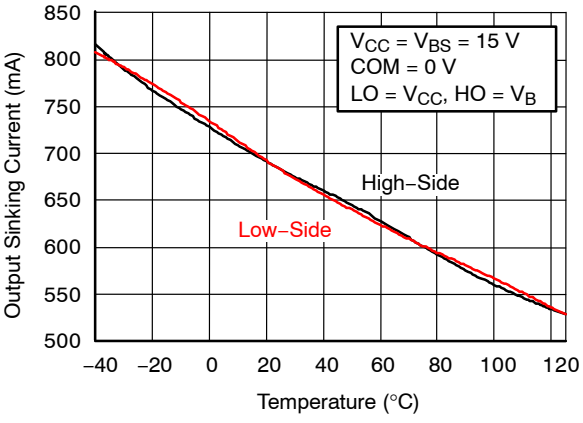


图 15. 输出灌电流与温度的关系

典型特性 (续)

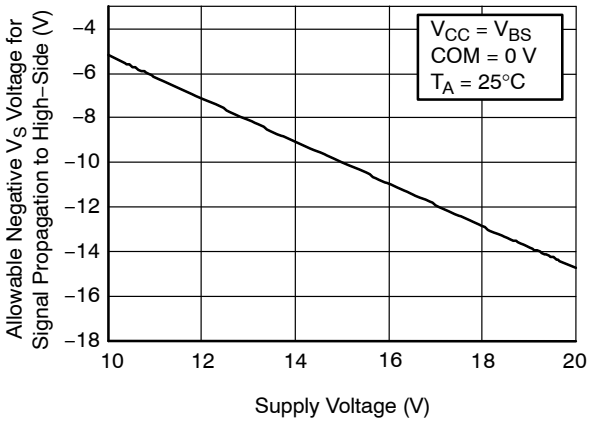


图 16. 信号传播到高侧时允许的 V_S 负电压与电源电压的关系

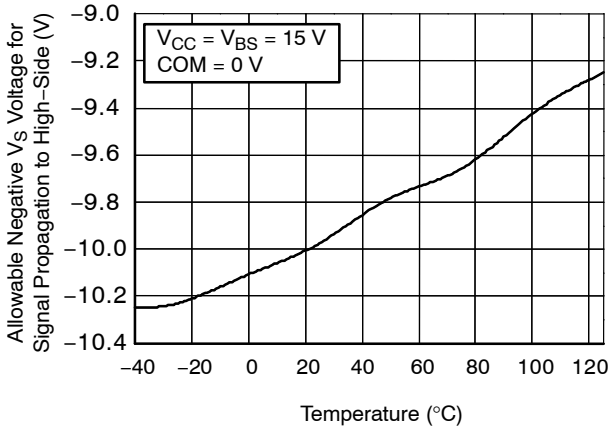


图 17. 信号传播到高侧时允许的 V_S 负电压与温度的关系

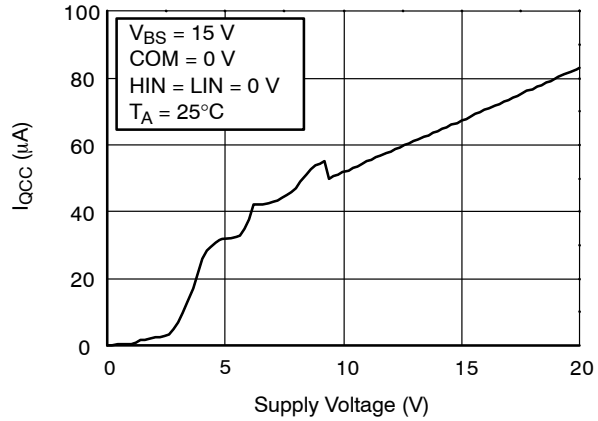


图 18. I_{QCC} 与电源电压的关系

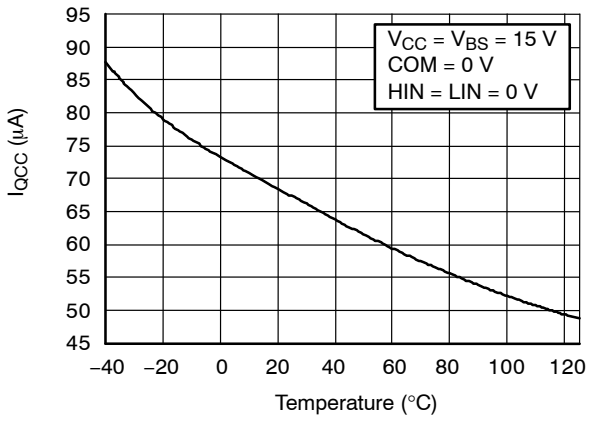


图 19. I_{QCC} 与温度的关系

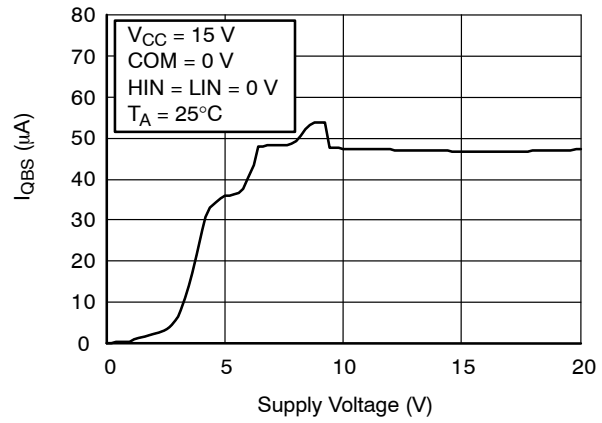


图 20. I_{QBS} 与电源电压的关系

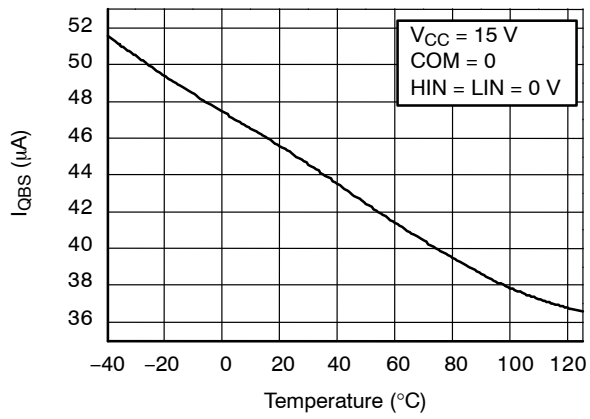


图 21. I_{QBS} 与温度的关系

典型特性 (续)

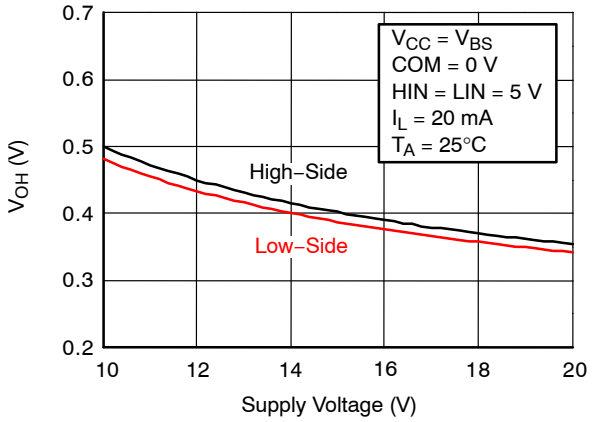


图 22. 高电平输出电压与电源电压的关系

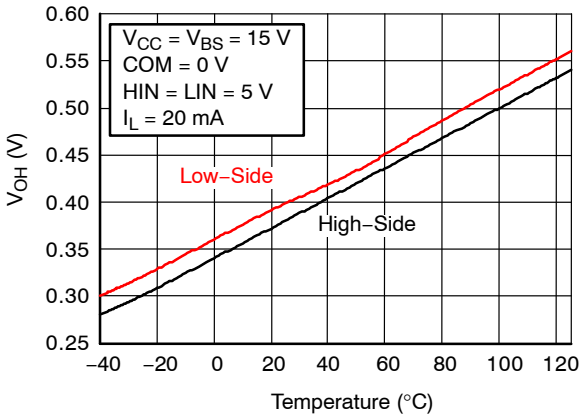


图 23. 高电平输出电压与温度的关系

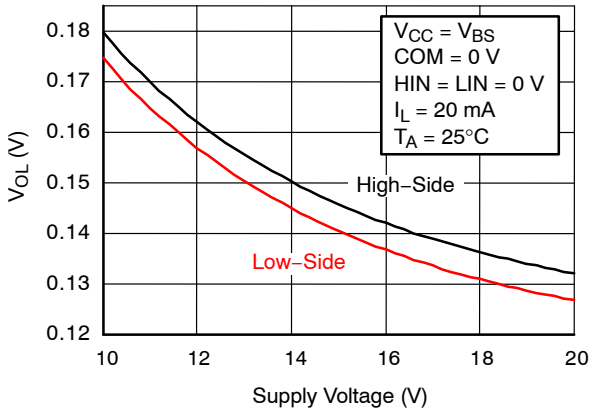


图 24. 低电平输出电压与电源电压的关系

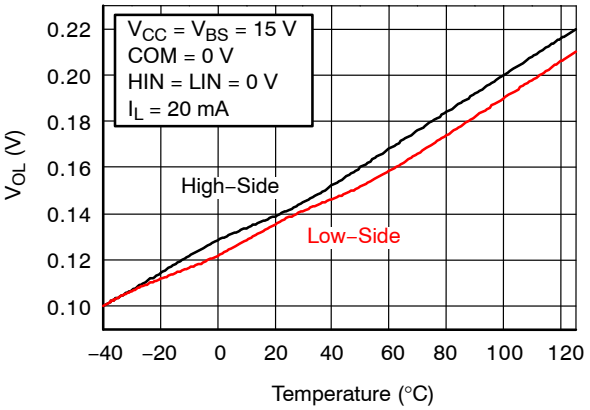


图 25. 低电平输出电压与温度的关系

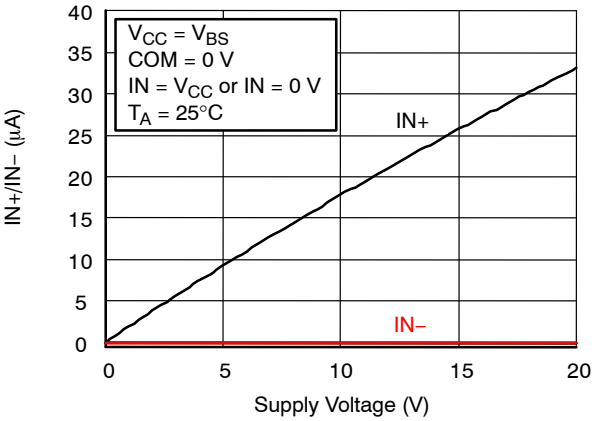


图 26. 输入偏置电流与电源电压的关系

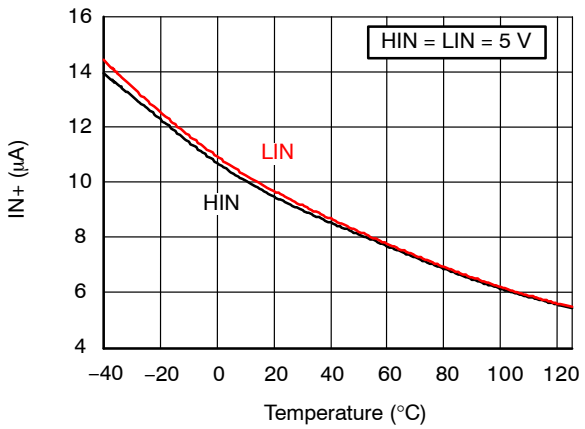


图 27. 输入偏置电流与温度的关系

典型特性 (续)

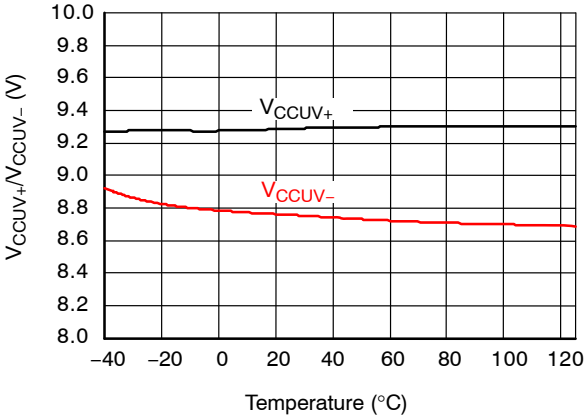


图 28. V_{CC} 欠压锁定阀值电压与温度的关系

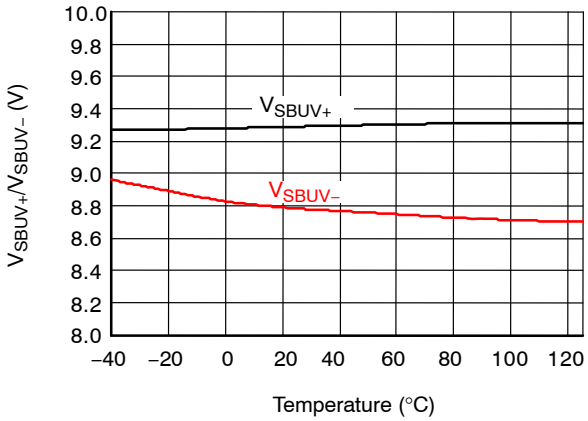


图 29. V_{BS} 欠压锁定阀值电压与温度的关系

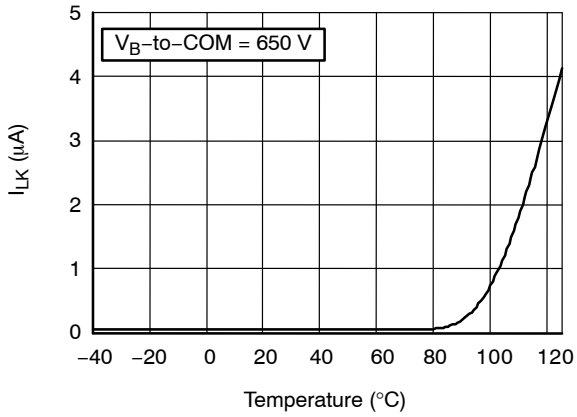


图 30. V_B 至 COM 漏电流与温度的关系

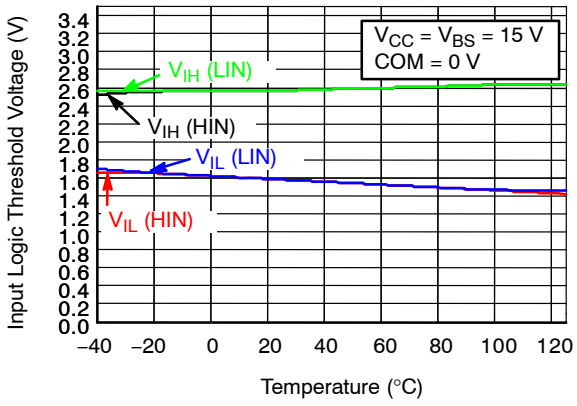


图 31. 输入逻辑阀值电压与温度的关系

典型特性 (续)

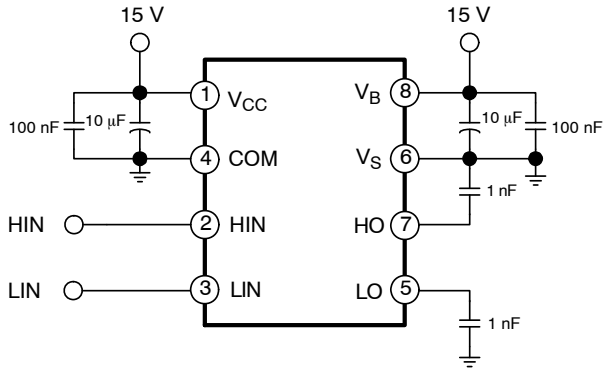


图 32. 开关时间测试电路

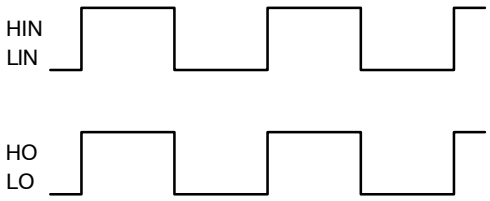


图 33. 输入 / 输出时序图

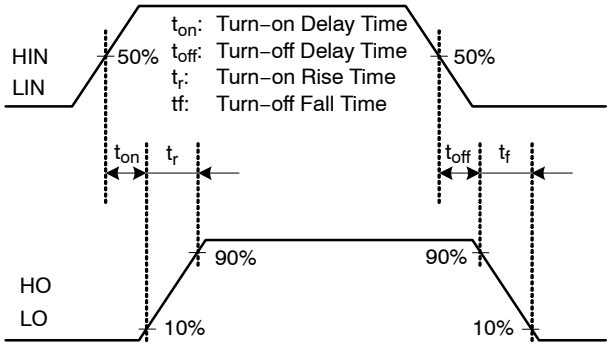


图 34. 开关时间波形定义

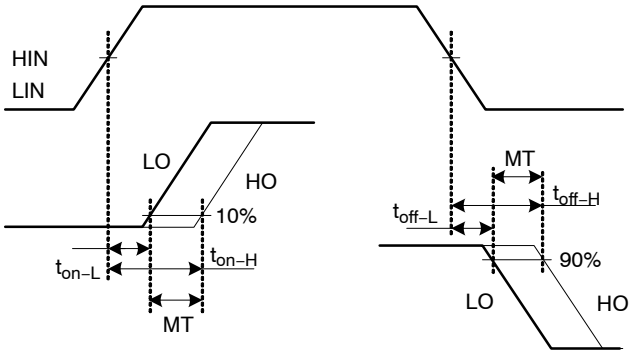


图 35. 延时匹配波形定义

订购信息

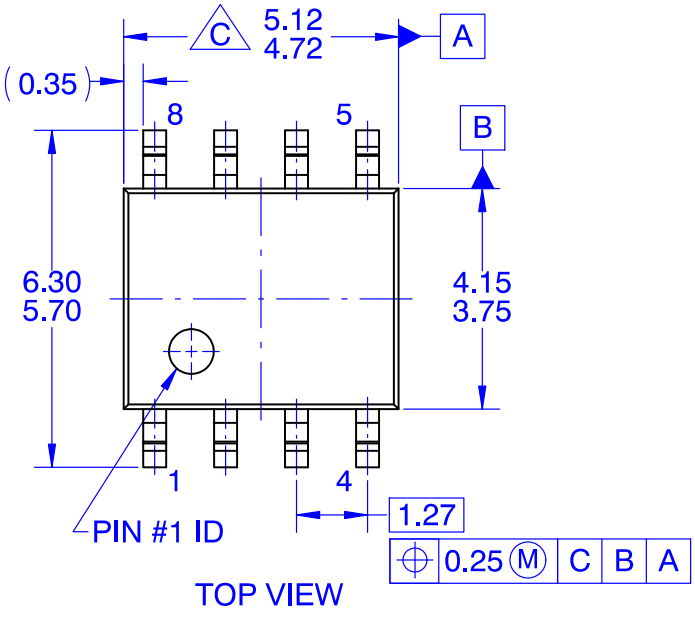
器件编号	工作温度范围	封装	Shipping†
FAN7382MX (说明 5)	−40°C ~125°C	SOIC8 (Pb−Free)	3000 / Tape & Reel
FAN7382M1X (说明 5)		SOIC14 N (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

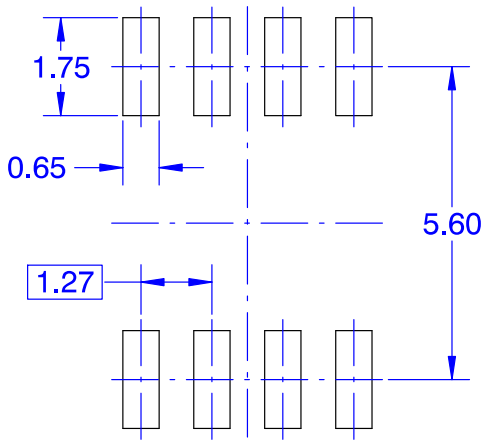
5. 这些器件通过了 JESD22A−111 波峰焊测试。

SOIC8
CASE 751EG
ISSUE O

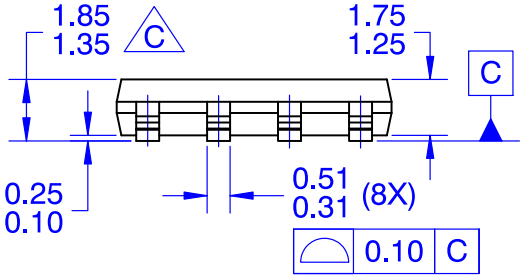
DATE 30 SEP 2016



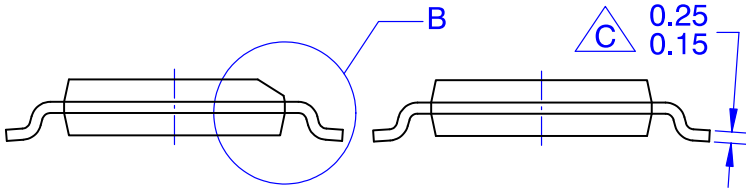
TOP VIEW



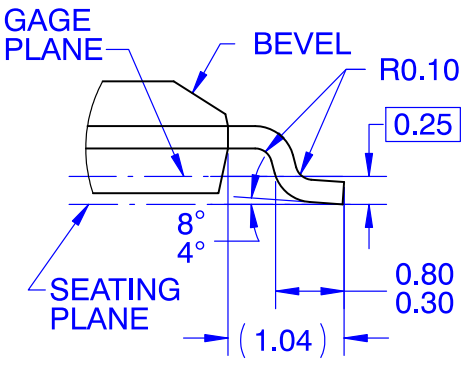
LAND PATTERN RECOMMENDATION



FRONT VIEW



SIDE VIEW



DETAIL "B"
SCALE 2:1

NOTES: UNLESS OTHERWISED SPECIFIED

A. THIS PACKAGE CONFORMS TO JEDEC MS–012 VARIATION A EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS
C OUT OF JEDEC STANDARD VALUE
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
E. LAND PATTERN AS PER IPC SOIC127P600X175–8M

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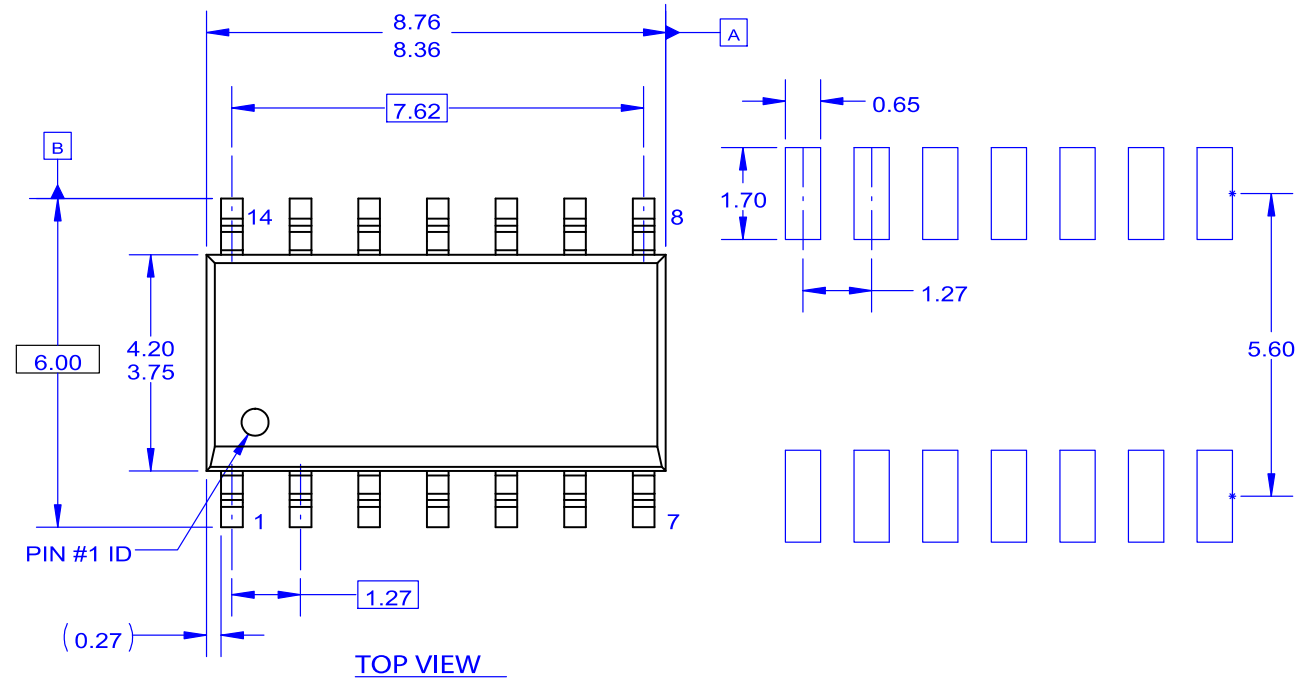
DESCRIPTION:	**SOIC8**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

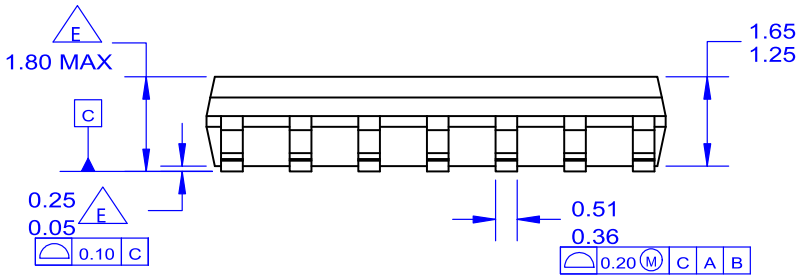
ON Semiconductor®

SOIC14 N
CASE 751ER
ISSUE O

DATE 31 DEC 2016

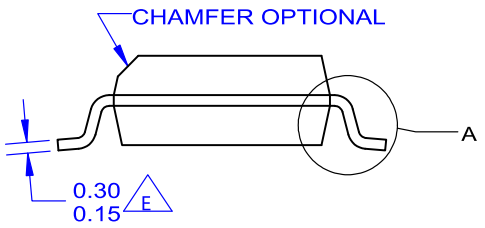


TOP VIEW



ALL LEAD TIPS

SIDE VIEW



END VIEW

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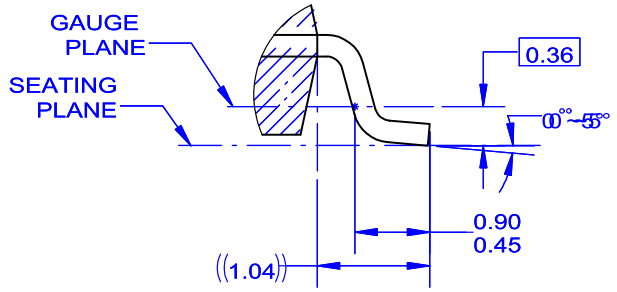
D. DIMENSIONS AND TOLERANCES AS PER ASME Y14.5-1994.
E OUT OF JEDEC STANDARD VALUE.



DETAIL "A"
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