MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

Synchronous Presettable Binary Counter

The MC74AC161/74ACT161 and MC74AC163/74ACT163 are high−speed synchronous modulo−16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters.

The MC74AC161/74ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC163/74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Features

- Synchronous Counting and Loading
- High−Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- ′ACT161 and ′ACT163 Have TTL Compatible Inputs
- These are Pb−Free Devices

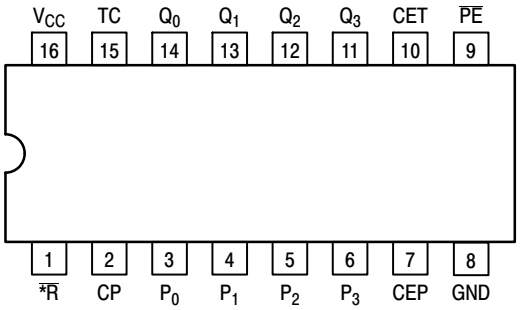

Figure 1. Pinout: 16−Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$	(′161) Asynchronous Master Reset Input
$\overline{SR}$	(′163) Synchronous Reset Input
P_0−P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0−Q_3	Flip−Flop Outputs
TC	Terminal Count Output

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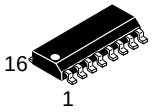
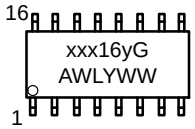
MARKING DIAGRAM



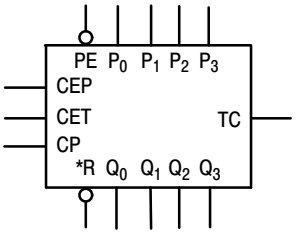
SOIC−16
D SUFFIX
CASE 751B



xxx	= AC or ACT
y	= 1 or 3
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.



*$\overline{MR}$ for ′161
*$\overline{SR}$ for ′163

Figure 2. Logic Symbol

FUNCTIONAL DESCRIPTION

The MC74AC161/ACT161 and MC74AC163/ACT163 count modulo−16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip−flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the ′161) occur as a result of, and synchronous with, the LOW−to−HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (′161), synchronous reset (′163), parallel load, count−up and hold. Five control inputs − Master Reset ($\overline{MR}$, ′161), Synchronous Reset ($\overline{SR}$, ′163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) − determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip−flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (′161) or $\overline{SR}$ (′163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC161/ACT161 and MC74AC163/ACT163 use D−type edge−triggered flip−flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip−flops, counters or registers.

Logic Equations:

$$\text{Count Enable} = CEP \bullet CET \bullet \overline{PE}$$

$$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$$

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	**Action on the Rising Clock Edge ( )**
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For ′163 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

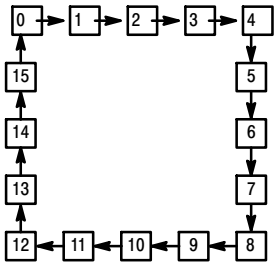
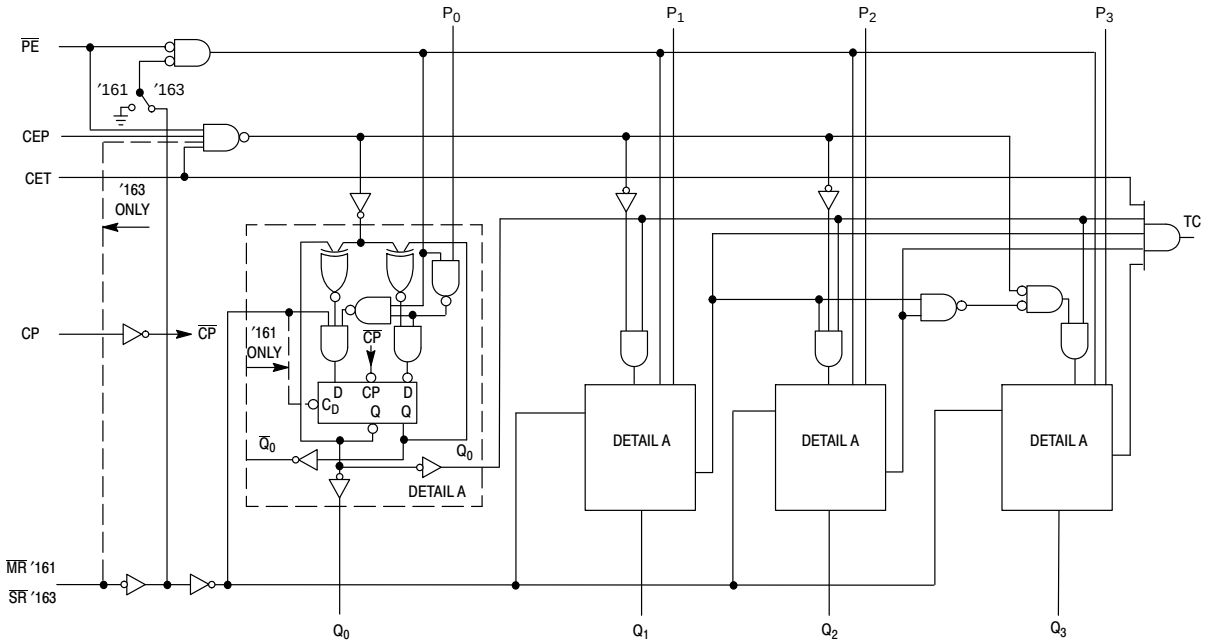


Figure 3. State Diagram



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 4. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0	V
V_I	DC Input Voltage	$-0.5 \le V_I \le V_{CC} + 0.5$	V
V_O	DC Output Voltage (Note 1)	$-0.5 \le V_O \le V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	±20	mA
I_{OK}	DC Output Diode Current	±50	mA
I_O	DC Output Sink/Source Current	±50	mA
I_{CC}	DC Supply Current per Output Pin	±50	mA
I_{GND}	DC Ground Current per Output Pin	±50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction temperature under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2)	69.1	°C/W
P_D	Power Dissipation in Still Air at 65°C (Note 3)	500	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 4) Machine Model (Note 5) Charged Device Model (Note 6)	> 2000 > 200 > 1000	V
$I_{Latch-Up}$	Latch−Up Performance Above V_{CC} and Below GND at 85°C (Note 7)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51−7.
3. 500 mW at 65°C; derate to 300 mW by 10 mW/ from 65°C to 85°C.
4. Tested to EIA/JESD22−A114−A.
5. Tested to EIA/JESD22−A115−A.
6. Tested to JESD22−C101−A.
7. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	−	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	−	150	−	ns/V
		V_{CC} @ 4.5 V	−	40	−	
		V_{CC} @ 5.5 V	−	25	−	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	−	10	−	ns/V
		V_{CC} @ 5.5 V	−	8.0	−	
T_J	Junction Temperature (PDIP)		−	−	140	°C
T_A	Operating Ambient Temperature Range		−40	25	85	°C
I_{OH}	Output Current − High		−	−	−24	mA
I_{OL}	Output Current − Low		−	−	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		74AC T_A = −40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = −50 μA
		3.0 4.5 5.5	− − −	2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} −12 mA I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5	− − −	0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	−	−	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC161 T_A = +25°C C_L = 50 pF			74AC161 T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	111 167	− −	60 95	− −	MHz	3−3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.0 5.0	12.0 9.0	1.5 1.0	13.5 9.5	ns	3−6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	7.0 5.0	12.0 9.5	1.5 1.5	13.0 10.0	ns	3−6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.0 6.0	15.0 10.5	2.5 1.5	16.5 11.5	ns	3−6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	8.5 6.5	14.0 11.0	2.5 2.0	15.5 11.5	ns	3−6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	5.5 3.5	9.5 6.5	1.5 1.0	11.0 7.5	ns	3−6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	6.5 5.0	11.0 8.5	2.0 1.5	12.5 9.5	ns	3−6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	2.0 1.5	6.0 5.5	12.0 9.5	1.5 1.5	13.5 10.0	ns	3−6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	3.3 5.0	3.5 2.5	10.0 8.5	15.0 13.0	3.0 2.5	17.5 13.5	ns	3−6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC163 T_A = +25°C C_L = 50 pF			74AC163 T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	95 140	− −	60 95	− −	MHz	3−3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.5 5.5	12.5 9.0	1.5 1.0	13.5 9.5	ns	3−6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	12.0 9.5	1.5 1.5	13.0 10.0	ns	3−6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.5 7.0	15.0 10.5	2.5 1.5	16.5 11.5	ns	3−6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	11.0 8.0	14.0 11.0	2.5 2.0	15.5 11.5	ns	3−6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	7.5 5.5	9.5 6.5	1.5 1.0	11.0 7.5	ns	3−6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	8.5 6.0	11.0 8.5	2.0 1.5	12.5 9.5	ns	3−6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC161 T_A = +25°C C_L = 50 pF		74AC161 T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	6.0 3.5	13.5 8.5	16.0 10.5	ns	3−9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −4.0	−1.0 0	−0.5 0	ns	3−9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	6.5 4.0	11.5 7.5	14.0 8.5	ns	3−9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−6.0 −3.5	0 0.5	0 1.0	ns	3−9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.0 2.0	6.0 4.5	7.0 5.0	ns	3−9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−3.5 −2.0	0 0	0 0.5	ns	3−9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	2.0 2.0	3.5 2.5	4.0 3.0	ns	3−6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	2.0 2.0	4.0 3.0	4.5 3.5	ns	3−6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	3.0 2.5	5.5 4.5	7.5 6.0	ns	3−6
t_{rec}	Recovery TIme $\overline{MR}$ to CP	3.3 5.0	−2.0 −1.0	−0.5 0	0 0.5	ns	3−9

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC163 T_A = +25°C C_L = 50 pF		74AC163 T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0	13.5 8.5	16.0 10.5	ns	3−9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0	−1.0 0	−0.5 0	ns	3−9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0	14 9.5	16.5 11.0	ns	3−9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5	−1.0 −0.5	−0.5 0	ns	3−9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0	11.5 7.5	14.0 8.5	ns	3−9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.0	−1.0 −0.5	−0.5 0	ns	3−9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5	7.0 5.0	ns	3−9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0	0 0	0 0.5	ns	3−9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5	4.0 3.0	ns	3−6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0	4.5 3.5	ns	3−6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT		74ACT	Unit	Conditions
			T_A = +25°C		T_A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5	− −	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5	− −	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	−	1.5	mA	V_I = V_{CC} − 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	−	−	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT161 T_A = +25°C C_L = 50 pF			74ACT161 T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	115	125	−	100	−	MHz	3−3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	8.0	9.5	1.5	10.5	ns	3−6
t_{PHL}	Propagation Delay CP or Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	8.0	10.5	1.5	11.5	ns	3−6
t_{PLH}	Propagation Delay CP to TC	5.0	2.0	11.0	11.0	1.5	12.5	ns	3−6
t_{PHL}	Propagation Delay CP to TC	5.0	1.5	11.0	12.5	1.5	13.5	ns	3−6
t_{PLH}	Propagation Delay CET to TC	5.0	1.5	7.5	8.5	1.5	10.0	ns	3−6
t_{PHL}	Propagation Delay CET to TC	5.0	1.5	8.0	9.5	1.5	10.5	ns	3−6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.5	8.0	10.0	1.5	11.0	ns	3−6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	5.0	2.5	10.0	13.5	2.0	14.5	ns	3−6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT163 T_A = +25°C C_L = 50 pF			74ACT163 T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	120	140	−	105	−	MHz	3−3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	5.5	10.0	1.5	11.0	ns	3−6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	6.0	11.0	1.5	12.0	ns	3−6
t_{PLH}	Propagation Delay CP to TC	5.0	2.5	7.0	11.5	2.0	13.5	ns	3−6
t_{PHL}	Propagation Delay CP to TC	5.0	3.0	8.0	13.5	2.0	15.0	ns	3−6
t_{PLH}	Propagation Delay CET to TC	5.0	2.0	5.5	9.0	1.5	10.5	ns	3−6
t_{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	10.0	2.0	11.0	ns	3−6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT161 T_A = +25°C C_L = 50 pF		74ACT161 T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	7.0	9.5	11.5	ns	3−9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−3.0	0	0	ns	3−9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	6.0	8.5	9.5	ns	3−9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−3.5	− 0.5	− 0.5	ns	3−9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	4.0	5.5	6.5	ns	3−9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−2.0	0	0	ns	3−9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3−6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3−6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	3.0	3.0	7.5	ns	3−6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0	0.5	ns	3−9

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT163 T_A = +25°C C_L = 50 pF		74ACT163 T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	10.0	12.0	ns	3−9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0.5	0.5	ns	3−9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	4.0	10.0	11.5	ns	3−9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	−5.5	−0.5	−0.5	ns	3−9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5	10.5	ns	3−9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5	0	ns	3−9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns	3−9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0	0.5	ns	3−9
t_w	Clock Pulse Width HIGH or LOW	5.0	2.0	3.5	3.5	ns	3−6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5	3.5	ns	3−6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

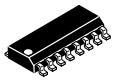
CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

ORDERING INFORMATION

Device	Package	Shipping†
MC74AC161DG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74AC161DR2G		2500 / Tape & Reel
MC74ACT161DG		48 Units / Rail
MC74ACT161DR2G		2500 / Tape & Reel
MC74AC163DG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74AC163DR2G		2500 / Tape & Reel
MC74ACT163DG		48 Units / Rail
MC74ACT163DR2G		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

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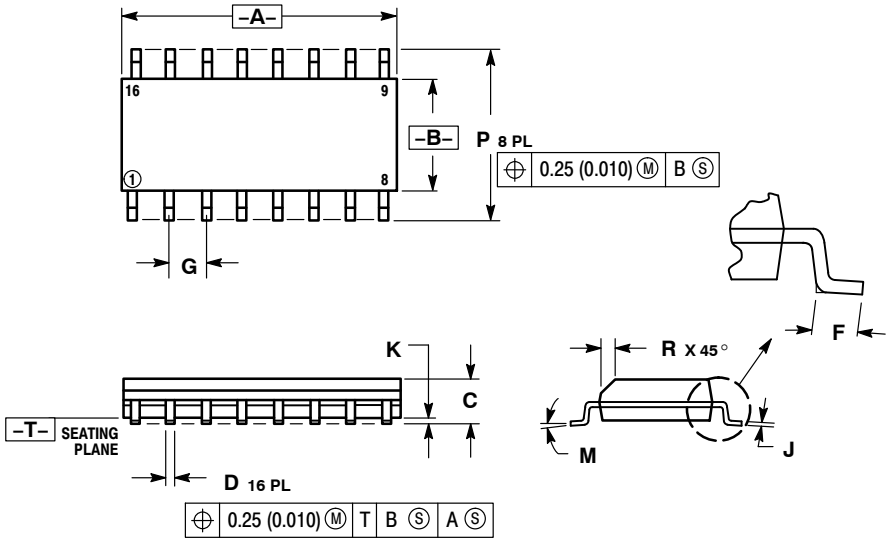
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

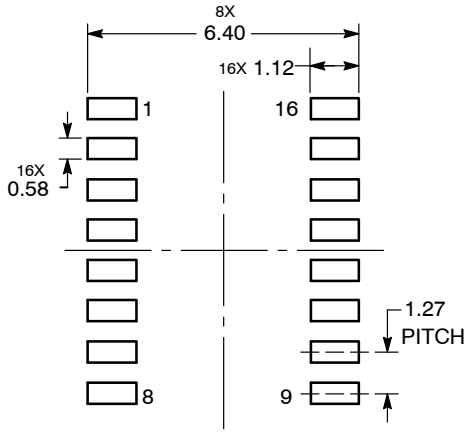
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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