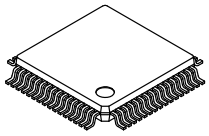
CMOS LSI
Iris/Zoom/Focus/Day-Night Switching Drive Controller
LC898201



TQFP64 7x7
CASE 932BC

Overview

LC898201 is the appropriate motor control LSI for the surveillance camera usage, and it can drive iris, focus, zoom and Day/Night switching simultaneously.

It incorporates feedback control circuits (max 2-systems), stepper motor control circuits (max 3-system) and VCM control circuit (1-system).

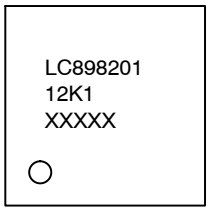
- Feedback Control Applies Iris
  Stepper Motor Controls Apply Focus, Zoom and Day/Night Switching
- Feedback Control Applies Iris
  Stepper Motor Controls Apply Focus and Zoom
  VCM Applies Day/Night Switching

LC898201 can control a variety of lens units like these examples.

Features

- Built-in Equalizer Circuit by Digital Operation
  - Iris Control Equalizer Circuit
  - Focus Control Equalizer Circuit (MR sensor can be connected)
  - Coefficients can be Set Arbitrarily through the SPI Interface
  - Computed Values in the Equalizer can be Monitored
- Built-in 3ch Stepper Motor Control Circuits
- SPI Bus Interface
- PI Control Circuit
  - 30 mA Sink Output Terminal
  - Built-in PI Detecting Function (A/D method)
- A/D Converter
  - 12bit (6ch): Iris, Focus, PI Detection, General
- D/A Converter
  - 8bit (4ch): Hall Offset, Constant Current Bias, MR Sensor Offset
- Operation Amplifier
  - 3ch (Iris Control ×1, Focus Control ×2)
- PWM Pulse Generator
  - PWM Pulse Generator for Feedback Control (Up to 12 bit Accuracy)
  - PWM Pulse Generator for Stepper Motor Control (Up to 1024 Micro Steps)
  - PWM Pulse Generator for General-purpose H-Bridge (128 Voltage Levels)
- Motor Driver
  - ch1 to ch6: Io max = 200 mA
  - ch7: Io max = 300 mA
  - Built-in Thermal Protection Circuit
  - Built-in Low-voltage Malfunction Prevention Circuit

MARKING DIAGRAM



LC898201	= Specific Device Code 1
12K1	= Specific Device Code 2
XXXXX	= Lot Number

ORDERING INFORMATION

Device	Package	Shipping†
LC898201TA–NH	TQFP64 7x7 (Pb–Free / Halogen Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

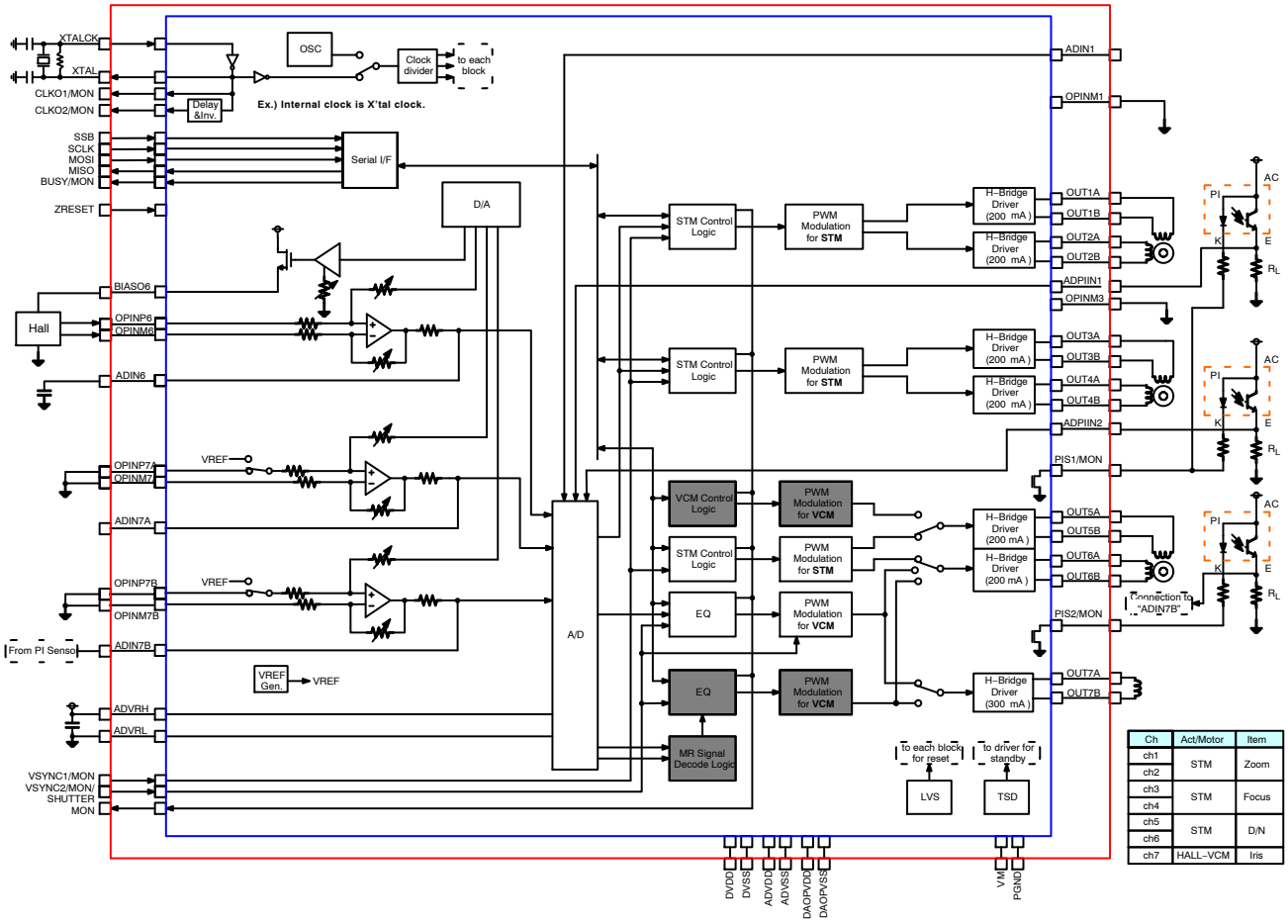
Features (Continued)

- Operation Clock
  - Selective Usage either Internal OSC (Typ. 48 MHz) or External Oscillating Circuit (48 MHz)
- Package
  - TQFP64 (7 × 7) 0.4 mm Pitch
  - Lead-free, Halogen-free
- Power Supply Voltage
  - Logic Unit: 2.7 V to 3.6 V (IO, Internal Core)
  - Driver Unit: 2.7 V to 5.5 V (Motor Drive)

BLOCK DIAGRAMS

Application 1

Stepper 3ch-ex.1 & using Crystal oscillator (or Ceramic oscillator) & PI sensor: R_L emitter connection.



Ch	Act/Motor	Item
ch1	STM	Zoom
ch2		
ch3	STM	Focus
ch4		
ch5	STM	D/N
ch6		
ch7	HALL-VCM	Iris

Figure 1. Application 1

Application 2

Stepper 3ch-ex.2 & using internal OSC & PI sensor: R_L collector connection.

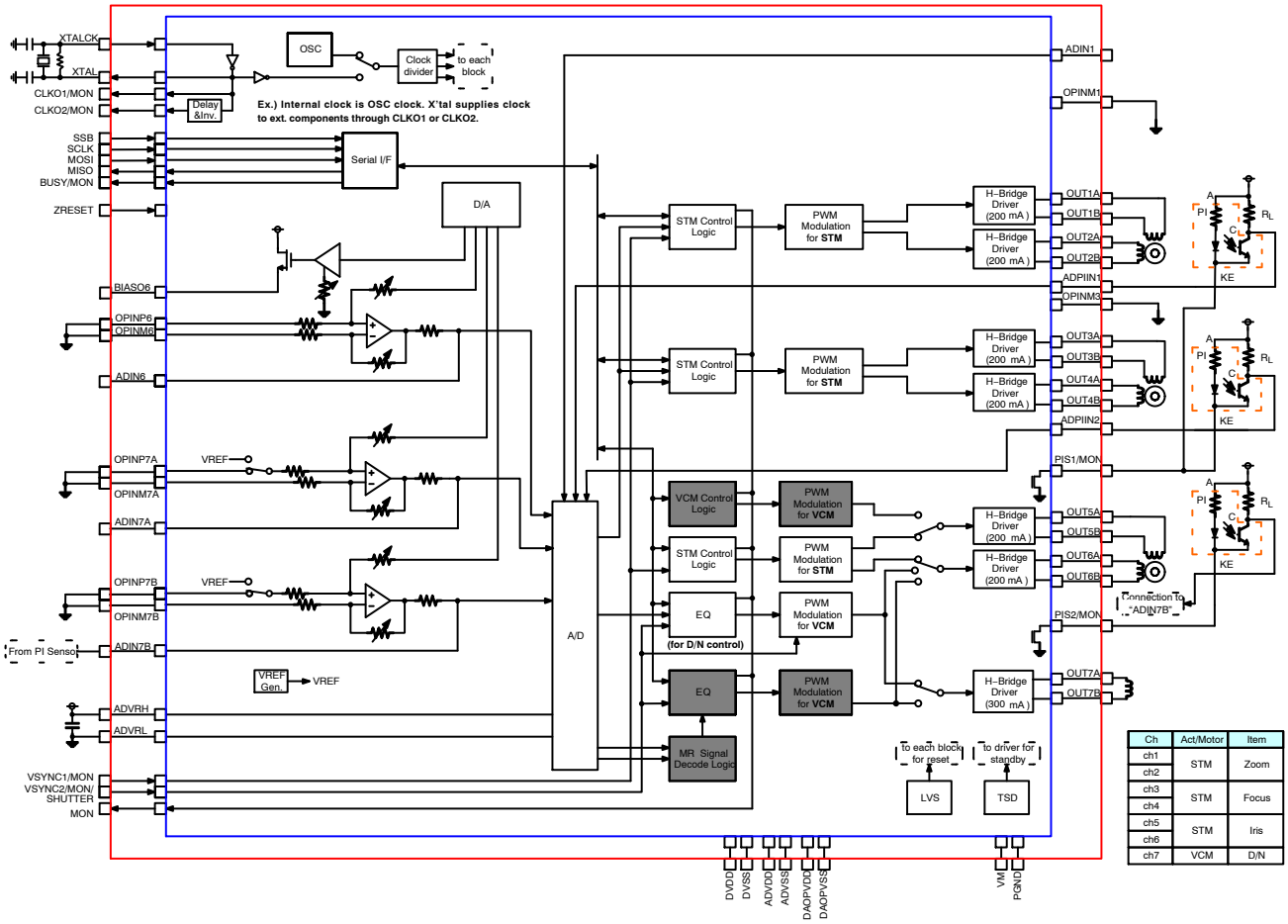


Figure 2. Application 2

Application−3

Stepper 2ch & using internal OSC & PI sensor: R_L emitter connection.

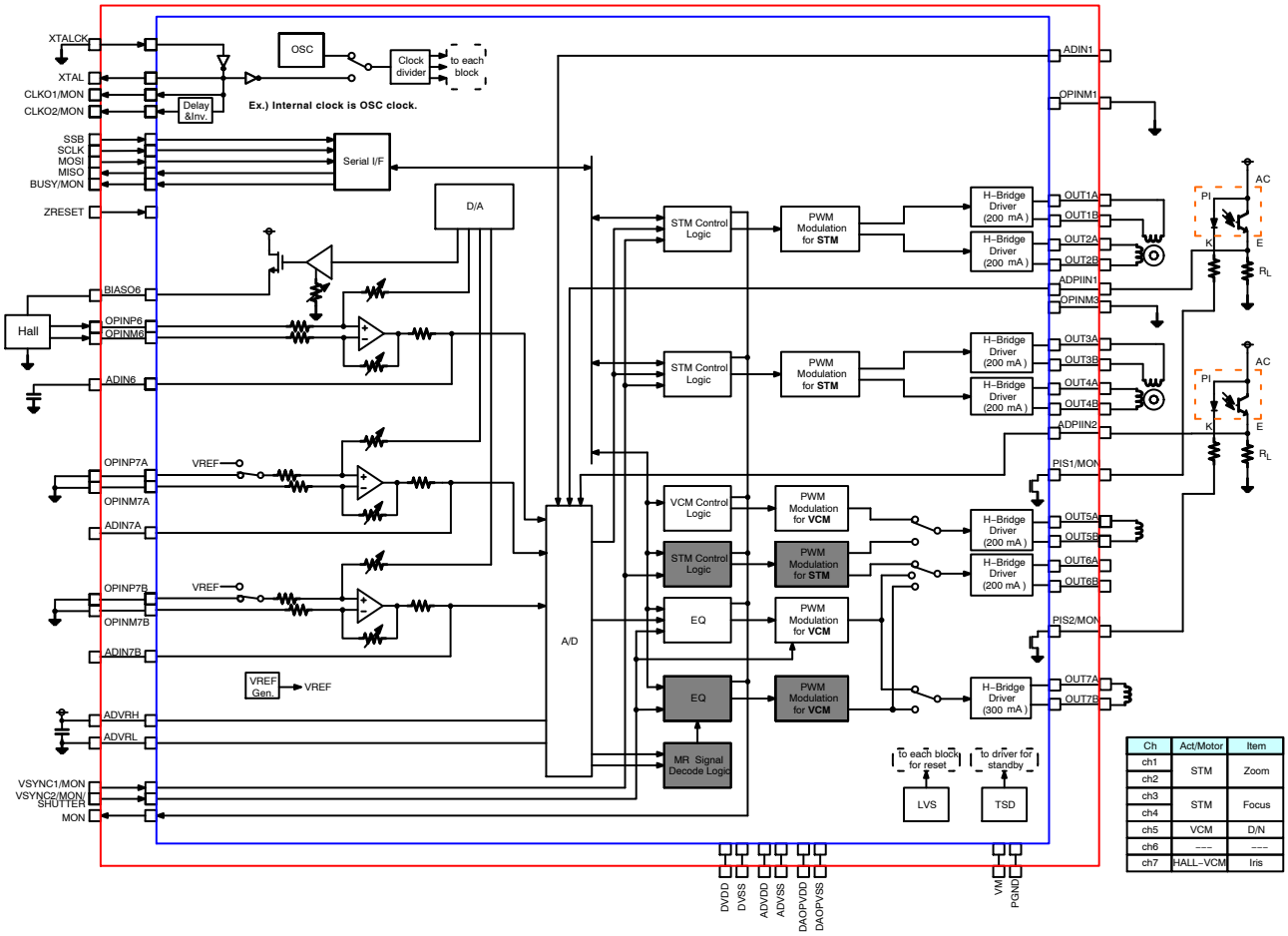


Figure 3. Application 3

Application−4

MR−VCM & using internal OSC & PI sensor: R_L emitter connection.

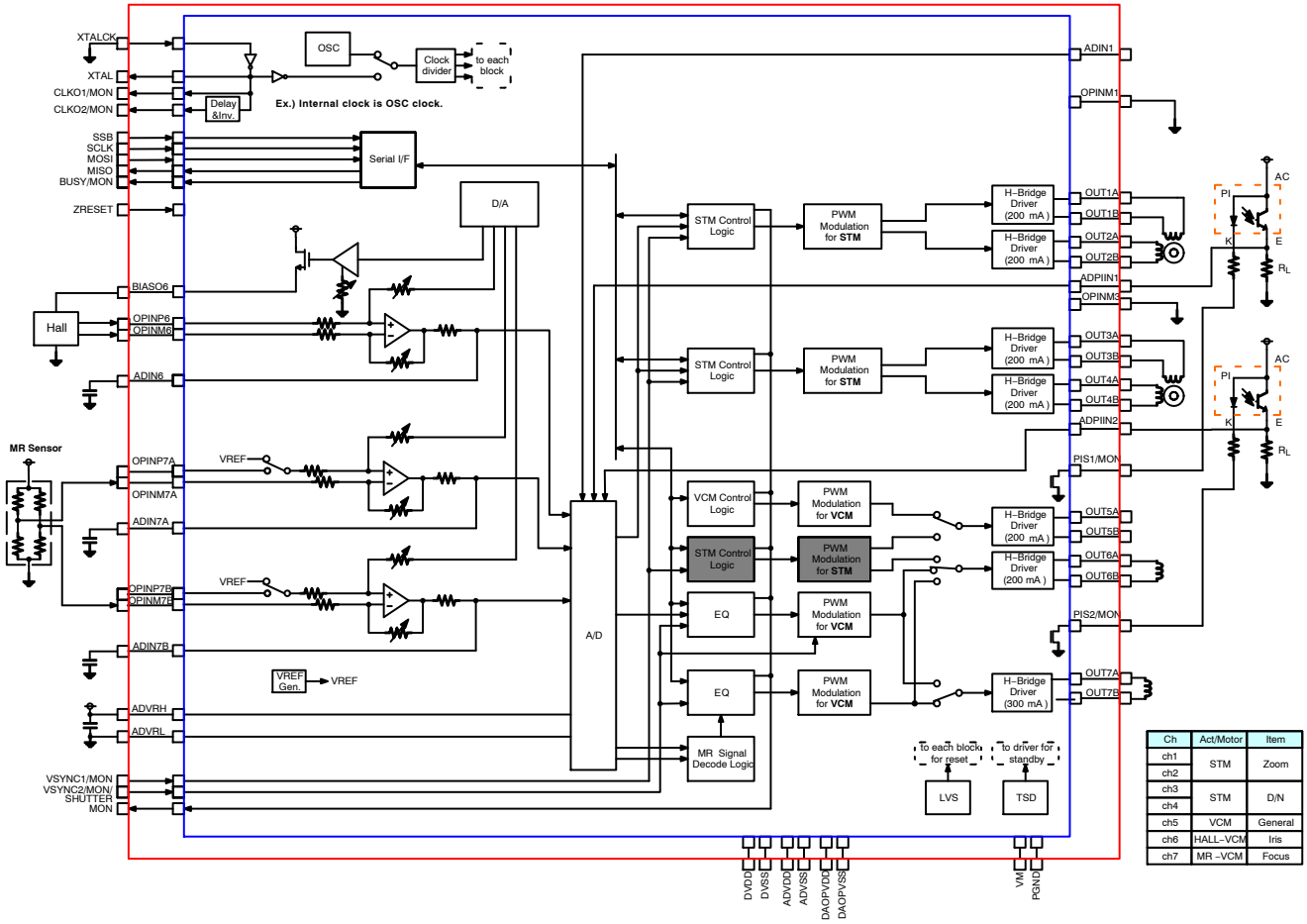


Figure 4. Application 4

PIN DESCRIPTION

Table 1. PIN DESCRIPTION

TYPE					
I	INPUT	P	Power, GND	NC	NOT CONNECT
O	OUTPUT				
B(I)	BIDIRECTION: INPUT at Reset				
B(O)	BIDIRECTION: OUTPUT at Reset				

SPI INTERFACE (SLAVE)		
SSB	I	Chip select
SCLK	I	Clock
MOSI	I	Received data
MISO	B(O)	Transmit data
BUSY/MON	B(O)	Transfer busy / Monitor output
PI SENSOR DRIVE SIGNAL OUTPUT		
PIS1/MON	B(O)	PI sensor drive signal output 1 / Monitor output
PIS2/MON	B(O)	PI sensor drive signal output 2 / Monitor output
VIDEO SYNCHRONIZING SIGNAL INPUT		
VSYNC1/MON	B(I)	Video synchronizing signal input / Monitor output (with pull-down resistance)
VSYNC2/MON /SHUTTER	B(I)	Video synchronizing signal input / Monitor output / Shutter input (with pull-down resistance)
MONITOR OUTPUT		
MON	B(O)	Monitor output
CLOCK OUTPUT		
XTALCK	I	Oscillation amplifier input
XTAL	O	Oscillation amplifier output
CLKO1/MON	B(O)	Clock output 1 / Monitor output
CLKO2/MON	B(O)	Clock output 2 / Monitor output
RESET		
ZRESET	I	Reset signal input (Low active)
BIAS CURRENT PIN		
BIASO6	O	CH6 Bias current output
OP AMP PIN		
OPINP6	I	CH6 OP Amp input (+)
OPINM6	I	CH6 OP Amp input (−)
OPINP7A	I	CH7−A OP Amp input (+)
OPINM7A	I	CH7−A OP Amp input (−)
OPINP7B	I	CH7−B OP Amp input (+)
OPINM7B	I	CH7−B OP Amp input (−)
A/D INPUT PIN		
ADIN1	B	General A/D input
ADIN6	B	CH6 A/D input (CH6 OP Amp output)
ADIN7A	B	CH7−A A/D input (CH7 OP Amp output)

A/D INPUT PIN		
ADIN7B	B	CH7−B A/D input (CH7 OP Amp output)
ADPIIN1	I	CH1/2 PI sensor signal A/D input
ADPIIN2	I	CH3/4 PI sensor signal A/D input
ADVRH	I	A/D conversion range standard voltage
ADVRL	I	A/D conversion range standard voltage
H−BRIDGE		
OUT1A	O	CH1 H−Bridge output
OUT1B	O	CH1 H−Bridge output
OUT2A	O	CH2 H−Bridge output
OUT2B	O	CH2 H−Bridge output
OUT3A	O	CH3 H−Bridge output
OUT3B	O	CH3 H−Bridge output
OUT4A	O	CH4 H−Bridge output
OUT4B	O	CH4 H−Bridge output
OUT5A	O	CH5 H−Bridge output
OUT5B	O	CH5 H−Bridge output
OUT6A	O	CH6 H−Bridge output
OUT6B	O	CH6 H−Bridge output
OUT7A	O	CH7 H−Bridge output
OUT7B	O	CH7 H−Bridge output
MISCELLANEOUS		
OPINM1	I	Connect to GND (DAOPVSS)
OPINM3	I	Connect to GND (DAOPVSS)
POWER PIN		
DVDD	P	Digital VDD
DVSS	P	Digital GND
DAOPVDD	P	D/A, OP Amp VDD
DAOPVSS	P	D/A, OP Amp GND
ADVDD	P	A/D VDD
ADVSS	P	A/D GND
VM	P	H−Bridge VDD
PGND	P	H−Bridge GND

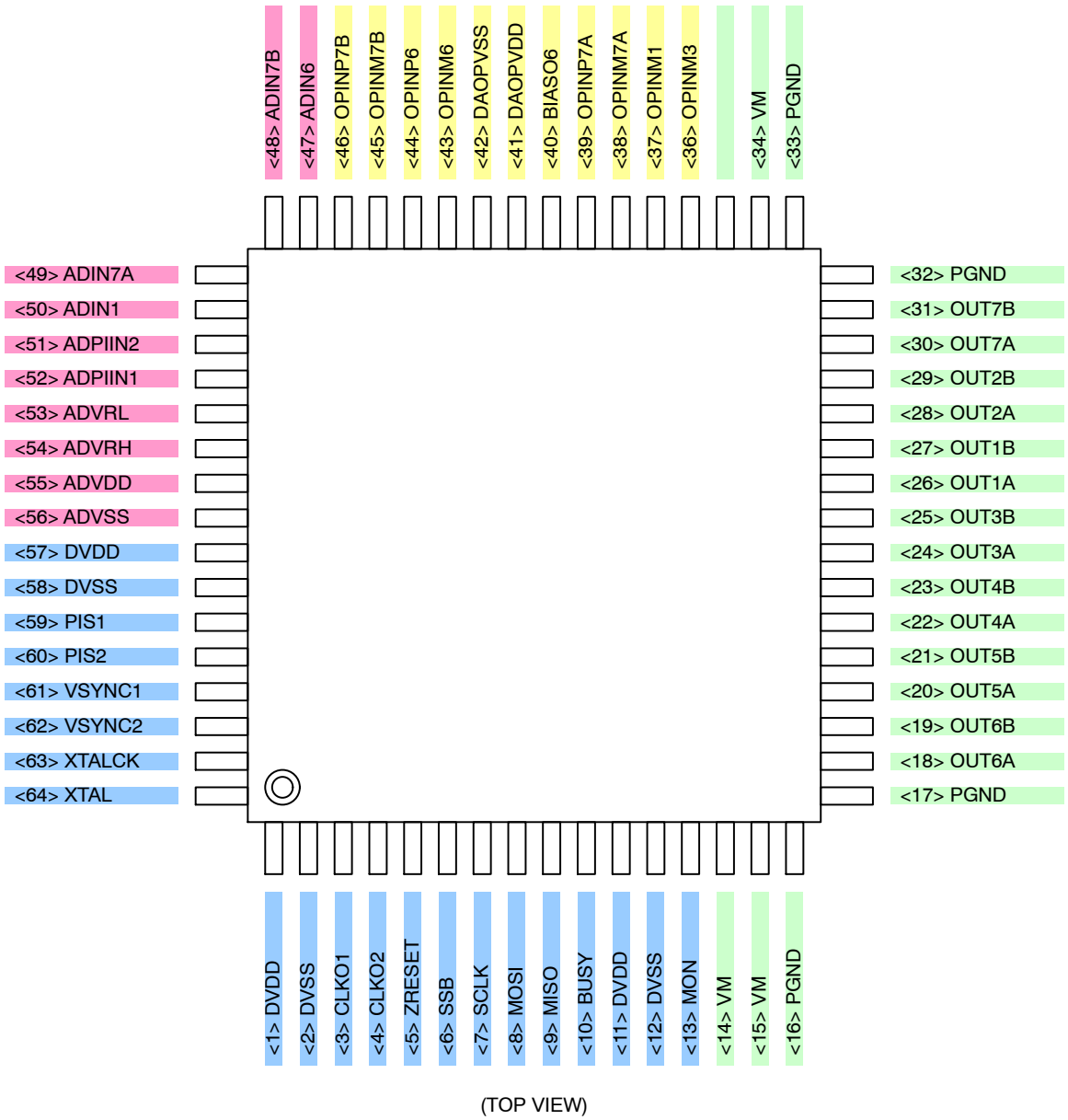
Process when pins are not used

- PIN TYPE “O” − The pin must be left open
- PIN TYPE “I” − The pin must not be left open. Please make sure to connect the pin to V_{DD} or V_{SS} even when it is not used. (Please check with us whether to connect to V_{DD} or V_{SS})
- PIN TYPE “B” − Please contact us if you are uncertain about a processing method in the pin description in the PIN layout table

A problem may occur if the processing method is used wrongly for any unused pin.

Please make sure to contact us.

PIN ASSIGNMENT



(TOP VIEW)

Figure 5. TQFP64 (7×7)

PIN NUMBER

Table 2. PIN NUMBER

Pin No.	Type	Pin name
1	P	DVDD
2	P	DVSS
3	B(O)	CLKO1
4	B(O)	CLKO2
5	I	ZRESET
6	I	SSB
7	I	SCLK
8	I	MOSI
9	B(O)	MISO
10	B(O)	BUSY
11	P	DVDD
12	P	DVSS
13	B(O)	MON
14	P	VM
15	P	VM
16	P	PGND
17	P	PGND
18	O	OUT6A
19	O	OUT6B
20	O	OUT5A
21	O	OUT5B
22	O	OUT4A
23	O	OUT4B
24	O	OUT3A
25	O	OUT3B
26	O	OUT1A
27	O	OUT1B
28	O	OUT2A
29	O	OUT2B
30	O	OUT7A
31	O	OUT7B
32	P	PGND
33	P	PGND
34	P	VM
35	P	VM
36	I	OPINM3
37	I	OPINM1
38	I	OPINM7A
39	I	OPINP7A
40	O	BIASO6

Table 2. PIN NUMBER (continued)

Pin No.	Type	Pin name
41	P	DAOPVDD
42	P	DAOPVSS
43	I	OPINM6
44	I	OPINP6
45	I	OPINM7B
46	I	OPINP7B
47	B	ADIN6
48	B	ADIN7B
49	B	ADIN7A
50	B	ADIN1
51	I	ADPIIN2
52	I	ADPIIN1
53	I	ADVRL
54	I	ADVRH
55	P	ADVDD
56	P	ADVSS
57	P	DVDD
58	P	DVSS
59	B(O)	PIS1
60	B(O)	PIS2
61	B(I)	VSYNC1
62	B(I)	VSYNC2
63	I	XTALCK
64	O	XTAL

ELECTRICAL CHARACTERISTICS

Logic, Analog

Logic, Analog power: DVDD/DVSS, OPDAVDD/ OPDAVSS, ADVDD/ADVSS, these should be connected at the same voltage. They are shown DVDD/DVSS as follows.

ABSOLUTE MAXIMUM RATINGS (DVSS = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	DVDD max	$T_A \le 25°C$	–0.3 to 4.6	V
Input/Output Voltage	V_{IN}, V_{OUT}	$T_A \le 25°C$	–0.3 to DVDD+0.3	V
Storage Temperature	T_{stg}		–55 to 125	°C
Operating Temperature	T_{opr}		–20 to 85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ALLOWABLE OPERATING RANGES (T_A = –20 to 85°C, DVSS = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Applicable Pins
Power Supply Voltage	DVDD	2.7	3.3	3.6	V	
Input Voltage Range	V_{IN}	0	–	DVDD	V	Except for OPINM1, OPINM3
		0	–	VM	V	OPINM1, OPINM3

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS: INPUT/OUTPUT LEVEL (T_A = –20 to 85°C, DVSS = 0 V, DVDD = 2.7 to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pins
High-level Input Voltage	V_{IH}	CMOS	0.7 DVDD			V	(2)(3)
Low-level Input Voltage	V_{IL}				0.2 DVDD	V	
High-level Input Voltage	V_{IH}	CMOS Schmidt	0.75 DVDD			V	(1)
Low-level Input Voltage	V_{IL}				0.15 DVDD	V	
High-level Output Voltage	V_{OH}	I_{OH} = –4 mA	DVDD – 0.4			V	(2)(3)(4)
Low-level Output Voltage	V_{OL}	I_{OL} = 4 mA			0.4	V	(2)(3)
		I_{OL} = 30 mA			0.4	V	(4)
PullDown Resistance	Rdn		40	80	200	kΩ	(3)
Analog Input Voltage	V_{AI}		DVSS		DVDD	V	(5)
			PGND		VM	V	(6)
VGA Output Resistance	R_{out}			1		kΩ	(7)
Analog Output Current	I_{AO}	CMSDAC = 001b & WH_DAV4 = 00h		1		mA	(8)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Applicable Pins:

(1) ZRESET, SSB, SCLK, MOSI
(2) MISO, BUSY, MON, CLKO1, CLKO2
(3) VSYNC1, VSYNC2
(4) PIS1, PIS2
(5) OPINP6, OPINM6, OPINP7A, OPINM7A, OPINP7B, OPINM7B, ADPIIN1, ADPIIN2
(6) OPINM1, OPINM3
(7) ADIN1, ADIN6, ADIN7A, ADIN7B
(8) BIASO6

VM

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, PGND = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	VM_{max}		–0.3 to 7.0	V
Output Peak Current	I_{opeak1}	OUT1A/B to OUT6A/B t ≤ 10 ms, On-duty ≤ 20%	300	mA
	I_{opeak2}	OUT7A/B t ≤ 10 ms, On-duty ≤ 20%	450	mA
Output Continuous Current	I_{omax1}	OUT1A/B to OUT6A/B	200	mA
	I_{omax2}	OUT7A/B	300	mA
Storage Temperature	T_{stg}		–55 to 125	°C
Operating Temperature	T_{opr}		–20 to 85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ALLOWABLE OPERATING RANGES (T_A = 25°C, PGND = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	VM		2.7 to 5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, PGND = 0 V, VM = 5 V)

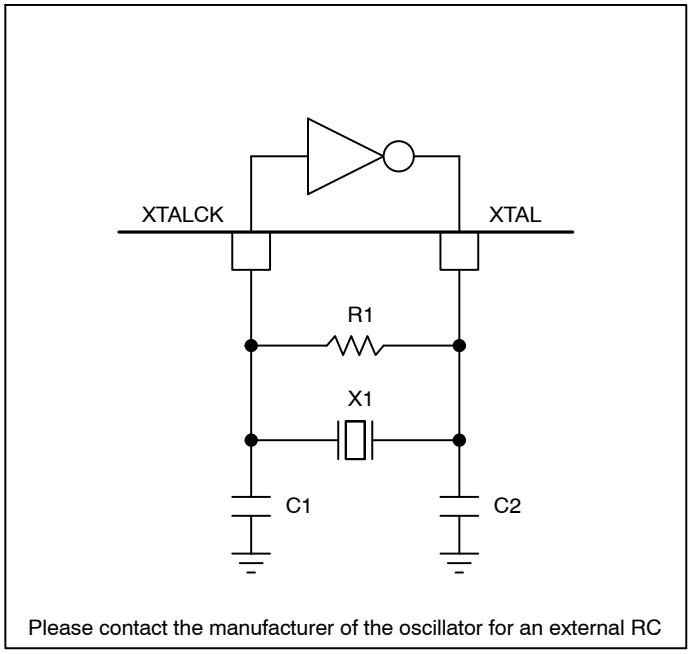
Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pins
Output ON Resistance	R_{onu}	I_O = 200 mA Pch		0.85		Ω	(9)
	R_{ond}	I_O = 200 mA Nch		0.45		Ω	
Output ON Resistance	R_{onu}	I_O = 300 mA Pch		0.85		Ω	(10)
	R_{ond}	I_O = 300 mA Nch		0.45		Ω	
Diode Forward Voltage	V_D	I_D = –200 mA		0.9		V	(9)
		I_D = –300 mA		0.9		V	(10)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Applicable Pins:
(9) OUT1A, OUT1B, OUT2A, OUT2B, OUT3A, OUT3B, OUT4A, OUT4B, OUT5A, OUT5B, OUT6A, OUT6B
(10) OUT7A, OUT7B

EXAMPLE OF EXTERNAL CIRCUIT

Connection example of oscillation circuit.



* In the case of X'tal, it takes about 50 ms for oscillation to stabilize (please check with the manufacturer for a precise time period).

Figure 6. Example of External Circuit

AC CHARACTERISTICS

1−a) Power Supply, Reset Pin

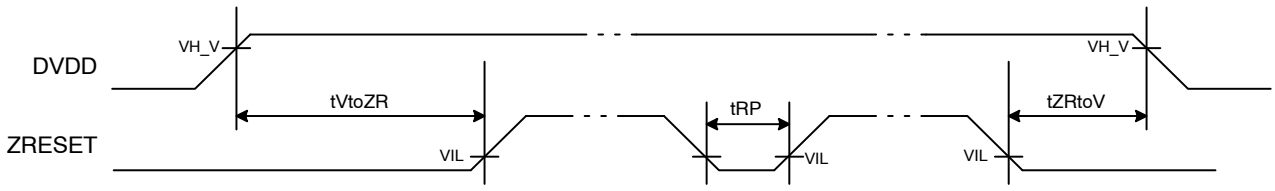


Figure 7.

1−b) Specification

DVDD: DVDD, OPDAVDD, ADVDD
VH_V: 2.7 V
VIL: 0.15 × DVDD

Parameter	Symbol	Min	Typ	Max	Unit
The time from the rise of DVDD to the rise of ZRESET	tVtoZR	1			ms
The time from the fall of DVDD to the fall of ZRESET	tZRtoV	500			μs
Low period of ZRESET	tRP	100			μs

VM can be turn on/off regardless above power supply AC timing.

2−a) Power Supply, Reset Pin

Upper: “H” active Use setting of 0250h−0253h−bit2 = 0
Lower: “L” active Use setting of the above bit = 1

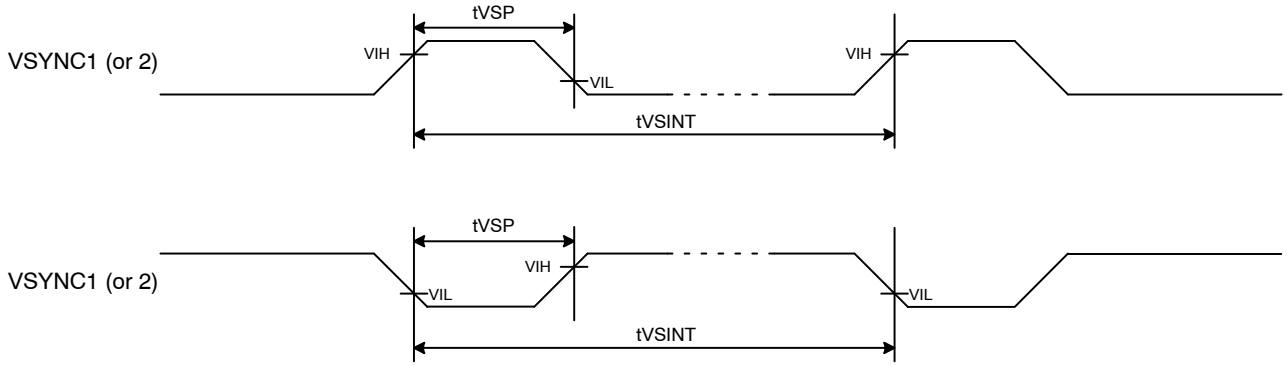


Figure 8.

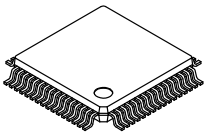
2−b) Specification

VIH: 0.7 × DVDD
VIL: 0.2 × DVDD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Active period of VSYNC1(or 2)	tVSP	STMCLK = 12 MHz	100			ns
Interval time of VSYNC1(or 2)	tVSINT		2			ms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



TQFP64 7x7 / TQFP64
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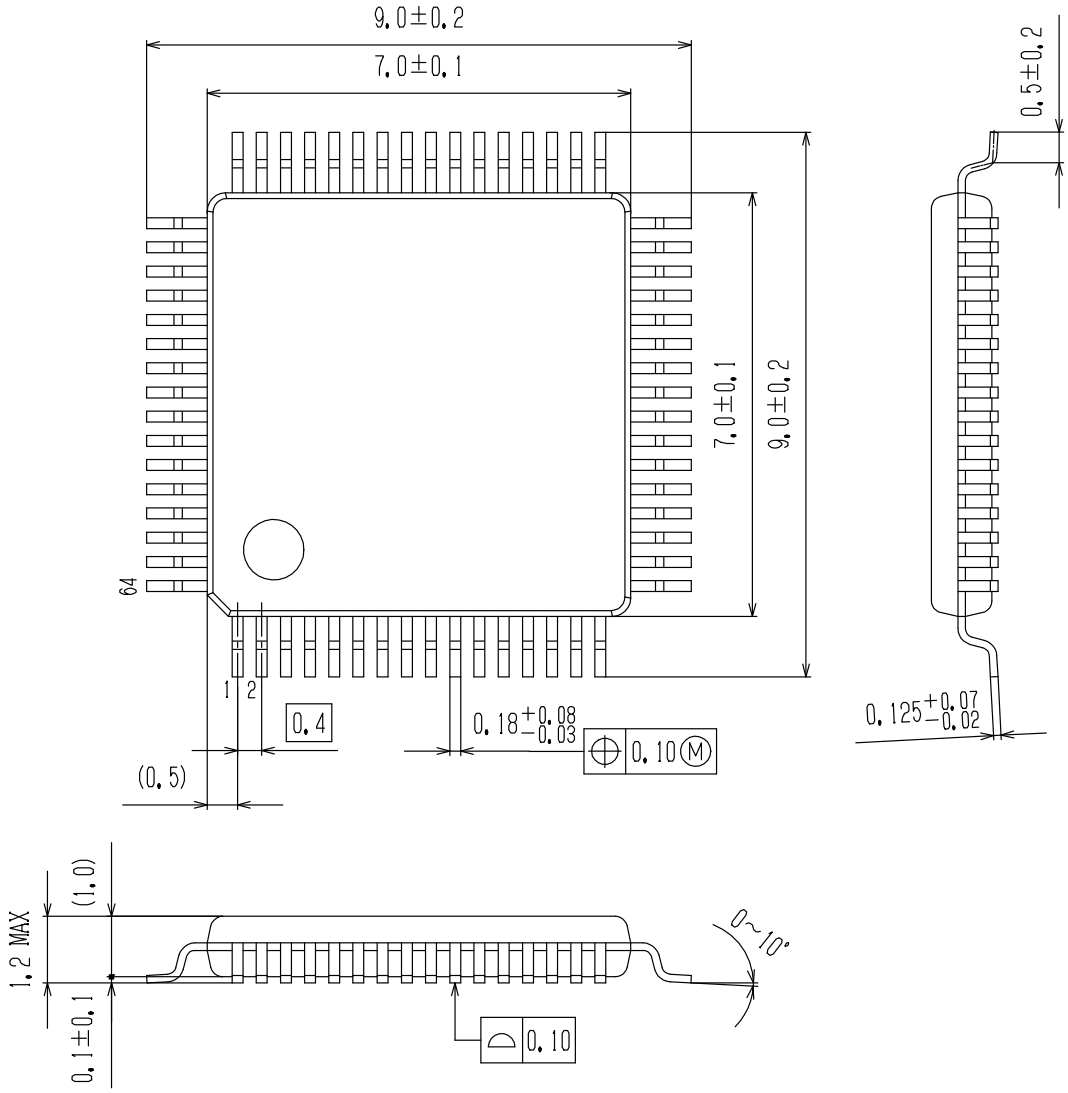
ISSUE O

DATE 31 MAY 2012



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DESCRIPTION:	**TQFP64 7X7 / TQFP64**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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