

# MOSFET – P-Channel, POWERTRENCH®

**-100 V, -50 A, 22 mΩ**

## FDMS86163P

### General Description

This P-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Features

- Max  $r_{DS(on)}$  = 22 mΩ at  $V_{GS} = -10$  V,  $I_D = -7.9$  A
- Max  $r_{DS(on)}$  = 30 mΩ at  $V_{GS} = -6$  V,  $I_D = -5.9$  A
- Very Low RDS-on Mid Voltage P-Channel Silicon Technology Optimised for Low Qg
- This Product is Optimised for Fast Switching Applications As Well As Load Switch Applications
- 100% UIL Tested
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

### Applications

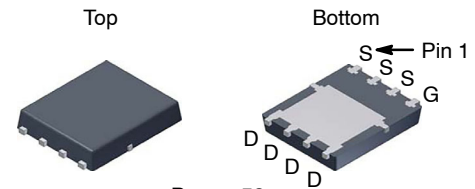
- Active Clamp Switch
- Load Switch

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Parameter	Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DS}$	-100	V
Gate-to-Source Voltage		$V_{GS}$	±25	V
Drain Current -Continuous	$T_C = 25^\circ\text{C}$	$I_D$	-50	A
	$T_A = 25^\circ\text{C}$ (Note 1a)		-7.9	
	-Pulsed (Note 4)		-100	
Single Pulse Avalanche Energy (Note 3)		$E_{AS}$	486	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	104	W
	$T_A = 25^\circ\text{C}$ (Note1a)		2.5	
Operating and Storage Junction Temperature Range		$T_J, T_{STG}$	-55 to +150	°C

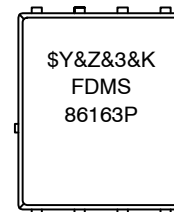
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$BV_{DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
-100 V	22 mΩ @ -10 V	-50 A



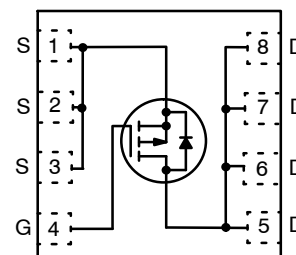
Power 56  
PQFN8  
CASE 483AE

### MARKING DIAGRAM



- \$Y = onsemi Logo
- &Z = Assembly Location
- &3 = 3-Digit Date Code
- &K = Lot Code
- FDMS86163P = Specific Device Code

### PIN CONNECTION



### ORDERING INFORMATION

Device	Package	Shipping†
FDMS86163P	PQFN-8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# FDMS86163P

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1a)	50	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}, V_{GS} = 0 \text{ V}$	-100	-	-	V
$\Delta B_{VDSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	-59	-	mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -80 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	-2	-2.8	-4	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	6.2	-	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10 \text{ V}, I_D = -7.9 \text{ A}$	-	17.8	22	m $\Omega$
		$V_{GS} = -6 \text{ V}, I_D = -5.9 \text{ A}$	-	21.3	30	
		$V_{GS} = -10 \text{ V}, I_D = -7.9 \text{ A}, T_J = 125^\circ\text{C}$	-	29	36	
$g_{FS}$	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_D = -7.9 \text{ A}$	-	29	-	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = -50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	3070	4085	pF
$C_{oss}$	Output Capacitance		-	501	670	
$C_{rss}$	Reverse Transfer Capacitance		-	21	35	
$R_g$	Gate Resistance		0.1	2.6	5.3	$\Omega$

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay	$V_{DD} = -50 \text{ V}, I_D = -7.9 \text{ A}, V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$	-	17	30	ns	
$t_r$	Rise Time		-	8.8	18		
$t_{d(off)}$	Turn-Off Delay		-	33	53		
$t_f$	Fall Time		-	6.9	14		
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V to } -10 \text{ V}$	$V_{DD} = -50 \text{ V}, I_D = -7.9 \text{ A}$	-	42	59	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V to } -6 \text{ V}$		-	26	37	
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = -50 \text{ V}, I_D = -7.9 \text{ A}$	-	11.8	-		
$Q_{gd}$	Gate to Drain "Miller" Charge		-	7.1	-		

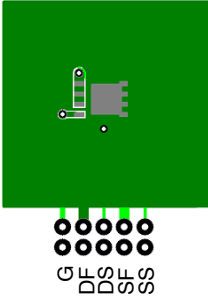
# FDMS86163P

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified) (continued)

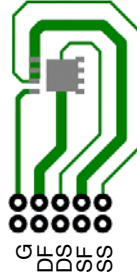
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -7.9\text{ A}$ (Note 2)	-	-0.81	-1.3	V
		$V_{GS} = 0\text{ V}, I_S = -2\text{ A}$ (Note 2)	-	-0.75	-1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = -7.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	63	102	ns
$Q_{rr}$	Reverse Recovery Charge		-	132	210	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b)  $50^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- Starting  $T_J = 25^\circ\text{C}$ ; P-ch:  $L = 3\text{ mH}$ ,  $I_{AS} = -18\text{ A}$ ,  $V_{DD} = -100\text{ V}$ ,  $V_{GS} = -10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = -58\text{ A}$ .
- Pulse Id refers to Figure 11. Forward Bias Safe Operation Area.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

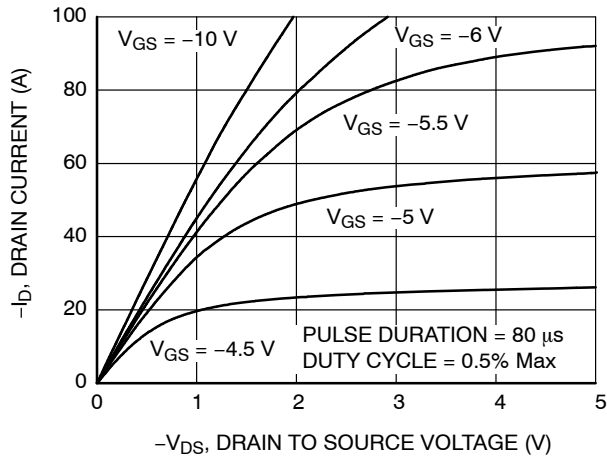


Figure 1. On Region Characteristics

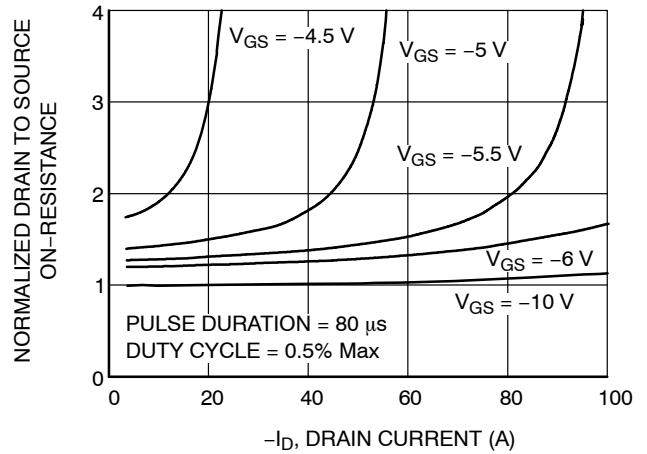


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

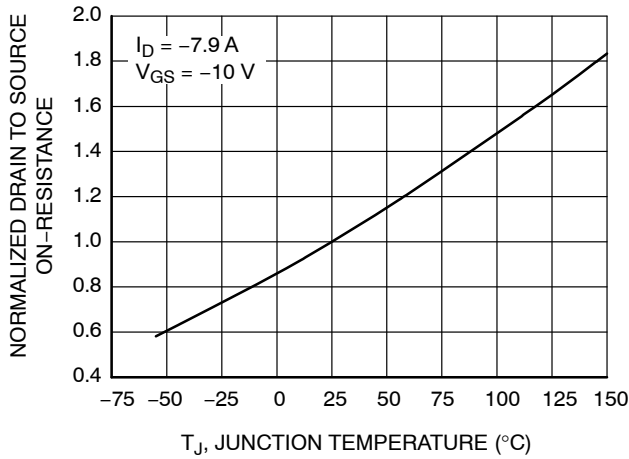


Figure 3. Normalized On Resistance vs. Junction Temperature

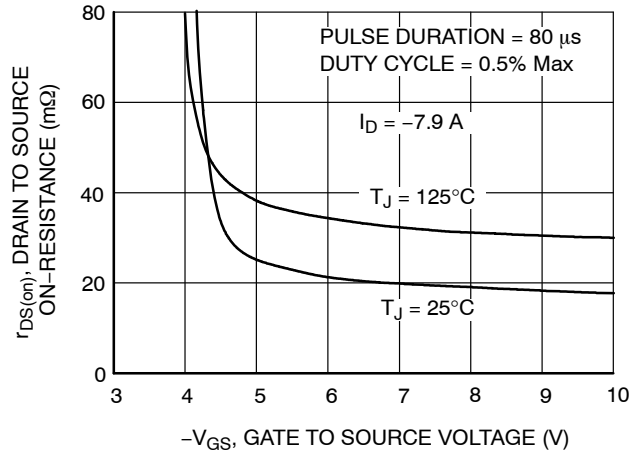


Figure 4. On-Resistance vs. Gate to Source Voltage

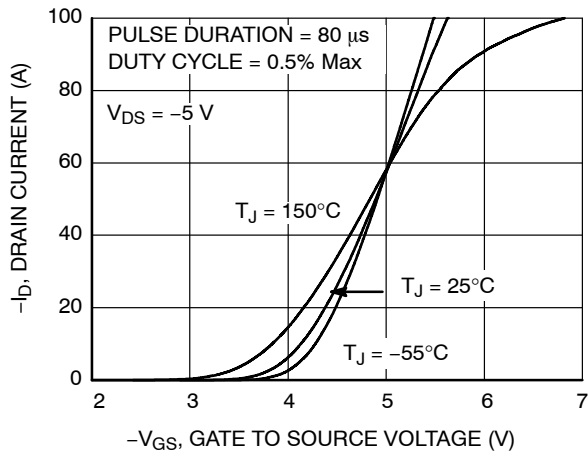


Figure 5. Transfer Characteristics

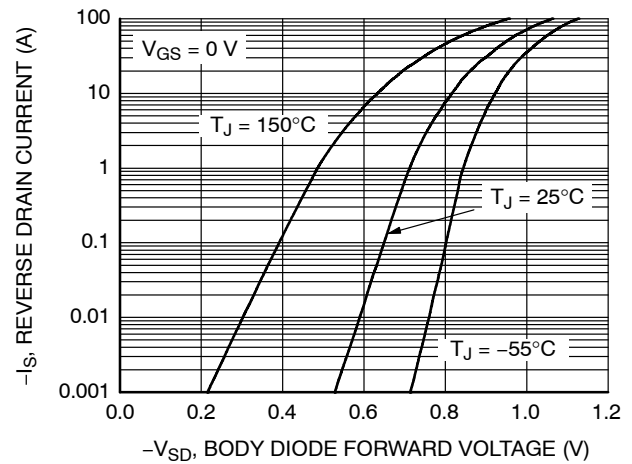


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

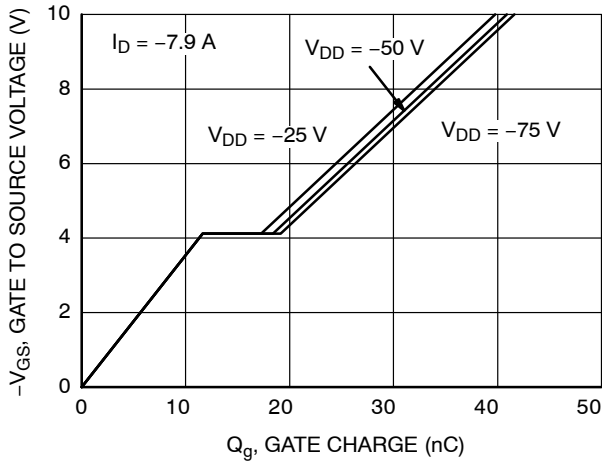


Figure 7. Gate Charge Characteristics

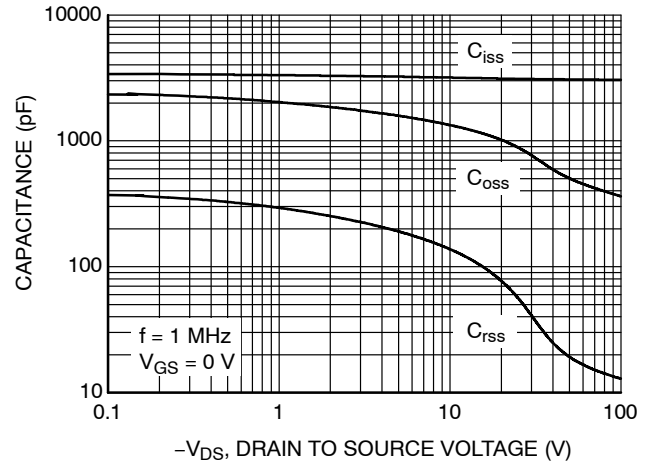


Figure 8. Capacitance vs. Drain to Source Voltage

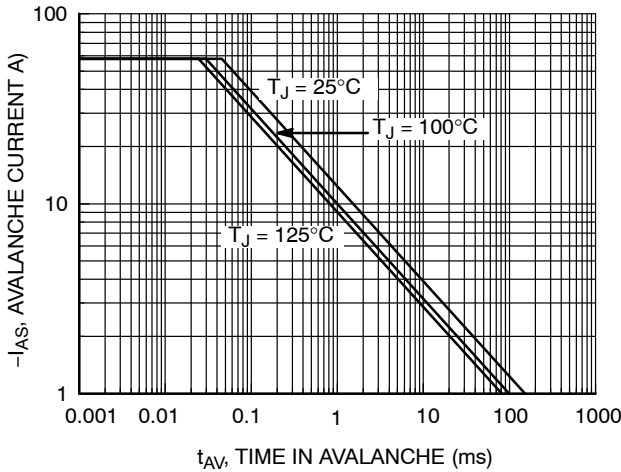


Figure 9. Unclamped Inductive Switching Capability

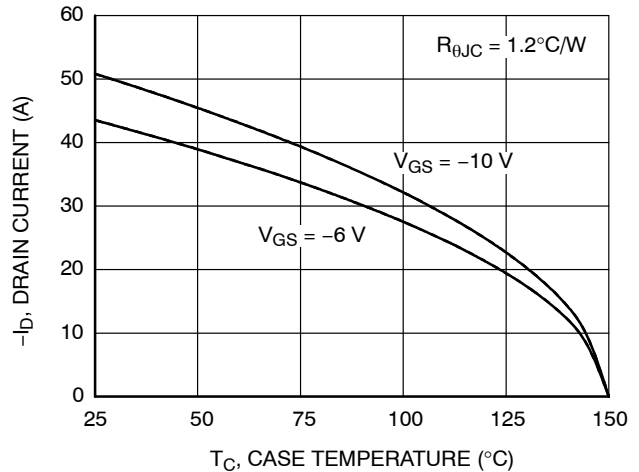


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

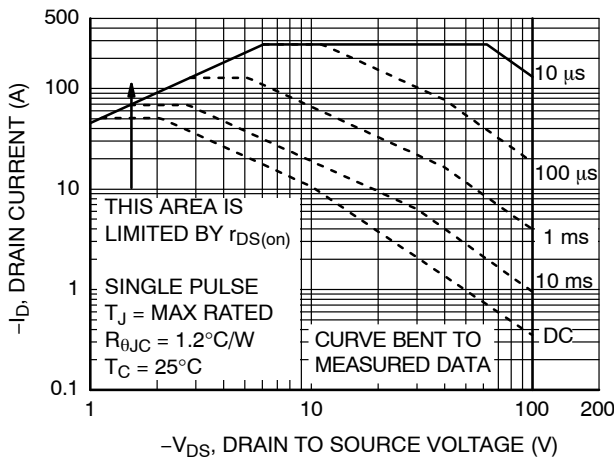


Figure 11. Forward Bias Safe Operating Area

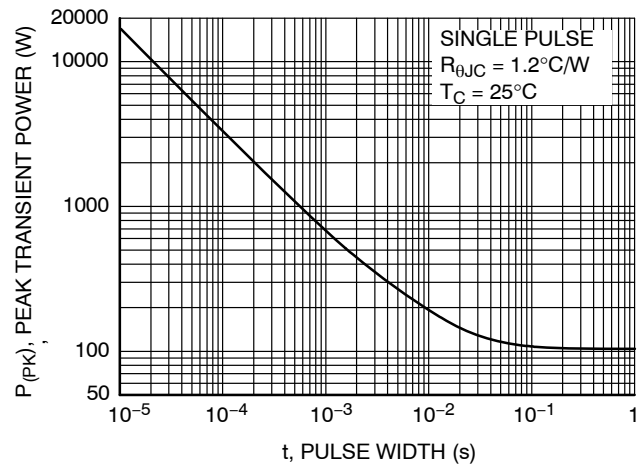


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

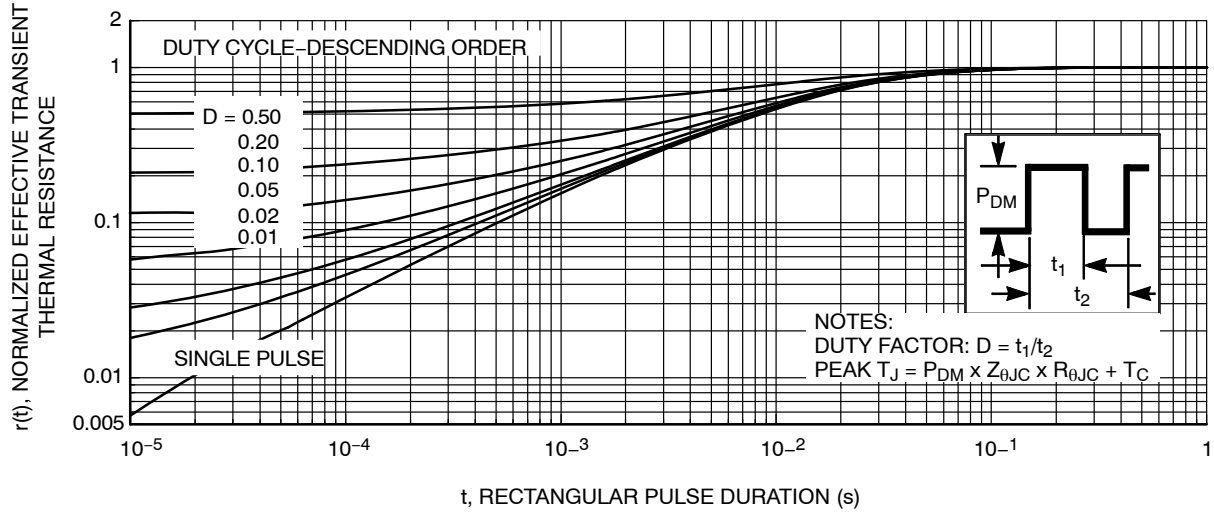


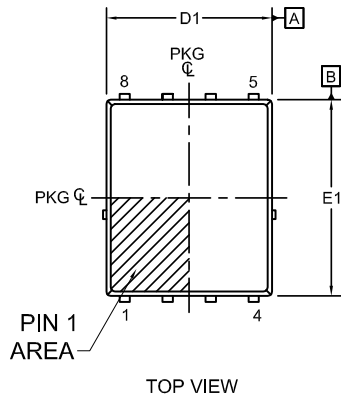
Figure 13. Junction-to-Case Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



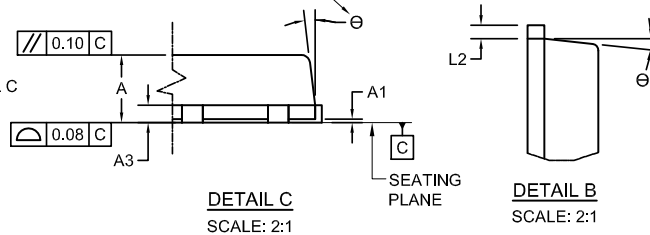
**PQFN8 5X6, 1.27P**  
CASE 483AE  
ISSUE C

DATE 21 JAN 2022

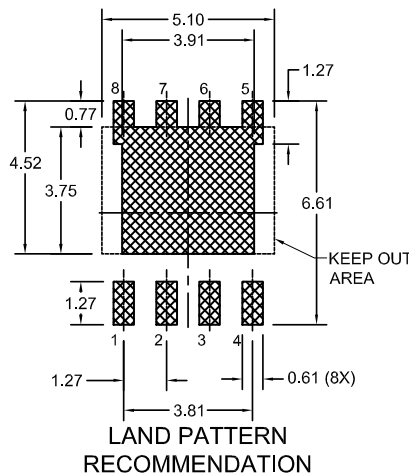
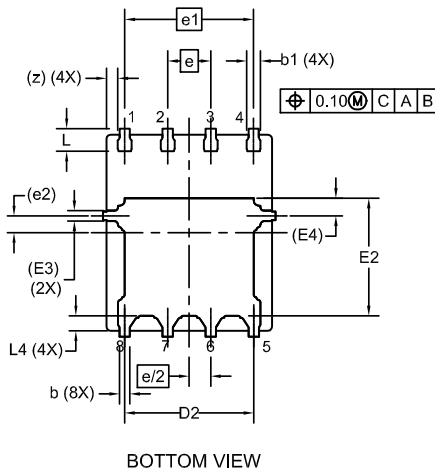


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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