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FDMC8554

N-Channel Power Trench[®] MOSFET

20V, 16.5A, 5mΩ

Features

- Max $r_{DS(on)}$ = 5mΩ at V_{GS} = 10V, I_D = 16.5A
- Max $r_{DS(on)}$ = 6.4mΩ at V_{GS} = 4.5V, I_D = 14A
- Low Profile - 1mm max in Power 33
- RoHS Compliant

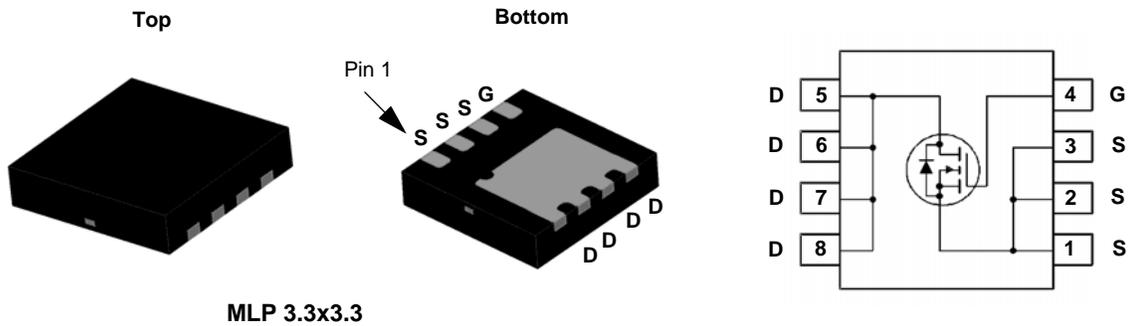


General Description

This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced Power Trench process. It has been optimized for power management applications.

Application

- DC - DC Conversion



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous	$T_C = 25^\circ\text{C}$	A
	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	
	-Pulsed		
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	W
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8554	FDMC8554	Power 33	7"	8mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		15.7		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$			1 100	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-6.1		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 16.5\text{A}$		3.6	5.0	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 14\text{A}$		4.6	6.4	
		$V_{GS} = 10\text{V}, I_D = 16.5\text{A}, T_J = 125^\circ\text{C}$		5.4	7.1	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 16.5\text{A}$		62		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		2540	3380	pF
C_{oss}	Output Capacitance			795	1060	pF
C_{rss}	Reverse Transfer Capacitance			510	765	pF
R_g	Gate Resistance		$f = 1\text{MHz}$		1.2	

Switching Characteristics

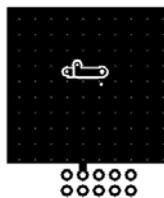
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{V}, I_D = 16.5\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		13	24	ns
t_r	Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			32	51	ns
t_f	Fall Time			7	14	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{DD} = 10\text{V}, I_D = 16.5\text{A}$		44	62	nC
$Q_{g(TOT)}$	Total Gate Charge at 4.5V			24	34	nC
Q_{gs}	Gate to Source Gate Charge			8.5		nC
Q_{gd}	Gate to Drain "Miller" Charge			10		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 16.5\text{A}$ (Note 2)		0.8	1.3	V
t_{rr}	Reverse Recovery Time	$I_F = 16.5\text{A}, di/dt = 100\text{A}/\mu\text{s}$		31	47	ns
Q_{rr}	Reverse Recovery Charge			22	33	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $60^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

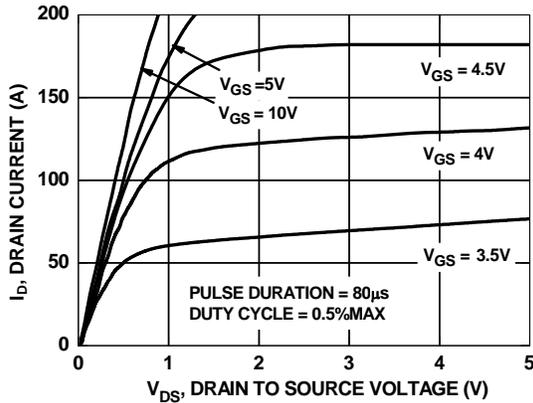


Figure 1. On-Region Characteristics

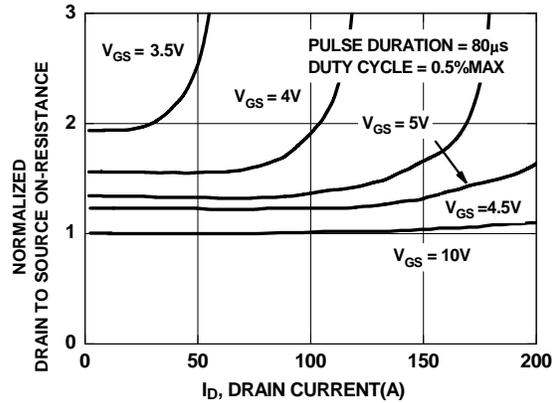


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

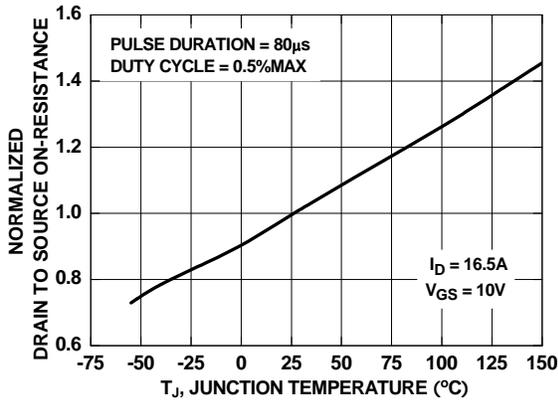


Figure 3. Normalized On-Resistance vs Junction Temperature

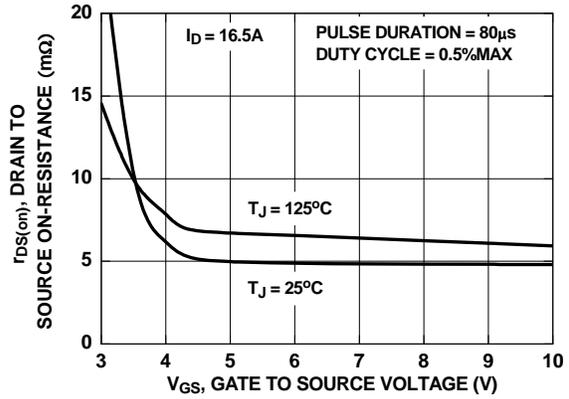


Figure 4. On-Resistance vs Gate to Source Voltage

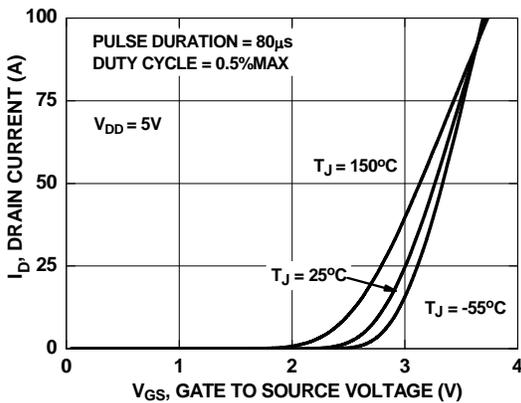


Figure 5. Transfer Characteristics

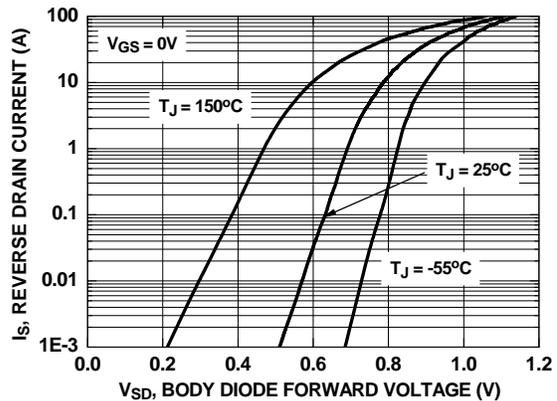


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

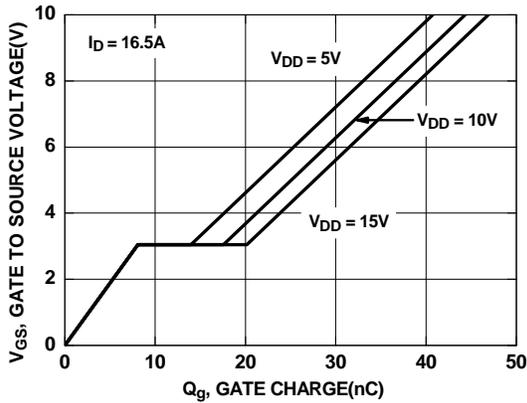


Figure 7. Gate Charge Characteristics

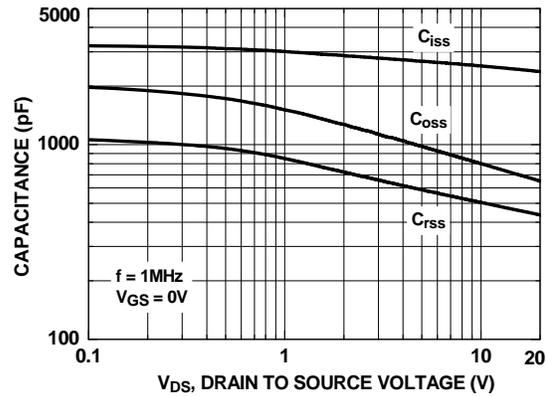


Figure 8. Capacitance vs Drain to Source Voltage

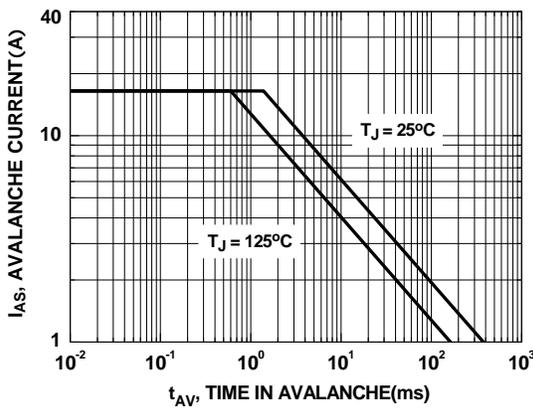


Figure 9. Unclamped Inductive Switching Capability

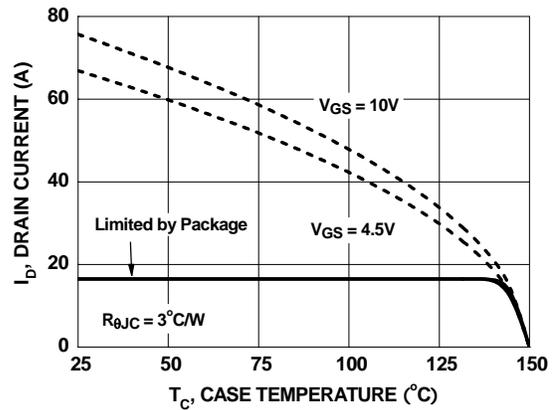


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

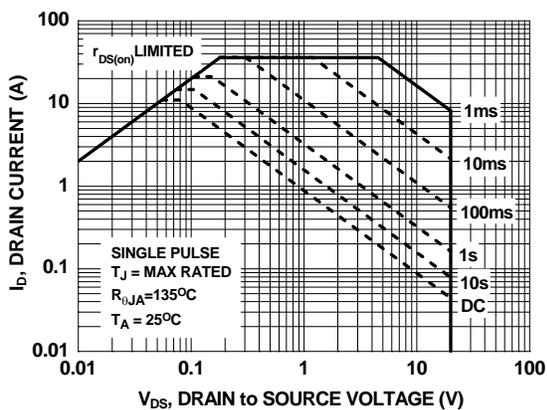


Figure 11. Forward Bias Safe Operating Area

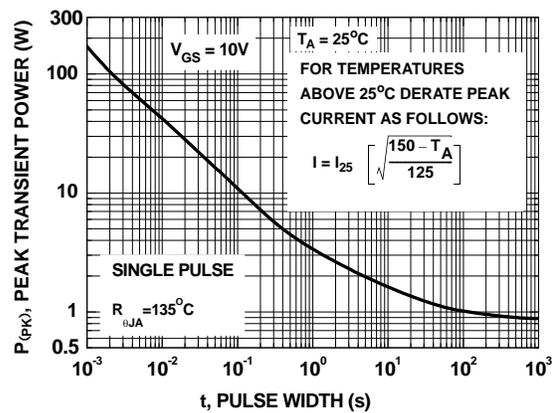


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

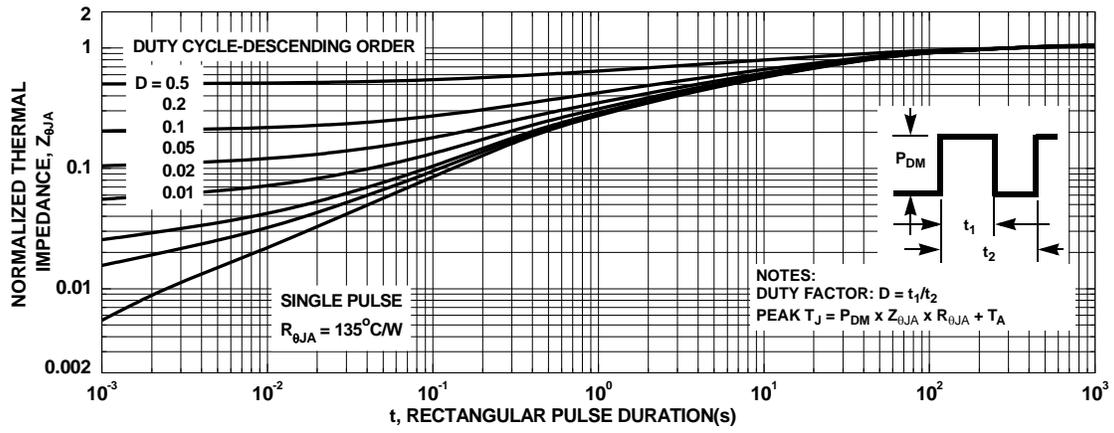
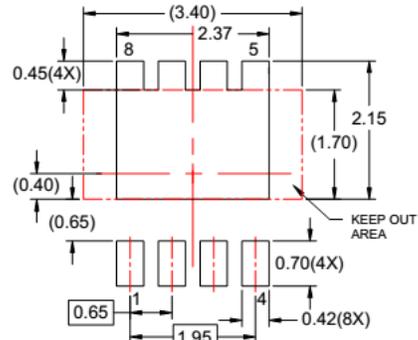
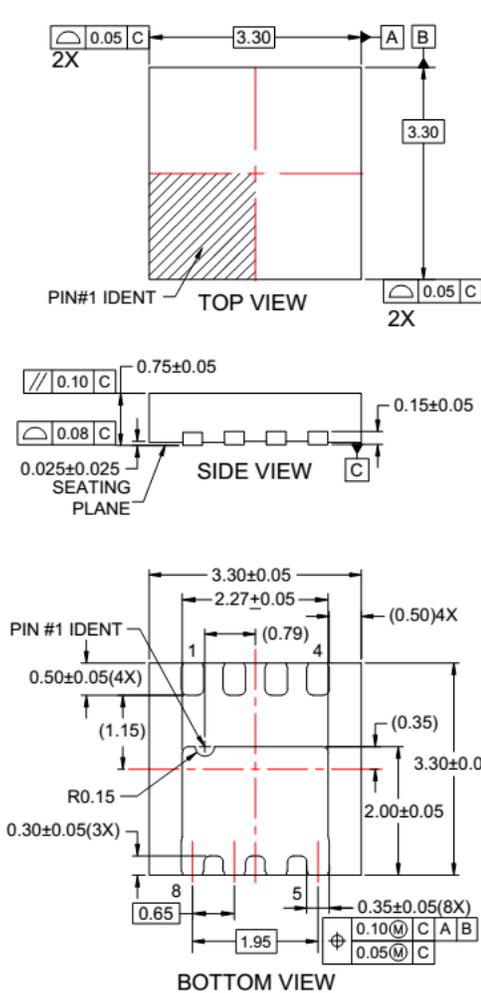


Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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