

NLHV4157N

Negative Voltage SPDT Switch

The NLHV4157N is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. The device passes analog and digital negative voltages that may vary across the full power-supply range (from V_{EE} to GND).

Features

- Operating Voltage Range: $V_{EE} = -12\text{ V}$ to -4 V
- Switch Signal Voltage Range: $V_{IS} = V_{EE}$ to GND
- Positive Control Signal Voltage: $V_{IN} = 0$ to 3.3 V
- Low ON Resistance: $R_{ON} \leq 5\ \Omega$ @ $V_{EE} = -10\text{ V}$
- Latch-up Performance Exceeds 200 mA
- Available in: SC-88 6-Pin Package
- These Devices are Pb-Free, Halogen-Free/BFR-Free and are RoHS-Compliant

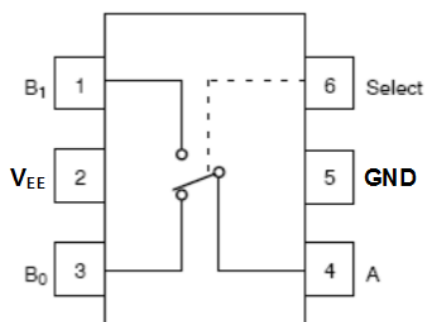


Figure 1. Pin Assignment and logic Diagram



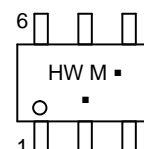
ON Semiconductor®

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MARKING DIAGRAM



**SC-88
DF SUFFIX
CASE 419B**



HW = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

FUNCTION TABLE

Select Input	Function
L	B0 Connected to A
H	B1 Connected to A

ORDERING INFORMATION

Device	Package	Shipping†
NLHV4157NDFT2G	SC-88 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS

Symbol	Rating	Value	Unit	
V_{EE}	DC Supply Voltage	-13 to +0.5	V	
V_{IS}	Analog Input Voltage (Note 1)	$V_{EE}-0.5$ to +0.5	V	
V_{IN}	Digital Select Input Voltage (Note 1)	-0.5 to +3.6	V	
I_{IOK}	Switch Input/Output diode current	± 50	mA	
I_{IK}	Select input diode current	-50	mA	
P_D	Power Dissipation in Still Air	60	mW	
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	$^{\circ}\text{C}$	
T_J	Junction Bias Under Bias	150	$^{\circ}\text{C}$	
MSL	Moisture Sensitivity	Level 1		
F_R	Flammability Rating	Oxygen Index: 30% – 35% UL94-V0 (0.125 in)	$^{\circ}\text{C}$	
I_L	Latch-up Current (Note1)	Below GND and above V_{EE} at 125 $^{\circ}\text{C}$	± 200	mA
		Below GND and above V_{EE} at 25 $^{\circ}\text{C}$	± 300	
T_s	Storage Temperature	-65 to +150	$^{\circ}\text{C}$	
θ_{JA}	Thermal Resistance	400	$^{\circ}\text{C}/\text{W}$	
ESD	ESD Protection	Human Body Model	3000	V
		Machine Model	150	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output voltage ratings may be exceeded if the input and output diode current ratings are observed.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Symbol	Parameter	Min	Max	Unit
V_{EE}	DC Supply Voltage	-12	-4	V
V_S	Switch Input / Output Voltage (B0, B1, A)	V_{EE}	GND	V
V_{IN}	Digital Select Input Voltage	GND	3.3	V
T_A	Operating Temperature Range	-55	+125	$^{\circ}\text{C}$
t_r, t_f	Input Transition Rise or Fall Time (Select Input)	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Select input must be held HIGH or LOW, it must not float.

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DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND; Typical characteristics are T_A at 25°C.)

Symbol	Parameter	Condition	V_{EE} , V	-55° to 125°C			Unit
				Min	Typ	Max	
SELECT INPUT							
V_{IH}	Minimum High-Level Input Voltage		-12	1.8		3.3	V
			-10	1.6		3.3	
			-8	1.4		3.3	
			-6	1.2		3.3	
			-4	1.0		3.3	
V_{IL}	Maximum Low-Level Input Voltage		-12	0		0.8	V
			-10	0		0.7	
			-8	0		0.6	
			-6	0		0.5	
			-4	0		0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 3.3$ V or GND	-10		±0.2	±50	μA
		$V_{IN} = 3.3$ V or GND, test at 25°C only	-10			±0.5	
POWER SUPPLY							
I_{CC}	Maximum Quiescent Supply Current	Select = 3.3 V or GND, $V_{IS} = V_{EE}$ or GND	-10 to -4		25	80	μA
ANALOG SWITCH							
R_{ON}	Maximum ON Resistance (Note 3)	$V_{IN} = V_{IL}$ or V_{IH} $V_{IS} = V_{EE}$ to GND $I_O \leq 10$ mA	-12		2.6	4.5	Ω
			-10		3.0	5	
			-8		3.5	5.8	
			-6		4.5	7.5	
		-4		9	15		
R_{FLAT}	ON Resistance Flatness (Notes 3, 4, 6)	$V_{IN} = V_{IL}$ or V_{IH} $V_{IS} = V_{EE}$ to GND $I_O \leq 10$ mA	-12		0.4		Ω
			-10		1.2		
			-8		1.7		
			-6		2.5		
		-4		6			
ΔR_{ON}	R_{ON} Mismatch Between (Notes 3, 4, 5)	$I_A = -10$ mA, $V_{Bn} = -8.4$ V	-12		0.2		Ω
		$I_A = -10$ mA, $V_{Bn} = -7$ V	-10		0.2		
		$I_A = -10$ mA, $V_{Bn} = -5.6$ V	-8		0.25		
		$I_A = -10$ mA, $V_{Bn} = -4.2$ V	-6		0.25		
		$I_A = -5$ mA, $V_{Bn} = -2.8$ V	-4		0.3		
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC or NO OFF Leakage Current (Figure 9)	$V_{IN} = V_{IL}$ or V_{IH} , $V_{Bn} = GND$, $V_A = V_{EE}$ to GND	-10		±1.0	±20	μA
$I_{COM(ON)}$	COM ON Leakage Current (Figure 9)	$V_{IN} = V_{IL}$ or V_{IH} ; $V_A = GND$ V or V_{EE} ; $V_{B1} = GND$ or V_{EE} with V_{B0} floating, or $V_{B0} = GND$ or V_{EE} with V_{B1} floating	-10		±2.0	±20	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
4. Parameter is characterized but not tested in production.
5. $\Delta R_{ON} = R_{ONmax} - R_{ONmin}$ measured at identical V_{EE} , temperature and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of ON Resistance over the specified range of conditions.

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AC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND; Typical characteristics are T_A at 25°C.)

Symbol	Parameter	Condition	V_{EE} , V	-55° to 125°C			Unit
				Min	Typ	Max	
t_{PHL} , t_{PLH}	Propagation Delay, Bus to Bus (Note 8) (A to B_n)	$C_L = 100$ pF (Figures 2, 3)	-12 to -4			2	ns
t_{PZL} , t_{PZH}	Switch Enable Time Turn-On Time (A to B_n)	$C_L = 100$ pF (Figures 2, 3)	-12			220	ns
			-10			175	
			-8			165	
			-6			165	
			-4			200	
t_{PLZ} , t_{PHZ}	Switch Disable Time Turn-Off Time (A to B_n)	$C_L = 100$ pF (Figures 2, 3)	-12			225	ns
			-10			155	
			-8			150	
			-6			120	
			-4			145	
t_B	Switch Break Time	$R_L = 50$ Ω , $C_L = 100$ pF, $V_{IS} = -2.5$ V (Figure 4)	-12	5		60	ns
			-10	5		60	
			-8	10		75	
			-6	10		90	
			-4	40		135	
t_{POR}	Power ON Reset Time	Measured from $V_{EE} = -4$ V	-12 to -4			20	μ s
Q	Charge Injection (Note 7)	$C_L = 1$ nF, $V_{GEN} = 0$ V, $R_{GEN} = 0$ Ω (Figure 5)	-12			170	pC
			-10			120	
			-8			95	
			-6			55	
			-4			40	
OIRR	Off-Isolation (Note 9)	$R_L = 50$ Ω , $f = 10$ MHz (Figure 6)	-12 to -4		-33		dB
Xtalk	Crosstalk	$R_L = 50$ Ω , $f = 10$ MHz (Figure 7)	-12 to -4		-42		dB
BW	-3 dB Bandwidth	$R_L = 50$ Ω (Figure 10)	-12 to -4		200		MHz

7. Guaranteed by Design.

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the ON Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

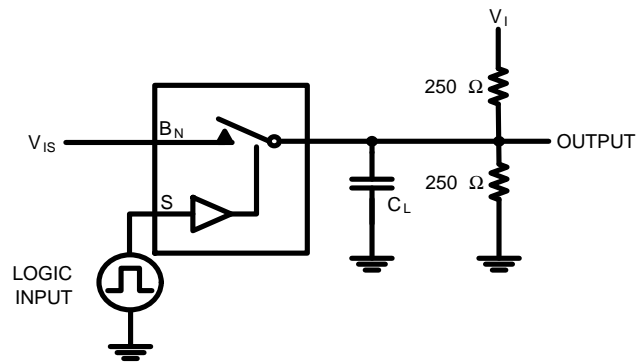
9. Off Isolation = $20 \log_{10} [V_A/V_{Bn}]$.

CAPACITANCES (Note 10)

Symbol	Parameter	Test Conditions	Typical @ 25°C	Unit
C_{IN}	Input Capacitance, Select Inputs	$V_{EE} = -12$ V	6	pF
C_{IOB}	B-Port OFF Capacitance	$V_{EE} = -10$ V	45	pF
C_{IOA_ON}	A Port Capacitance when Switch is Enabled	$V_{EE} = -10$ V	100	pF

10. $T_A = +25^\circ\text{C}$, $f = 1$ MHz, Capacitance is characterized but not tested in production.

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Note: Input V_{IS} driven by 50Ω source terminated by 50Ω .
Note: C_L includes load and stray capacitance.
 Input PRR = 100 kHz, $t_W = 5 \mu s$.

Parameter	V_I	V_{IS}
t_{PLH} / t_{PHL}	Open	Source
t_{PZL} / t_{PLZ}	GND	V_{EE}
t_{PZH} / t_{PHZ}	$2 \times V_{EE}$	GND

Figure 2. AC Test Circuit

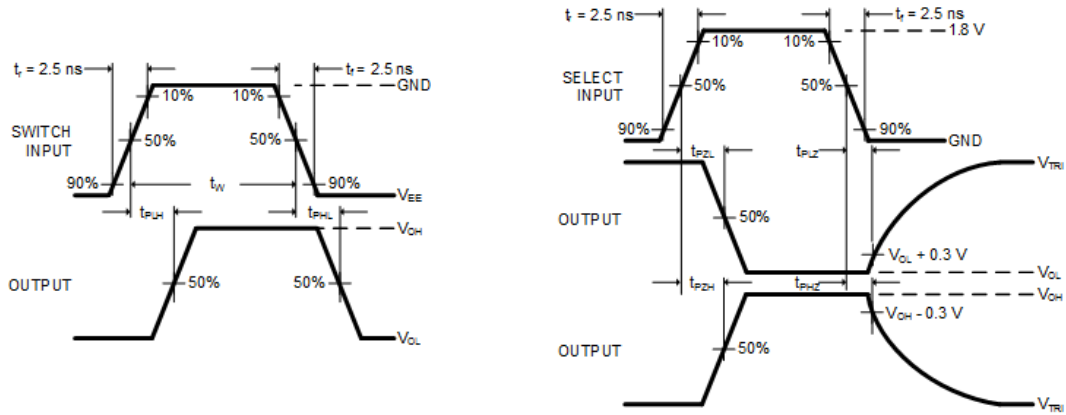


Figure 3. AC Test Waveforms

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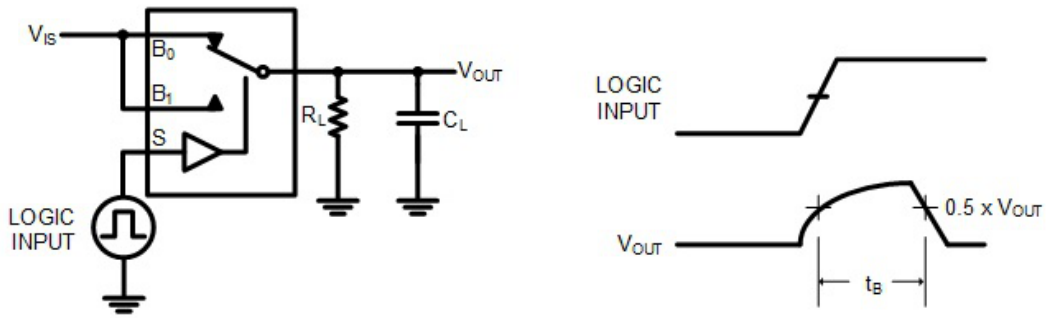


Figure 4. Switch Break Interval Timing

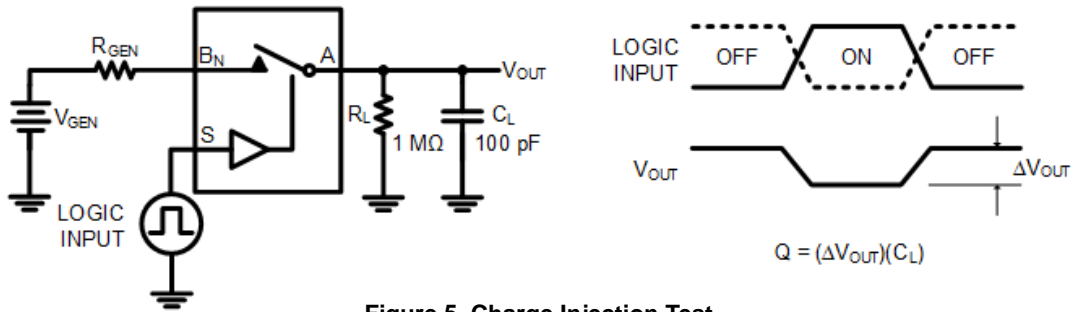


Figure 5. Charge Injection Test

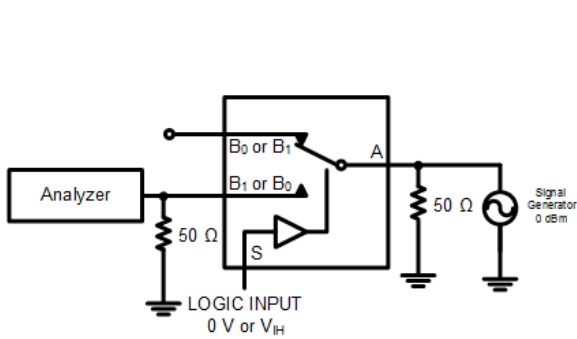


Figure 6. Off Isolation

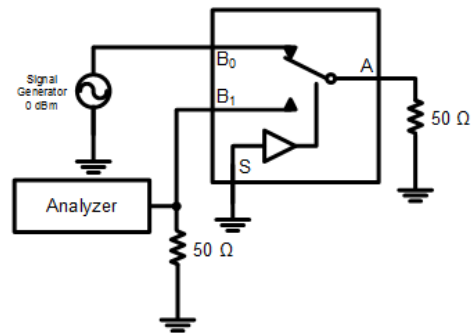


Figure 7. Crosstalk

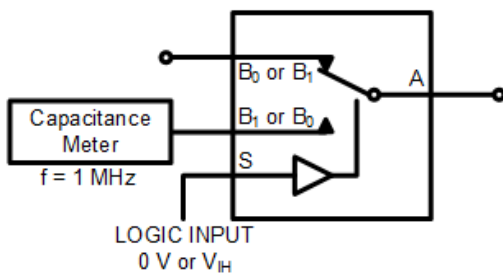


Figure 8. Channel Off Capacitance

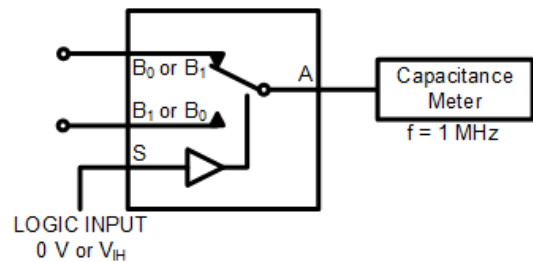
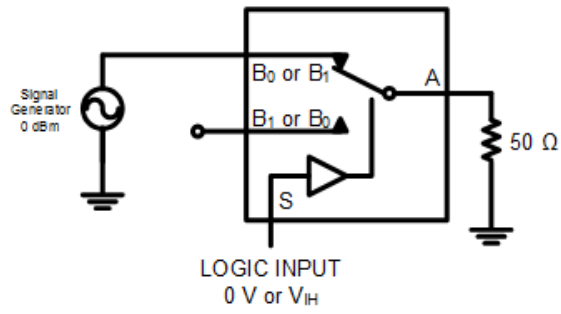


Figure 9. Channel On Capacitance

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$$BW = \frac{0.707 \cdot VA}{VBn}, \quad n = 0 \text{ or } 1$$

Figure 10. Bandwidth

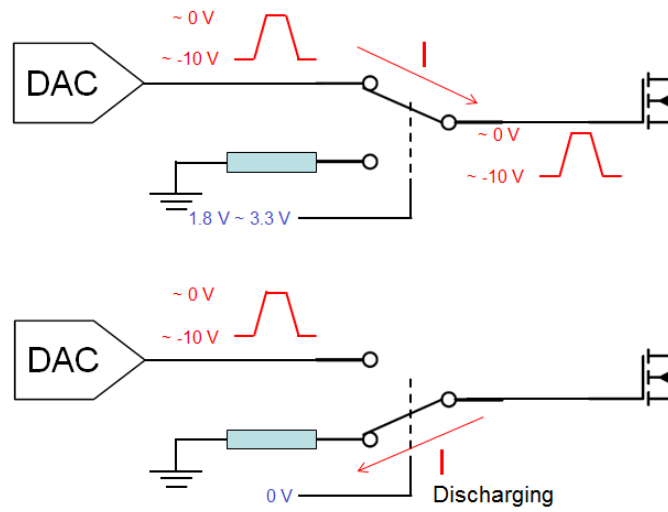


Figure 11. Typical Application

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



1
SCALE 2:1

SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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