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# FDMC007N30D

## Dual N-Channel PowerTrench<sup>®</sup> MOSFET

Q1: 30 V, 11.6 mΩ; Q2: 30 V, 6.4 mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 11.6 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 10\text{ A}$
- Max  $r_{DS(on)}$  = 13.3 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 9\text{ A}$

Q2: N-Channel

- Max  $r_{DS(on)}$  = 6.4 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 16\text{ A}$
- Max  $r_{DS(on)}$  = 7.0 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 15\text{ A}$
- RoHS Compliant

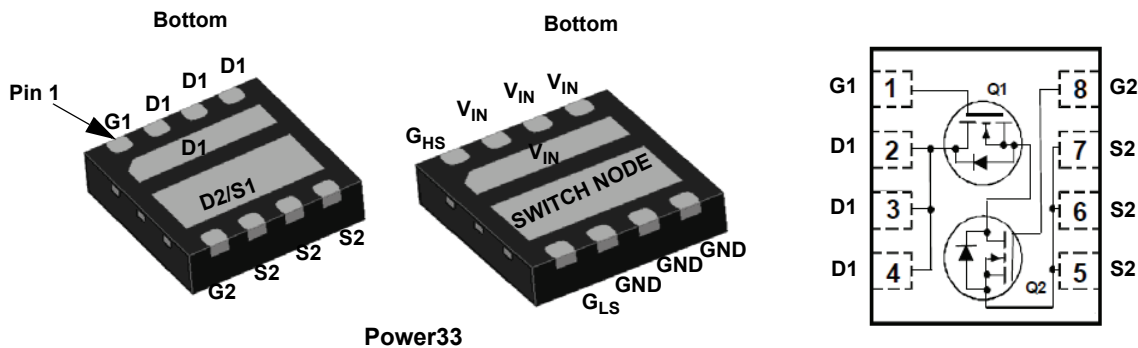


### General Description

This device includes two specialized N-Channel MOSFETs in a dual power33(3mm X 3mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

### Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	30	30	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 12$	$\pm 12$	V
$I_D$	Drain Current -Continuous $T_C = 25^\circ\text{C}$ (Note 6)	29	46	A
	-Continuous $T_C = 100^\circ\text{C}$ (Note 6)	18	29	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	10 <sup>1a</sup>	16 <sup>1b</sup>	
	-Pulsed (Note 5)	113	302	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	24	54	mJ
$P_D$	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	1.9 <sup>1a</sup>	2.5 <sup>1b</sup>	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	0.7 <sup>1c</sup>	1.0 <sup>1d</sup>	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	8.2	6.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 <sup>1a</sup>	50 <sup>1b</sup>	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	180 <sup>1c</sup>	125 <sup>1d</sup>	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7N30D	FDMC007N30D	Power 33	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$ $I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1 Q2		15 16		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	Q1 Q2			1 1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0 \text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ $V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	Q1 Q2	1.0 1.0	1.3 1.8	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1 Q2		-4 -4		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 9 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}, T_J = 125^\circ\text{C}$	Q1		7.7 8.9 10.8	11.6 13.3 16.3	m $\Omega$
		$V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}, T_J = 125^\circ\text{C}$	Q2		4.4 5.4 6.2	6.4 7.0 9.0	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 10 \text{ A}$ $V_{DD} = 5 \text{ V}, I_D = 16 \text{ A}$	Q1 Q2		46 70		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance		Q1 Q2		792 1685	1110 2360	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Q1 Q2		230 467	325 655	pF
$C_{riss}$	Reverse Transfer Capacitance		Q1 Q2		20 36	30 50	pF
$R_g$	Gate Resistance		Q1 Q2	0.1 0.1	2.0 1.2	4.0 2.4	$\Omega$

**Switching Characteristics**

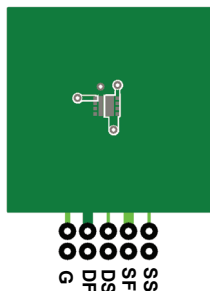
$t_{d(on)}$	Turn-On Delay Time	Q1	Q1 Q2		7 10	14 20	ns
$t_r$	Rise Time	$V_{DD} = 15 \text{ V}, I_D = 10 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2		2 3	10 10	ns
			Q2	Q1 Q2		19 24	33 39
$t_f$	Fall Time	$V_{DD} = 15 \text{ V}, I_D = 16 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2		2 3	10 10	ns
			Q1 Q2	Q1 Q2		12 24	17 34
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$	Q1 Q2		5.5 11	7.7 16	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 15 \text{ V},$ $I_D = 10 \text{ A}$	Q1 Q2		1.7 4.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		Q1 Q2		1.3 2.7		nC

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

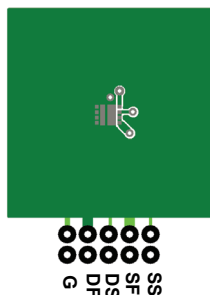
Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$ (Note 2)	Q1		0.85	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 1.5\text{ A}$ (Note 2)	Q1		0.75	1.2	
		$V_{GS} = 0\text{ V}, I_S = 16\text{ A}$ (Note 2)	Q2		0.83	1.2	
		$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)	Q2		0.73	1.2	
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		17	31	ns
$Q_{rr}$	Reverse Recovery Charge	$I_F = 16\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		5	10	nC
			Q2		10	20	

### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a.  $0.65\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b.  $0.50\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



c.  $0.180\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper



d.  $0.125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width  $< 300\ \mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. Q1:  $E_{AS}$  of 24 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 4\text{ A}$ ,  $V_{DD} = 30\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 13\text{ A}$ .

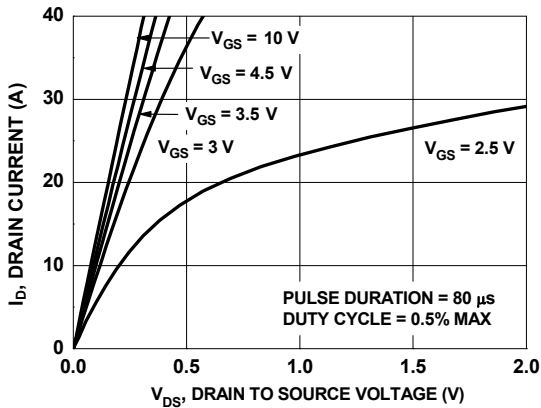
Q2:  $E_{AS}$  of 54 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 6\text{ A}$ ,  $V_{DD} = 30\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 22\text{ A}$ .

4. As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

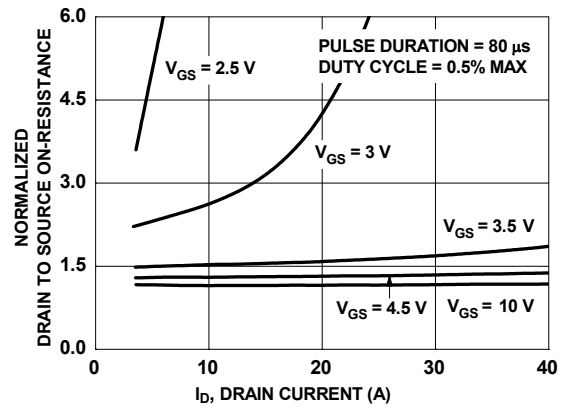
5. Pulsed  $I_d$  please refer to Fig 11 and Fig. 24 SOA graph for more details.

6. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

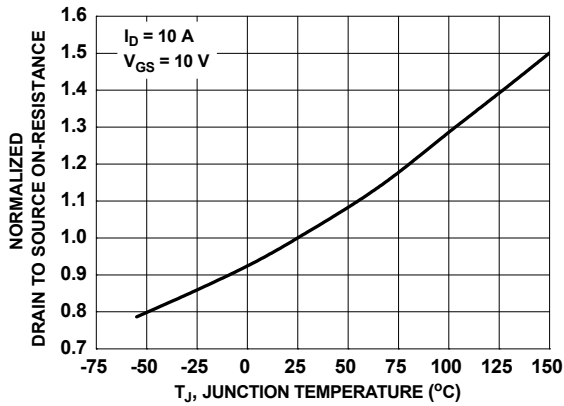
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



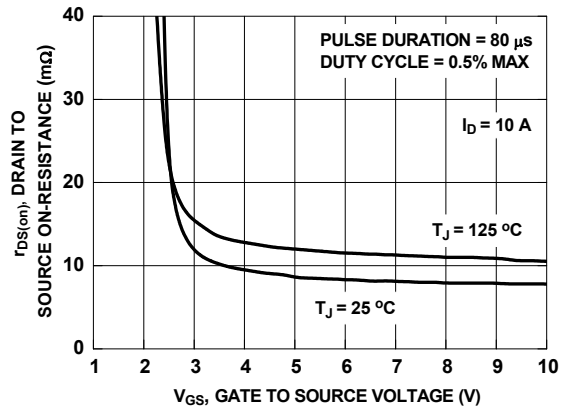
**Figure 1. On Region Characteristics**



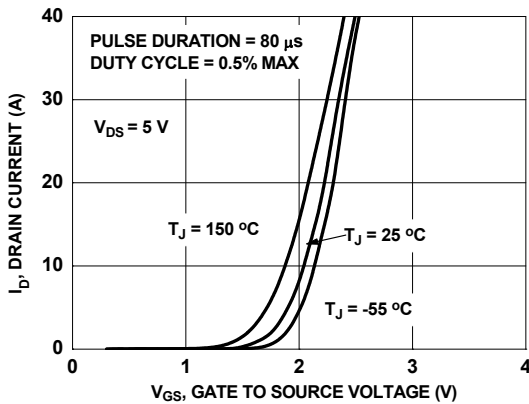
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



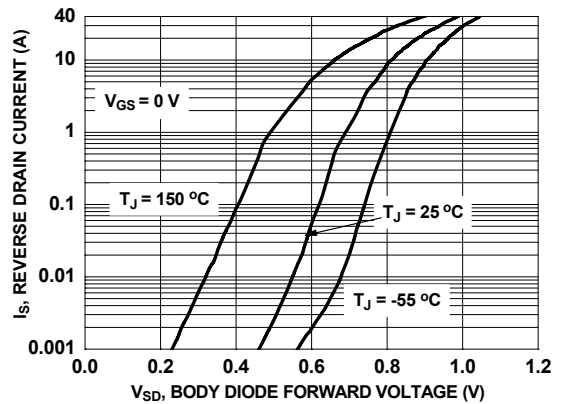
**Figure 3. Normalized On Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**

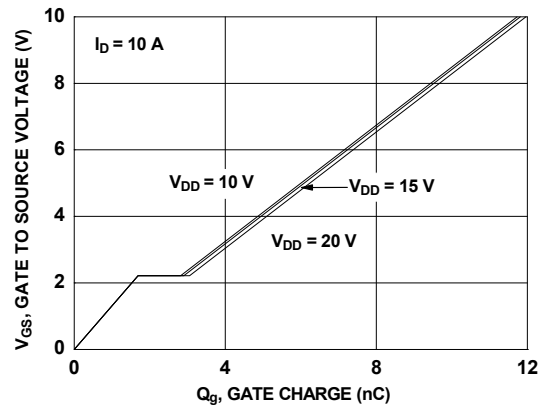


**Figure 5. Transfer Characteristics**

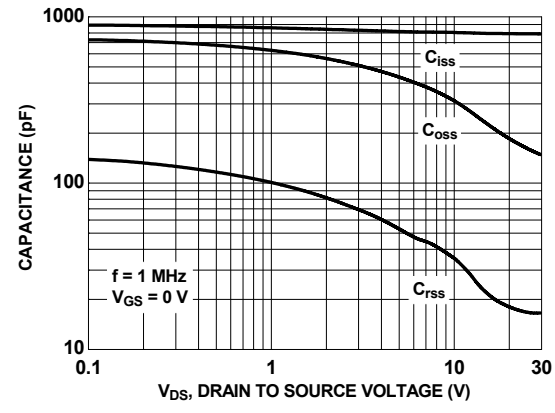


**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

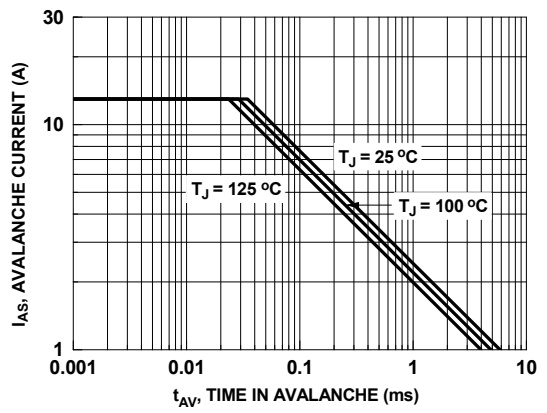
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



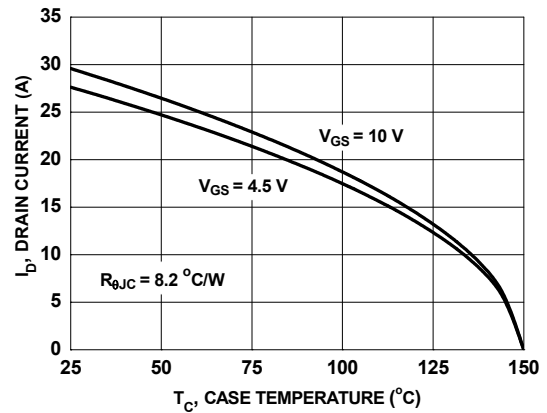
**Figure 7. Gate Charge Characteristics**



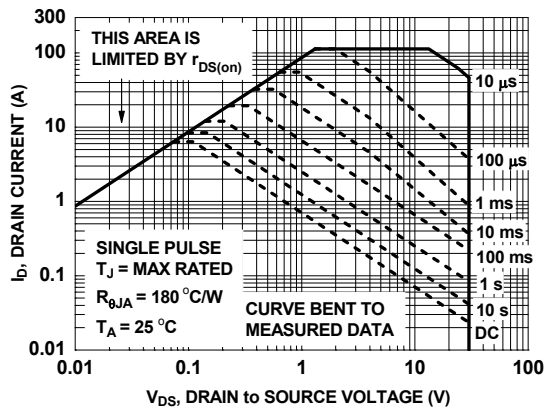
**Figure 8. Capacitance vs. Drain to Source Voltage**



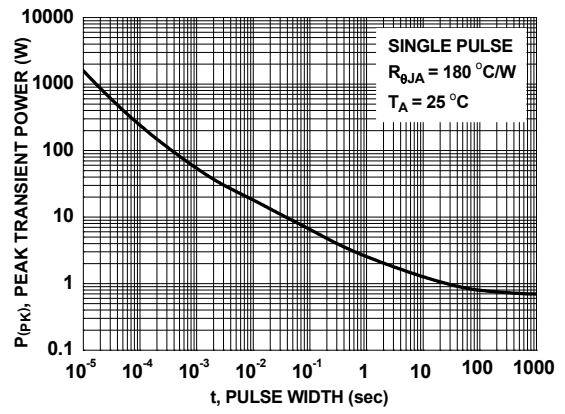
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

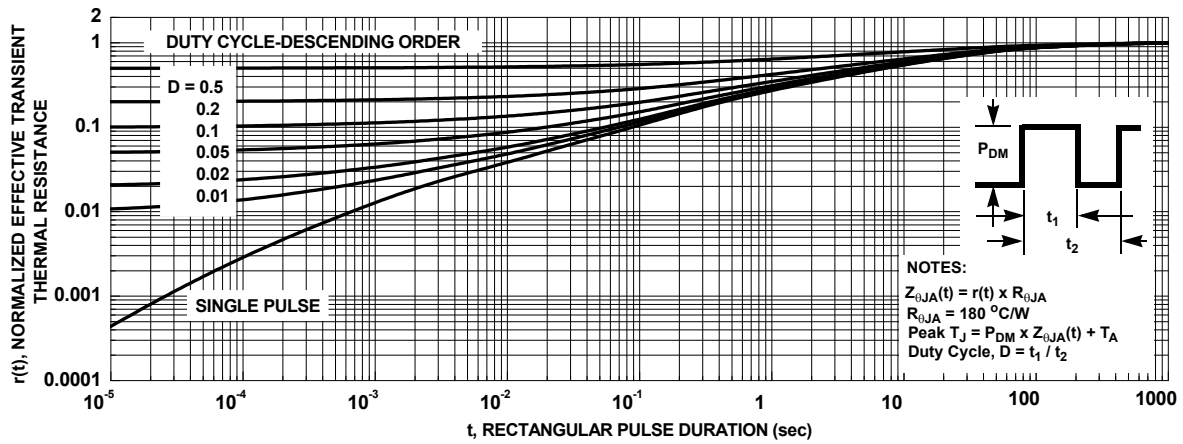


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

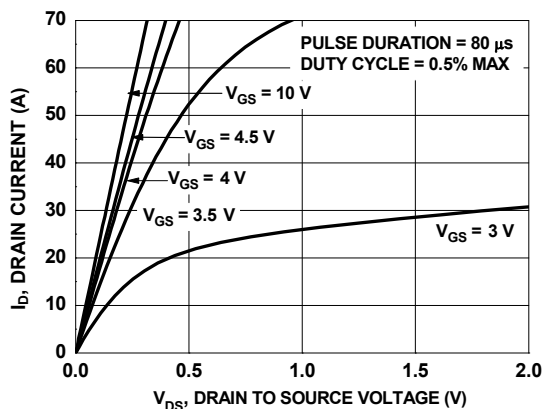


Figure 14. On-Region Characteristics

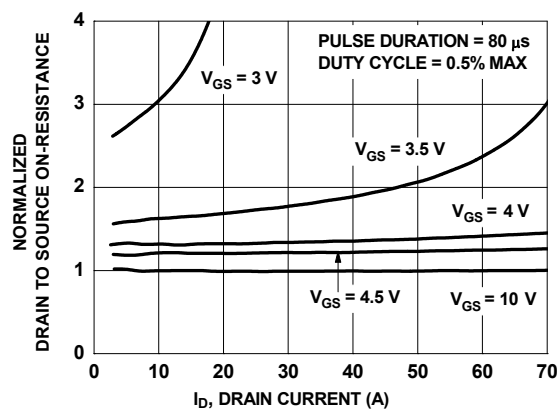


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

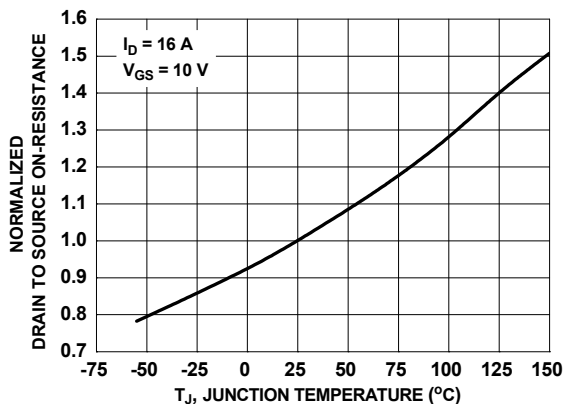


Figure 16. Normalized On-Resistance vs. Junction Temperature

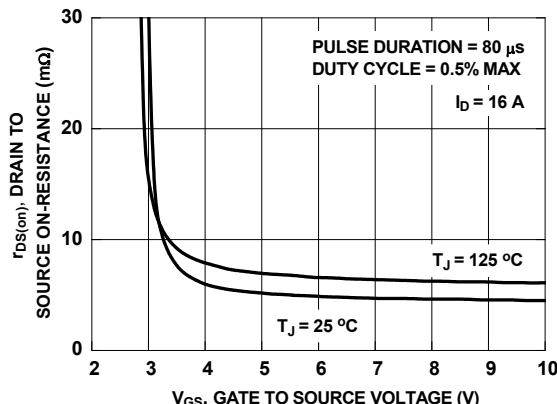


Figure 17. On-Resistance vs. Gate to Source Voltage

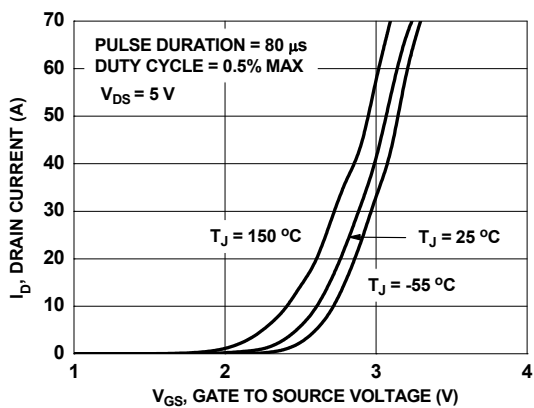


Figure 18. Transfer Characteristics

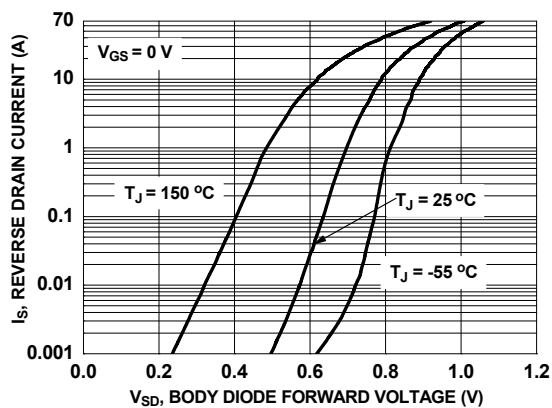
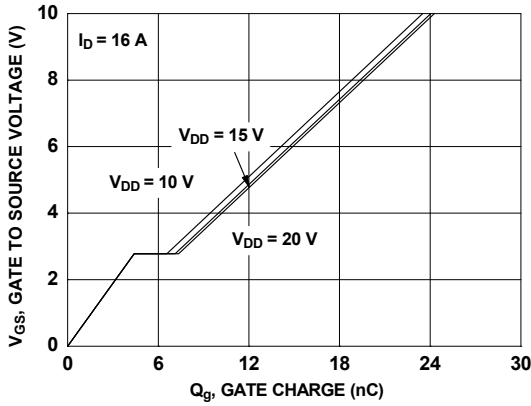


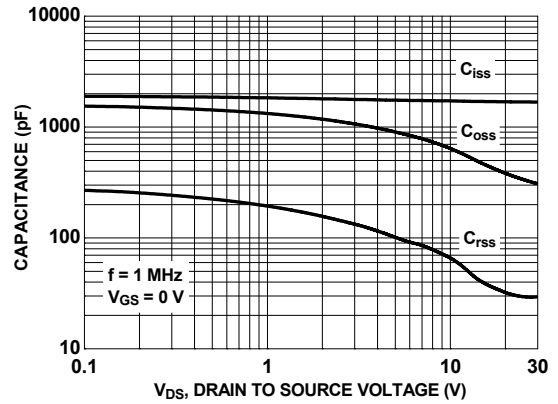
Figure 19. Source to Drain Diode Forward Voltage vs. Source Current



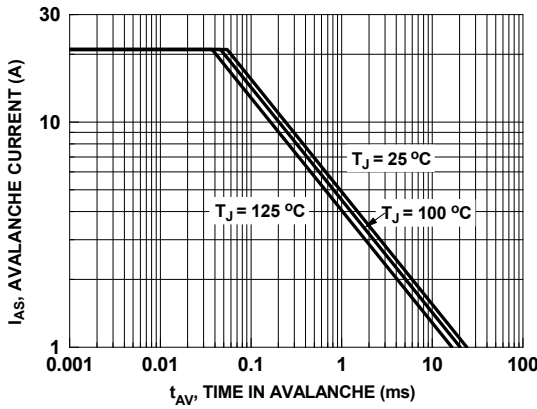
**Typical Characteristics (Q2 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



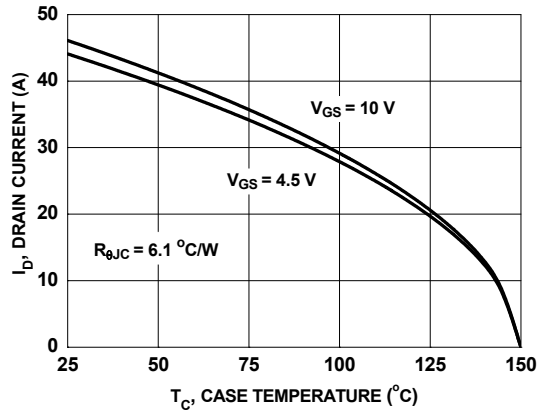
**Figure 20. Gate Charge Characteristics**



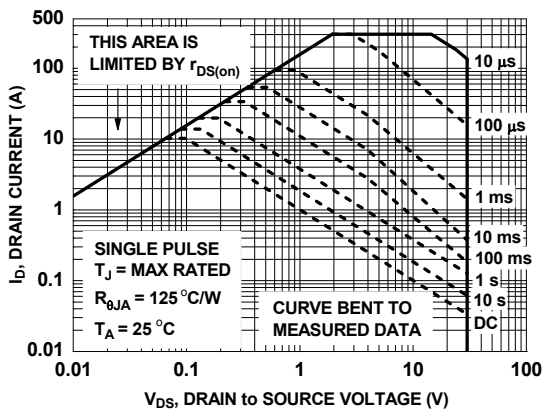
**Figure 21. Capacitance vs. Drain to Source Voltage**



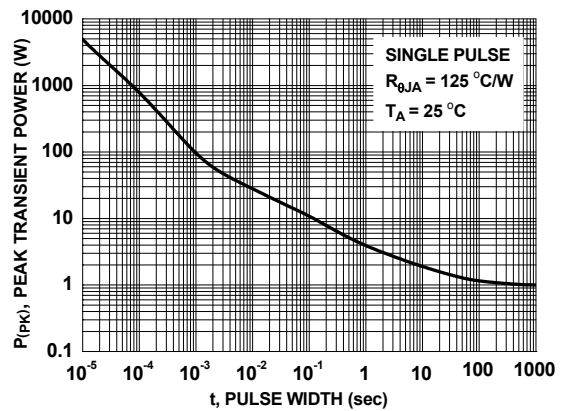
**Figure 22. Unclamped Inductive Switching Capability**



**Figure 23. Maximum Continuous Drain Current vs. Case Temperature**

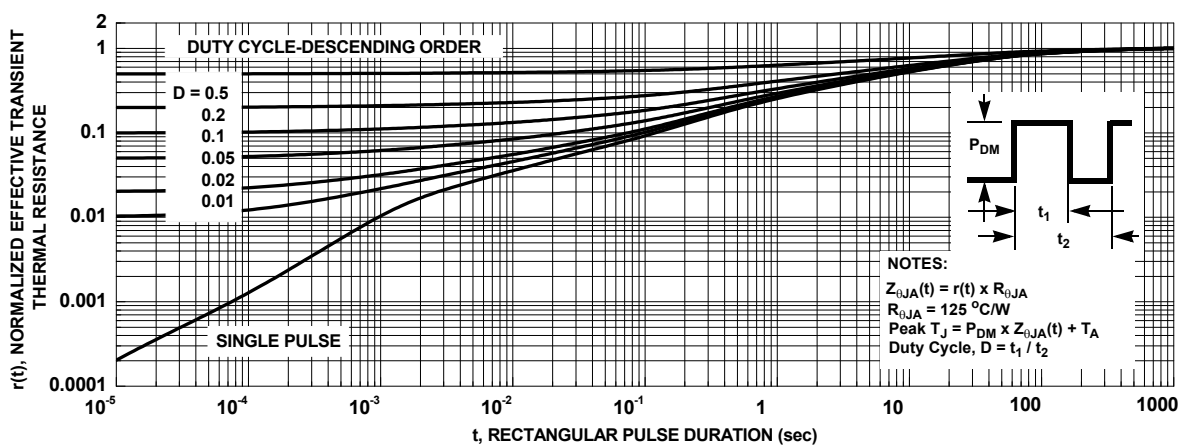


**Figure 24. Forward Bias Safe Operating Area**



**Figure 25. Single Pulse Maximum Power Dissipation**

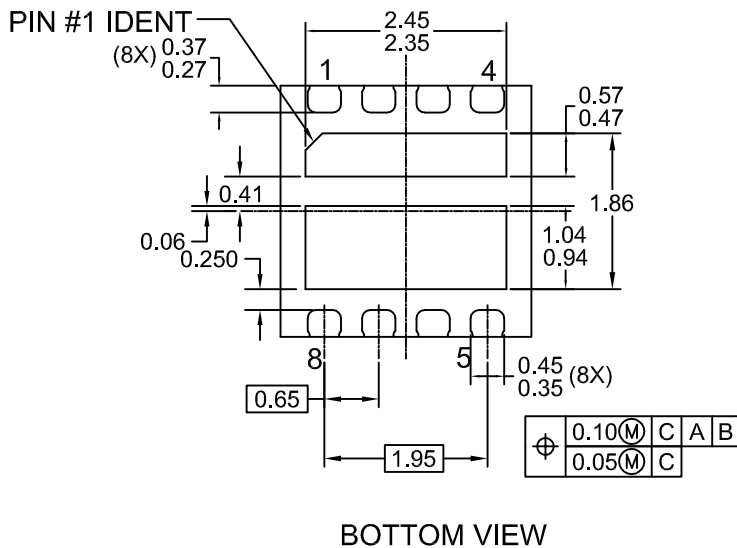
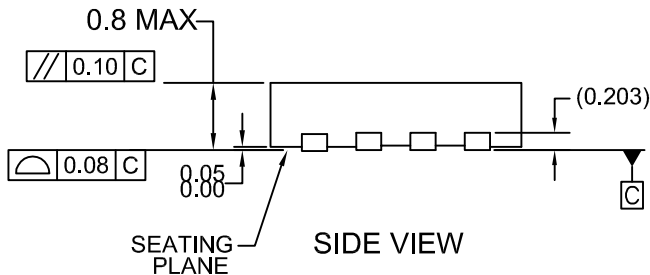
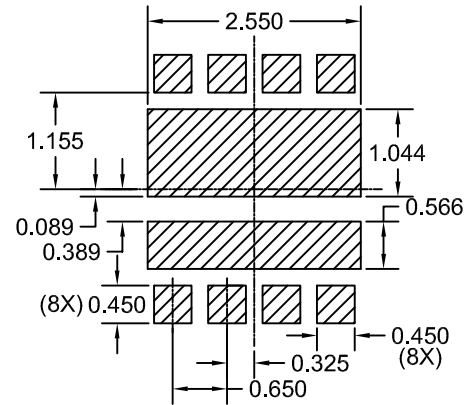
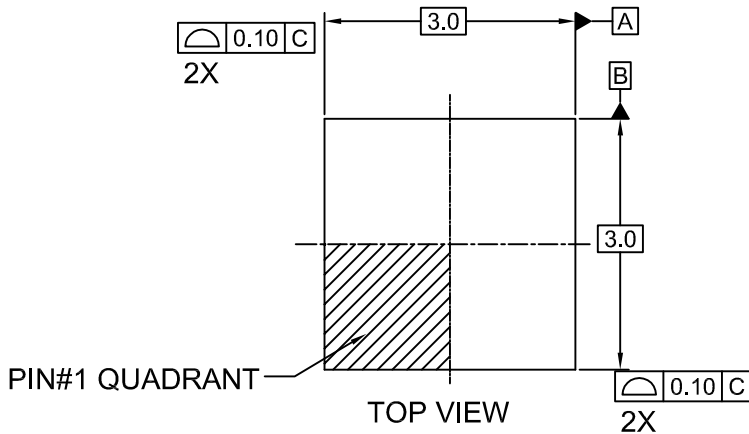
**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



**Figure 26. Junction-to-Ambient Transient Thermal Response Curve**

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