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August 2016

FDMC007N30D

Dual N-Channel PowerTrench® MOSFET
Q1:30 V, 11.6 mΩ; Q2: 30 V, 6.4 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 11.6 mΩ at V_{GS} = 10 V, I_D = 10 A
- Max $r_{DS(on)}$ = 13.3 mΩ at V_{GS} = 4.5 V, I_D = 9 A

Q2: N-Channel

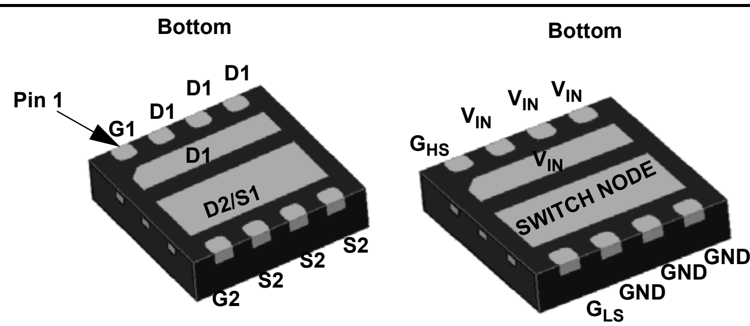
- Max $r_{DS(on)}$ = 6.4 mΩ at V_{GS} = 10 V, I_D = 16 A
- Max $r_{DS(on)}$ = 7.0 mΩ at V_{GS} = 4.5 V, I_D = 15 A
- RoHS Compliant

General Description

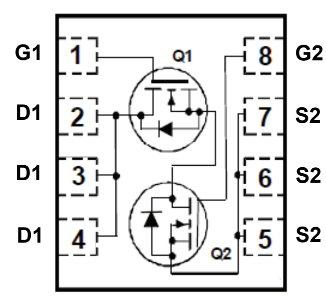
This device includes two specialized N-Channel MOSFETs in a dual power33(3mm X 3mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load



Power33



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			Q1	Q2	Units
V_{DS}	Drain to Source Voltage			30	30	V
V_{GS}	Gate to Source Voltage		(Note 4)	±12	±12	V
I_D	Drain Current -Continuous	T_C = 25 °C	(Note 6)	29	46	A
	-Continuous	T_C = 100 °C	(Note 6)	18	29	
	-Continuous	T_A = 25 °C	(Note 1a)	10 1a	16 1b	
	-Pulsed		(Note 5)	113	302	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	24	54	mJ
P_D	Power Dissipation for Single Operation	T_A = 25°C		1.9 1a	2.5 1b	W
	Power Dissipation for Single Operation	T_A = 25°C		0.7 1c	1.0 1d	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150		°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	8.2	6.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 1a	50 1b	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	180 1c	125 1d	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7N30D	FDMC007N30D	Power 33	13”	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 250 μA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 250 μA, referenced to 25°C	Q1 Q2		15 16		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA nA

On Characteristics

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 250 μA	Q1 Q2	1.0 1.0	1.3 1.8	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 250 μA, referenced to 25°C	Q1 Q2		-4 -4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 10 A V_{GS} = 4.5 V, I_D = 9 A V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	Q1		7.7 8.9 10.8	11.6 13.3 16.3	mΩ
		V_{GS} = 10 V, I_D = 16 A V_{GS} = 4.5 V, I_D = 15 A V_{GS} = 10 V, I_D = 16 A, T_J = 125°C	Q2		4.4 5.4 6.2	6.4 7.0 9.0	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 10 A V_{DD} = 5 V, I_D = 16 A	Q1 Q2		46 70		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		792 1685	1110 2360	pF
C_{oss}	Output Capacitance		Q1 Q2		230 467	325 655	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		20 36	30 50	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	2.0 1.2	4.0 2.4	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 15 V, I_D = 10 A, V_{GS} = 10 V, R_{GEN} = 6 Ω Q2 V_{DD} = 15 V, I_D = 16 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	Q1 Q2		7 10	14 20	ns
t_r	Rise Time		Q1 Q2		2 3	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		19 24	33 39	ns
t_f	Fall Time		Q1 Q2		2 3	10 10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; Q1 V_{DD} = 15 V, I_D = 10 A; Q2 V_{DD} = 15 V, I_D = 16 A	Q1 Q2		12 24	17 34	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V	Q1 Q2		5.5 11	7.7 16	nC
Q_{gs}	Gate to Source Charge		Q1 Q2		1.7 4.4		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		1.3 2.7		nC

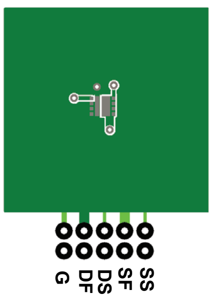
Electrical Characteristics T_J = 25°C unless otherwise noted.

Drain-Source Diode Characteristics

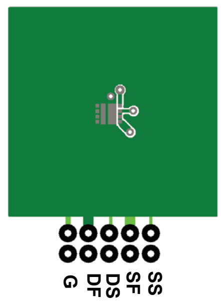
Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 10 A (Note 2)	Q1		0.85	1.2	V
		V_{GS} = 0 V, I_S = 1.5 A (Note 2)	Q1		0.75	1.2	
		V_{GS} = 0 V, I_S = 16 A (Note 2)	Q2		0.83	1.2	
		V_{GS} = 0 V, I_S = 2 A (Note 2)	Q2		0.73	1.2	
t_{rr}	Reverse Recovery Time	Q1: I_F = 10 A, di/dt = 100 A/µs	Q1		17	31	ns
		Q2: I_F = 16 A, di/dt = 100 A/µs	Q2		27	42	
Q_{rr}	Reverse Recovery Charge	Q1: I_F = 10 A, di/dt = 100 A/µs	Q1		5	10	nC
		Q2: I_F = 16 A, di/dt = 100 A/µs	Q2		10	20	

Notes:

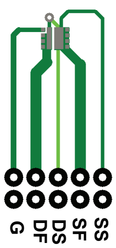
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



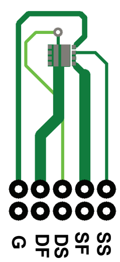
a.65 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b.50 °C/W when mounted on a 1 in^2 pad of 2 oz copper



c. 180 °C/W when mounted on a minimum pad of 2 oz copper



d. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
3. Q1: E_{AS} of 24 mJ is based on starting T_J = 25 ^oC, L = 3 mH, I_{AS} = 4 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 13 A.
   Q2: E_{AS} of 54 mJ is based on starting T_J = 25 ^oC, L = 3 mH, I_{AS} = 6 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 22 A.
4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.
5. Pulsed Id please refer to Fig 11 and Fig. 24 SOA graph for more details.
6. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

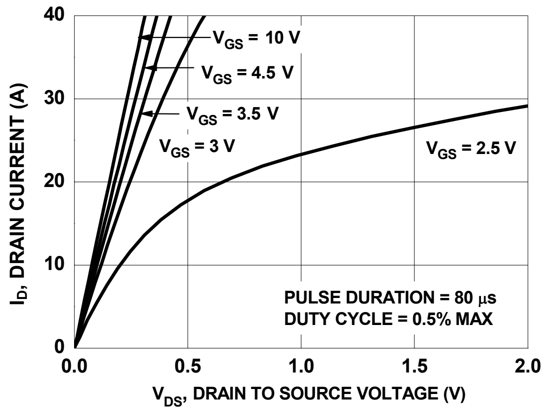


Figure 1. On Region Characteristics

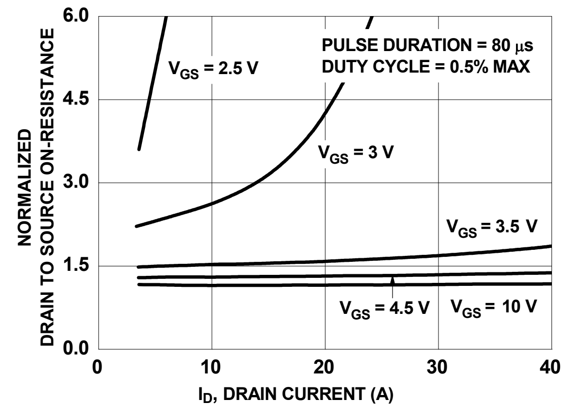


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

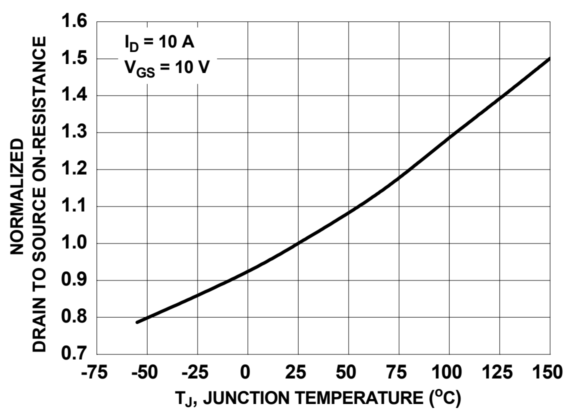


Figure 3. Normalized On Resistance vs. Junction Temperature

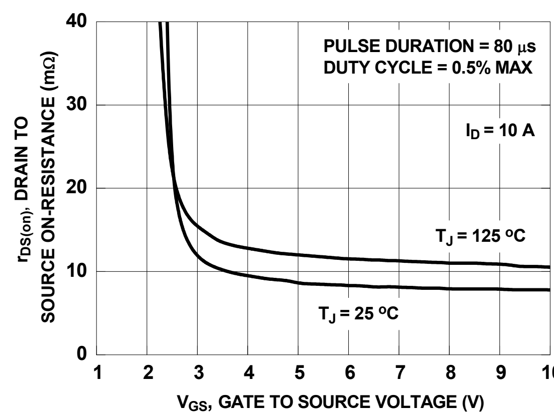


Figure 4. On-Resistance vs. Gate to Source Voltage

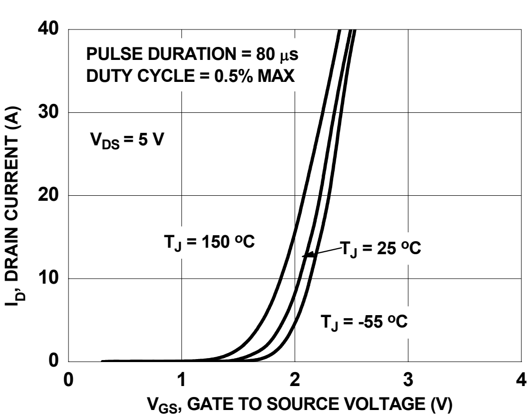


Figure 5. Transfer Characteristics

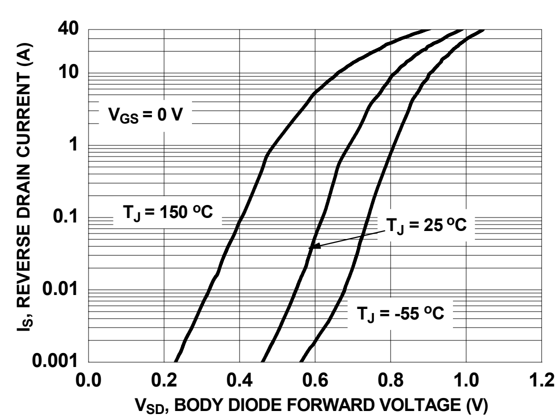


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

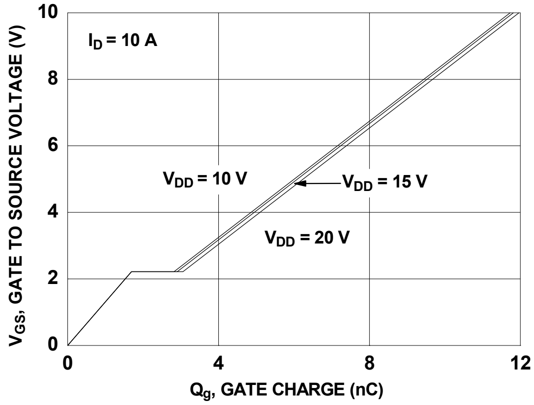


Figure 7. Gate Charge Characteristics

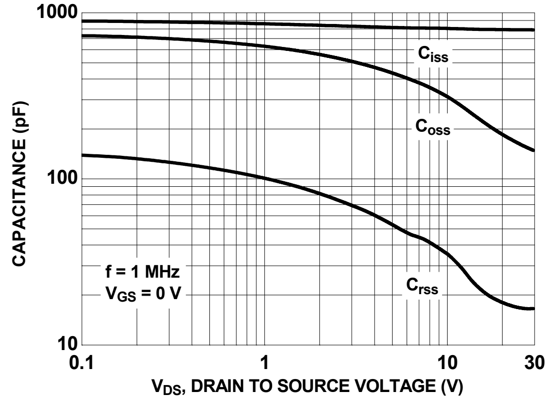


Figure 8. Capacitance vs. Drain to Source Voltage

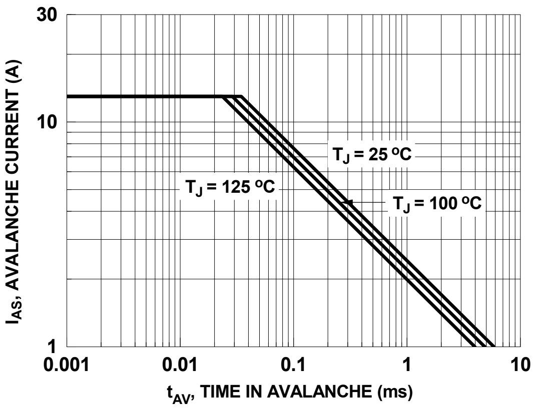


Figure 9. Unclamped Inductive Switching Capability

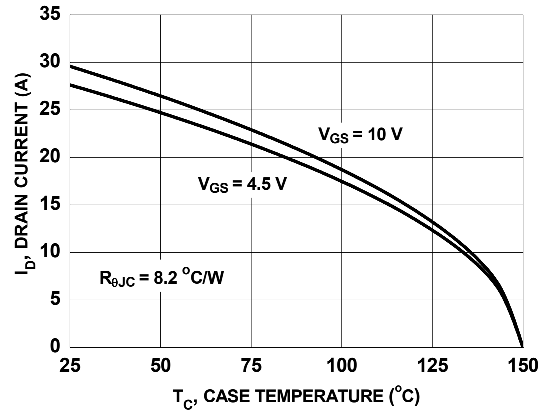


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

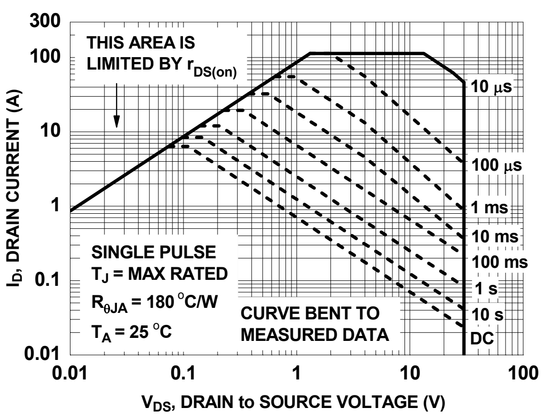


Figure 11. Forward Bias Safe Operating Area

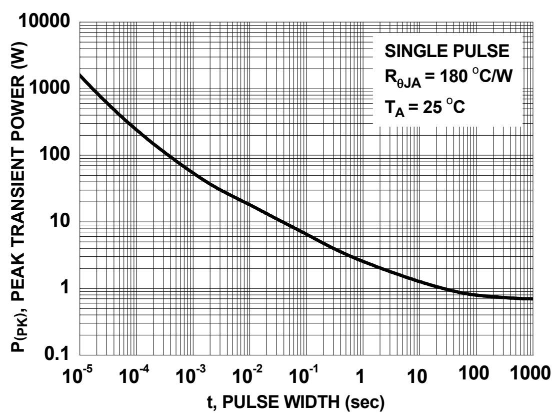


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

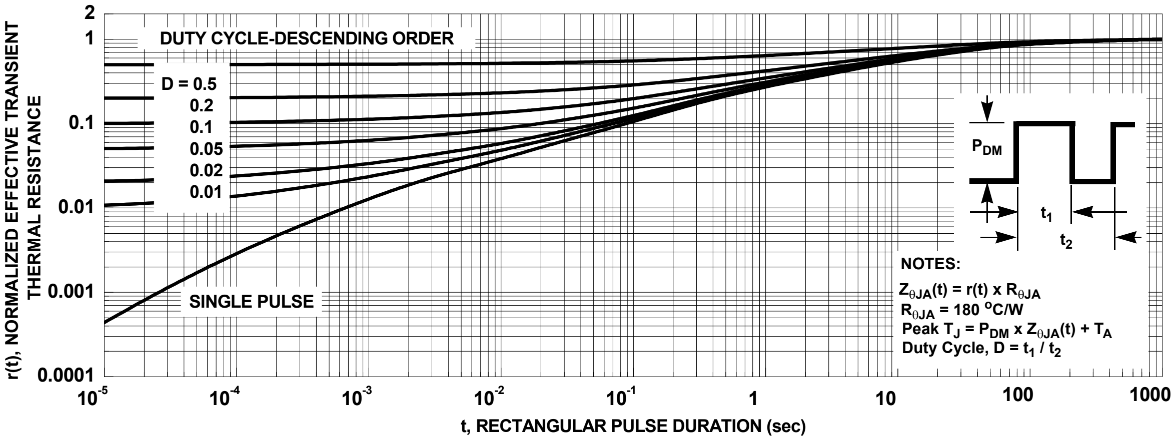


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

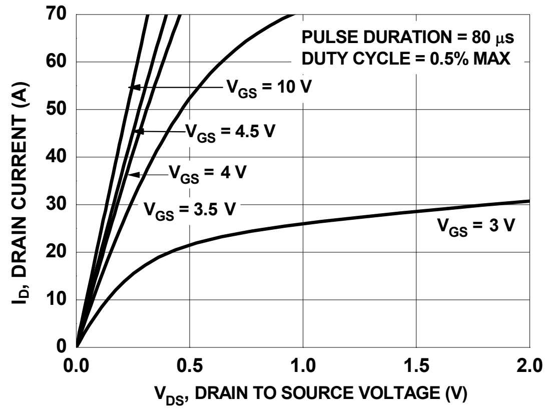


Figure 14. On- Region Characteristics

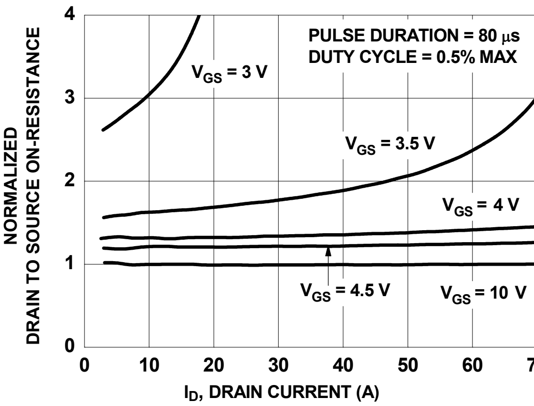


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

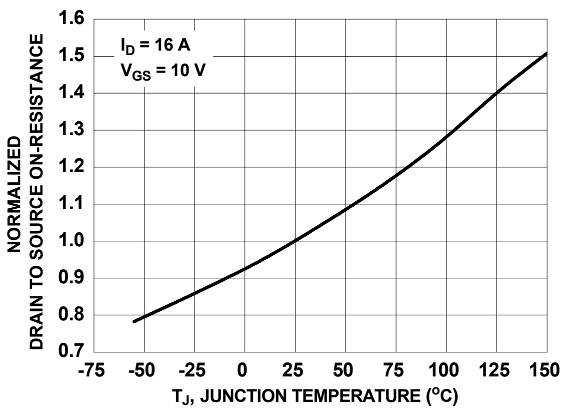


Figure 16. Normalized On-Resistance vs. Junction Temperature

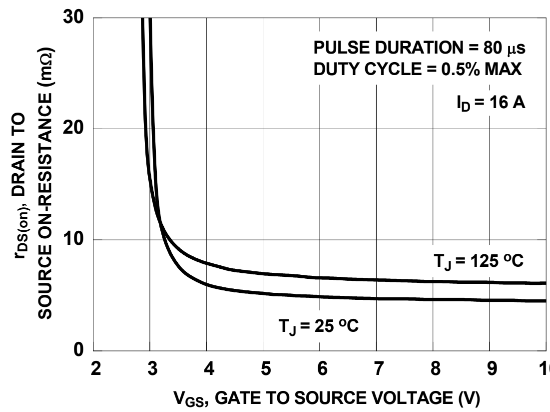


Figure 17. On-Resistance vs. Gate to Source Voltage

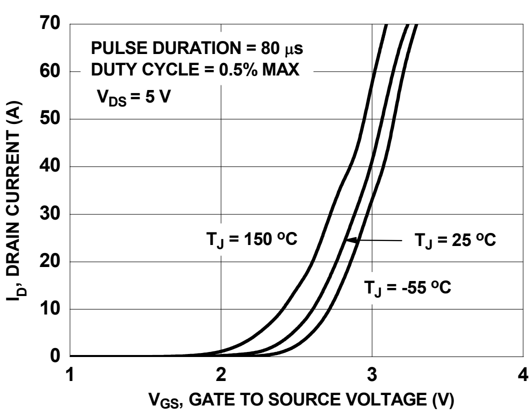


Figure 18. Transfer Characteristics

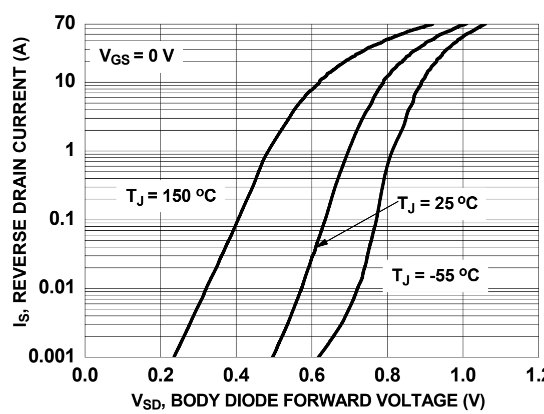


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted.

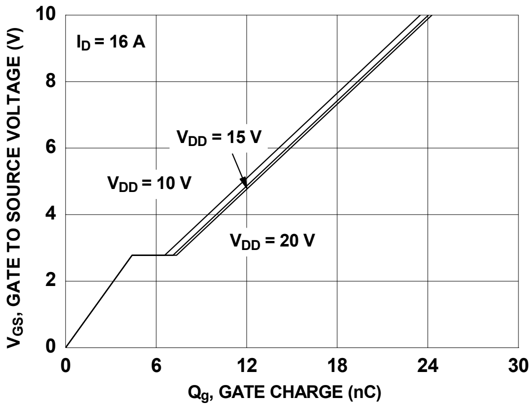


Figure 20. Gate Charge Characteristics

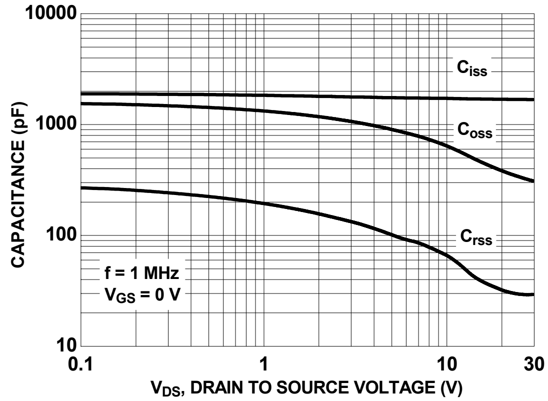


Figure 21. Capacitance vs. Drain to Source Voltage

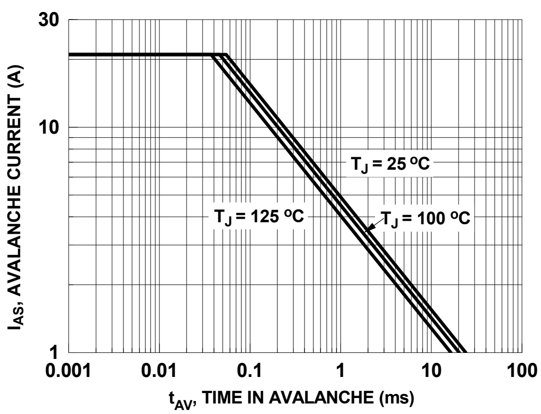


Figure 22. Unclamped Inductive Switching Capability

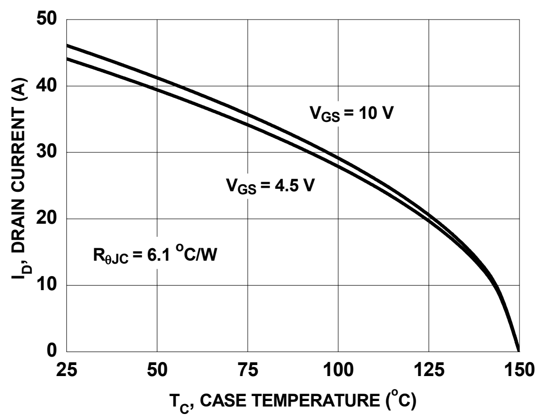


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

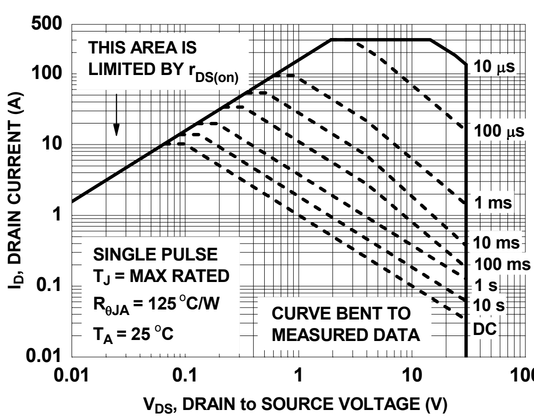


Figure 24. Forward Bias Safe Operating Area

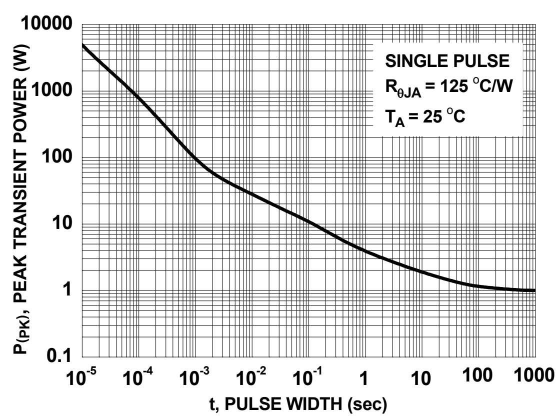


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

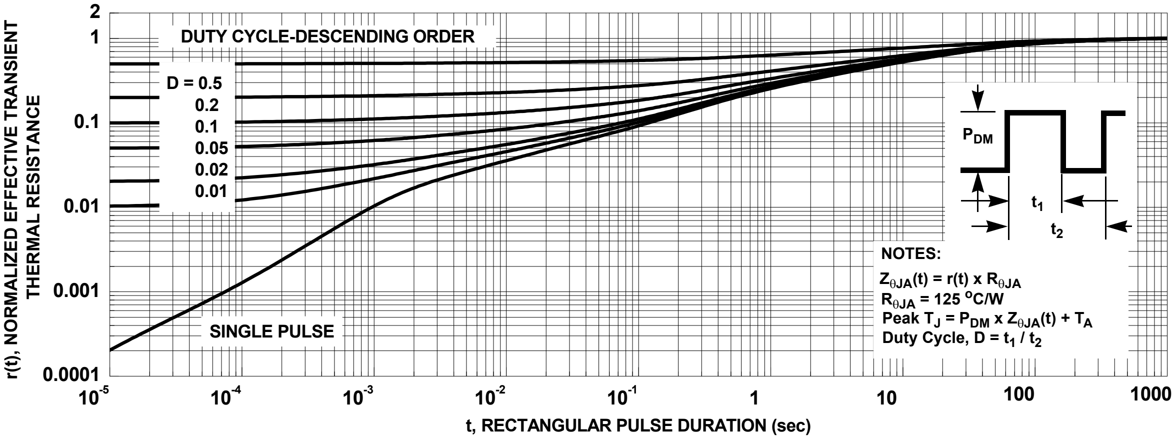
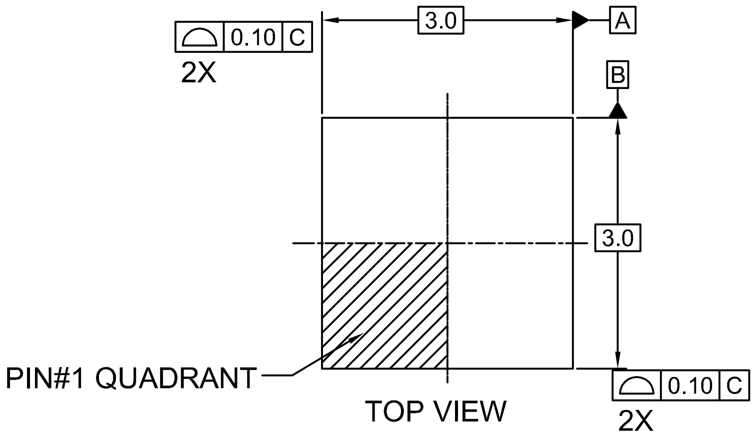


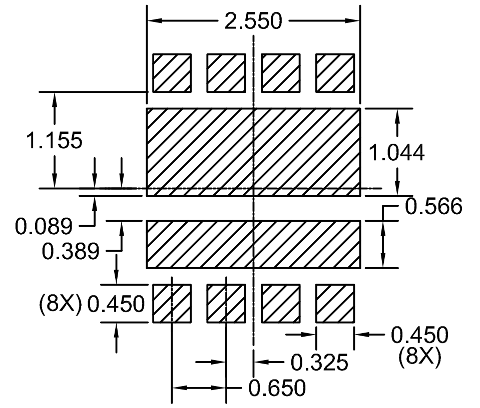
Figure 26. Junction-to-Ambient Transient Thermal Response Curve

REVISIONS

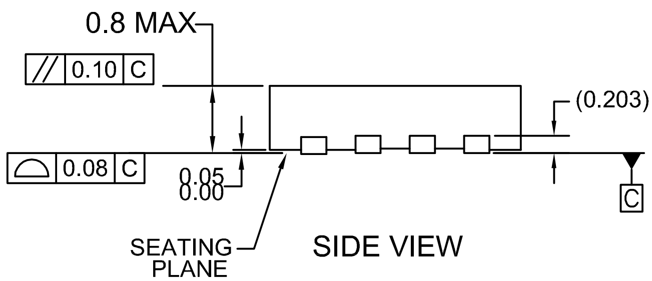
LTR	DESCRIPTION	EDCN	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL		01-08-2008	LY Lim



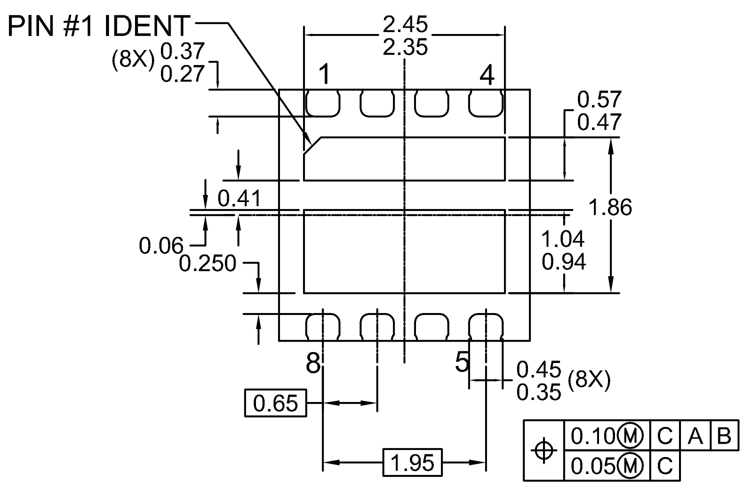
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

C. DRAWING FILE NAME : MLP08NREVA

APPROVALS		DATE
DRAWN	LY Lim	01-8-2008
DFTG. CHK.	David	01-8-2008
ENGR. CHK.	David	01-8-2008
PROJECTION	INCH [MM]	

FAIRCHILD SEMICONDUCTOR™ Bayan Lepas, FIZ, 11900, Penang, Malaysia.

8LD,MLP,NON JEDEC, DUAL 3.0MM SQUARE

SCALE	SIZE	DRAWING NUMBER	REV
N/A	N/A	MKT-MLP08N	1

DO NOT SCALE DRAWING SHEET 1 of 1

PUBLICATION ORDERING INFORMATION

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