**ON Semiconductor** 

Is Now

# Onsemi

To learn more about onsemi<sup>™</sup>, please visit our website at <u>www.onsemi.com</u>

onsemi and ONSEMI. and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product factures, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and asfety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or by customer's technical experts. onsemi products and actal performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiari

# 32-tap Digital Potentiometer (POT)

# Description

The CAT5115 is a single digital POT designed as an electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5115 contains a 32-tap series resistor array connected between two terminals  $R_H$  and  $R_L$ . An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper,  $R_W$ . The wiper is always set to the mid point, tap 15 at power up. The tap position is not stored in memory. Wiper-control of the CAT5115 is accomplished with three input control pins,  $\overline{CS}$ , U/D, and  $\overline{INC}$ . The  $\overline{INC}$  input increments the wiper in the direction which is determined by the logic state of the U/D input. The  $\overline{CS}$  input is used to select the device.

The digital POT can be used as a three-terminal resistive divider or as a two-terminal variable resistor. Digital POTs bring variability and programmability to a wide variety of applications including control, parameter adjustments, and signal processing.

For a pin-compatible device that recalls a stored tap position on power-up refer to the CAT5114 data sheet.

### Features

- 32-position Linear Taper Potentiometer
- Low Power CMOS Technology
- Single Supply Operation: 2.5 V 6.0 V
- Increment Up/Down Serial Interface
- Resistance Values:  $10 \text{ k}\Omega$ ,  $50 \text{ k}\Omega$  and  $100 \text{ k}\Omega$
- Available in PDIP, SOIC, TSSOP, MSOP Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

# Applications

- Automated Product Calibration
- Remote Control Adjustments
- Offset, Gain and Zero Control
- Tamper-proof Calibrations
- Contrast, Brightness and Volume Controls
- Motor Controls and Feedback Systems
- Programmable Analog Functions



# **ON Semiconductor®**

http://onsemi.com





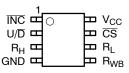




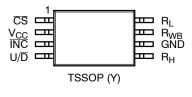
PDIP-8 L SUFFIX CASE 646AA

TSSOP-8 Y SUFFIX CASE 948AL

# **PIN CONFIGURATIONS**



PDIP (L), SOIC (V), MSOP (Z)



(Top Views)

# **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# **Functional Diagram**

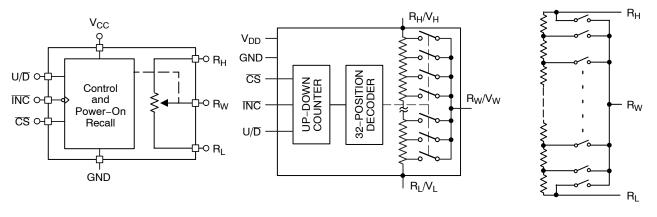


Figure 1. General

Figure 2. Detailed

Figure 3. Electronic Potentiometer Implementation

### Table 1. PIN DESCRIPTIONS

Name	Function
INC	Increment Control
U/D	Up/Down Control
R <sub>H</sub>	Potentiometer High Terminal
GND	Ground
R <sub>W</sub>	Buffered Wiper Terminal
RL	Potentiometer Low Terminal
CS	Chip Select
V <sub>CC</sub>	Supply Voltage

# **Pin Function**

# **INC:** Increment Control Input

The  $\overline{INC}$  input moves the wiper in the up or down direction determined by the condition of the U/ $\overline{D}$  input.

# U/D: Up/Down Control Input

The  $U\overline{D}$  input controls the direction of the wiper movement. When in a high state and  $\overline{CS}$  is low, any high-to-low transition on  $\overline{INC}$  will cause the wiper to move one increment toward the  $R_H$  terminal. When in a low state and  $\overline{CS}$  is low, any high-to-low transition on  $\overline{INC}$  will cause the wiper to move one increment towards the  $R_L$  terminal.

# RH: High End Potentiometer Terminal

 $R_{\rm H}$  is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the  $R_{\rm L}$  terminal. Voltage applied to the  $R_{\rm H}$  terminal cannot exceed the supply voltage,  $V_{\rm CC}$  or go below ground, GND.

**R**<sub>W</sub>: Wiper Potentiometer Terminal

 $R_W$  is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs,  $\overline{INC}$ ,

 $U/\overline{D}$  and  $\overline{CS}$ . Voltage applied to the  $R_W$  terminal cannot exceed the supply voltage,  $V_{CC}$  or go below ground, GND.

# RL: Low End Potentiometer Terminal

 $R_L$  is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the  $R_H$  terminal. Voltage applied to the  $R_L$  terminal cannot exceed the supply voltage,  $V_{CC}$  or go below ground, GND.  $R_L$  and  $R_H$  are electrically interchangeable.

# CS: Chip Select

The chip select input is used to activate the control input of the CAT5115 and is active low. When in a high state, activity on the  $\overline{INC}$  and  $U/\overline{D}$  inputs will not affect or change the position of the wiper.

# **Device Operation**

The CAT5115 operates like a digitally controlled potentiometer with  $R_H$  and  $R_L$  equivalent to the high and low terminals and  $R_W$  equivalent to the mechanical potentiometer's wiper. There are 32 available tap positions including the resistor end points,  $R_H$  and  $R_L$ . There are 31 resistor elements connected in series between the  $R_H$  and  $R_L$  terminals. The wiper terminal is connected to one of the 32 taps and controlled by three inputs,  $\overline{INC}$ ,  $U/\overline{D}$  and  $\overline{CS}$ . These inputs control a five-bit up/down counter whose output is decoded to select the wiper position.

With  $\overline{CS}$  set LOW the CAT5115 is selected and will respond to the U/ $\overline{D}$  and  $\overline{INC}$  inputs. HIGH to LOW transitions on  $\overline{INC}$  will increment or decrement the wiper (depending on the state of the U/ $\overline{D}$  input and five-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. When the CAT5115 is powered-down, the wiper position is reset. When power is restored, the counter is set to the mid point, tap 15.

# **Table 2. OPERATION MODES**

INC	CS	U/D	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	х	Store Wiper Position
Low	Low to High	х	No Store, Return to Standby
Х	High	Х	Standby

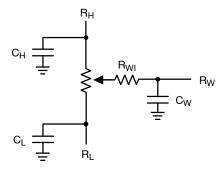


Figure 4. Potentiometer Equivalent Circuit

# Table 3. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage V <sub>CC</sub> to GND	-0.5 to +7	V
Inputs CS to GND	–0.5 to V <sub>CC</sub> +0.5	V
INC to GND	–0.5 to V <sub>CC</sub> +0.5	V
U/D to GND	-0.5 to V <sub>CC</sub> +0.5	V
H to GND	-0.5 to V <sub>CC</sub> +0.5	V
L to GND	–0.5 to V <sub>CC</sub> +0.5	V
W to GND	-0.5 to V <sub>CC</sub> +0.5	V
Operating Ambient Temperature Industrial ('I' suffix)	-40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	-65 to 150	°C
Lead Soldering (10 s max)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### **Table 4. RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Test Method	Min	Тур	Max	Units
V <sub>ZAP</sub> (Note 1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			V
I <sub>LTH</sub> (Notes 1, 2)	Latch-up	JEDEC Standard 17	100			mA
T <sub>DR</sub>	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N <sub>END</sub>	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

This parameter is tested initially and after a design or process change that affects the parameter.
 Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1 V to V<sub>CC</sub> + 1 V.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
POWER SUPPL	Y	•	•			
V <sub>CC</sub>	Operating Voltage Range		2.5	-	6.0	V
I <sub>CC1</sub>	Supply Current (Increment)	V <sub>CC</sub> = 6 V, f = 1 MHz, I <sub>W</sub> = 0	-	-	100	μA
		$V_{CC} = 6 V, f = 250 \text{ kHz}, I_W = 0$	-	-	50	μΑ
I <sub>SB1</sub> (Note 4)	Supply Current (Standby)	$\frac{\overline{CS}}{U/\overline{D}} = \frac{V_{CC} - 0.3 \text{ V}}{IN\overline{C}} = V_{CC} - 0.3 \text{ V or GND}$	-	0.01	1	μA
LOGIC INPUTS						
Ι <sub>ΙΗ</sub>	Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub>	-	-	10	μΑ
۱ <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V	-	-	-10	μΑ
V <sub>IH1</sub>	TTL High Level Input Voltage	$4.5~\textrm{V} \leq \textrm{V}_{\textrm{CC}} \leq 5.5~\textrm{V}$	2	-	V <sub>CC</sub>	V
V <sub>IL1</sub>	TTL Low Level Input Voltage		0	-	0.8	V
V <sub>IH2</sub>	CMOS High Level Input Voltage	$2.5 \text{ V} \le \text{V}_{\text{CC}} \le 6 \text{ V}$	V <sub>CC</sub> x 0.7	-	V <sub>CC</sub> + 0.3	V
V <sub>IL2</sub> CMOS Low Level Input Voltage		1 [	-0.3	-	V <sub>CC</sub> x 0.2	V
POTENTIOMET	ER CHARACTERISTICS					
R <sub>POT</sub>	Potentiometer Resistance	-10 Device		10		kΩ
		-50 Device		50		1
		-00 Device		100		
	Pot. Resistance Tolerance				±20	%
V <sub>RH</sub>	Voltage on R <sub>H</sub> pin		0		V <sub>CC</sub>	V
V <sub>RL</sub>	Voltage on R <sub>L</sub> pin		0		V <sub>CC</sub>	V
	Resolution			3.2		%
INL	Integral Linearity Error	I <sub>W</sub> ≤ 2 μA		0.5	1	LSB
DNL	Differential Linearity Error	I <sub>W</sub> ≤ 2 μA		0.25	0.5	LSB
R <sub>WI</sub>	Wiper Resistance	$V_{CC} = 5 \text{ V}, I_W = 1 \text{ mA}$		70	200	Ω
		V <sub>CC</sub> = 2.5 V, I <sub>W</sub> = 1 mA		150	400	Ω
I <sub>W</sub>	Wiper Current	(1)			1	mA
TC <sub>RPOT</sub>	TC of Pot Resistance			±50	±300	ppm/°0
TC <sub>RATIO</sub>	Ratiometric TC				20	ppm/°0
V <sub>N</sub>	Noise	100 kHz / 1 kHz		8/24		nV/√H:
C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub>	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10 k $\Omega$	1	1.7		MHz

This parameter is tested initially and after a design or process change that affects the parameter.
 Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1 V to V<sub>CC</sub> + 1 V.
 I<sub>W</sub> = source or sink.
 These parameters are periodically sampled and are not 100% tested.

# Table 6. AC TEST CONDITIONS

V <sub>CC</sub> Range	$2.5~\textrm{V} \leq \textrm{V}_{\textrm{CC}} \leq 6.0~\textrm{V}$
Input Pulse Levels	0.2 x V_{CC} to 0.7 x V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Levels	$0.5 \times V_{CC}$

# Table 7. AC OPERATING CHARACTERISTICS ( $V_{CC}$ = +2.5 V to +6.0 V, $V_{H}$ = $V_{CC}$ , $V_{L}$ = 0 V, unless otherwise specified)

Symbol	Parameter	Min	Typ (Note 7)	Max	Units
t <sub>CI</sub>	CS to INC Setup	100	-	-	ns
t <sub>DI</sub>	U/D to INC Setup	50	-	-	ns
t <sub>ID</sub>	U/D to INC Hold	100	-	-	ns
t <sub>IL</sub>	INC LOW Period	250	-	-	ns
t <sub>IH</sub>	INC HIGH Period	250	-	-	ns
t <sub>IC</sub>	INC Inactive to CS Inactive	1	-	-	μs
t <sub>CPH</sub>	CS Deselect Time	100	-	-	ns
t <sub>IW</sub>	INC to V <sub>OUT</sub> Change	-	1	5	μs
t <sub>CYC</sub>	INC Cycle Time	1	-	_	μs
t <sub>R</sub> , t <sub>F</sub> (Note 8)	INC Input Rise and Fall Time	_	-	500	μs
t <sub>PU</sub> (Note 8)	Power-up to Wiper Stable	_	_	1	ms

Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.
 This parameter is periodically sampled and not 100% tested.
 MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

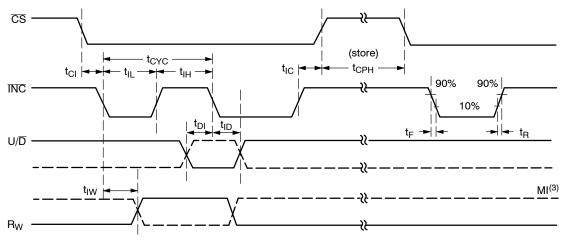


Figure 5. A.C. Timing

# **APPLICATIONS INFORMATION**

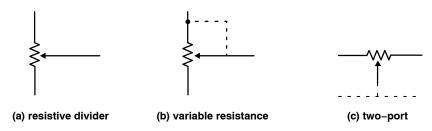
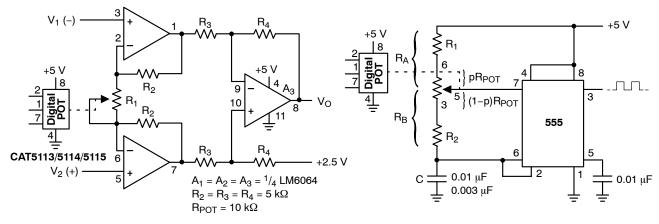


Figure 6. Potentiometer Configuration

Applications



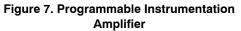
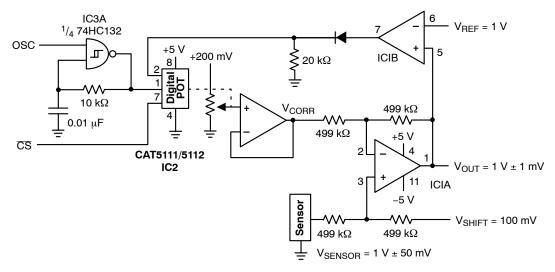
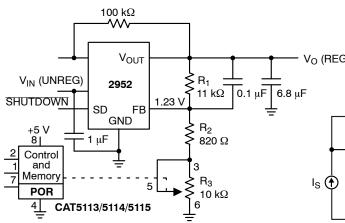
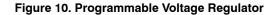


Figure 8. Programmable Sq. Wave Oscillator (555)









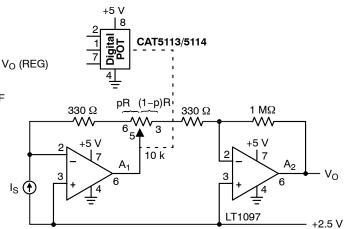


Figure 11. Programmable I to V Convertor

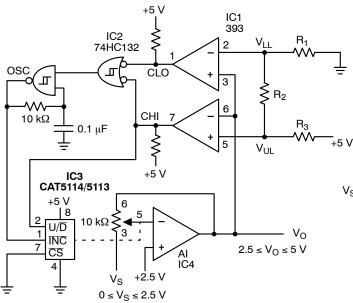


Figure 12. Automatic Gain Control

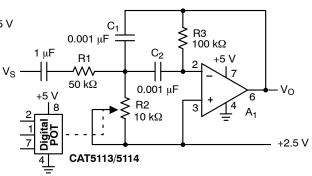


Figure 13. Programmable Bandpass Filter

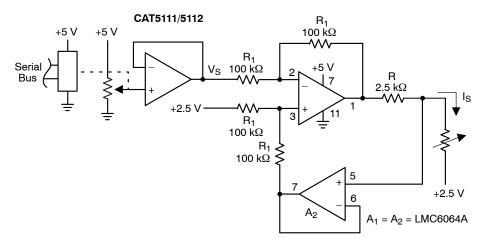


Figure 14. Programmable Current Source/Sink

# **Table 8. ORDERING INFORMATION**

Orderable Part Numbers	Reset Threshold Voltage	Package-Pin	Lead Finish	Shipping <sup>†</sup>
CAT5115LI-10-G	10			50 Units / Tube
CAT5115LI-50-G	50	PDIP-8	NiPdAu	50 Units / Tube
CAT5115LI-00-G	100			50 Units / Tube
CAT5115VI-10-GT3	10			3000 / Tape & Reel
CAT5115VI-50-GT3	50	SOIC-8 NiPdAu	3000 / Tape & Reel	
CAT5115VI-00-GT3	100			3000 / Tape & Reel
CAT5115YI-10-GT3	10			3000 / Tape & Reel
CAT5115YI-50-GT3	50	TSSOP-8	NiPdAu	3000 / Tape & Reel
CAT5115YI-00-GT3	100			3000 / Tape & Reel
CAT5115ZI-10-GT3	10	MSOP-8		3000 / Tape & Reel
CAT5115ZI-50-GT3	50		NiPdAu	3000 / Tape & Reel
CAT5115ZI-00-GT3	100			3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

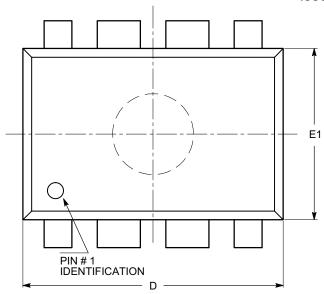
For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at <u>www.onsemi.com</u>.

Contact factory for package availability.
 All packages are RoHS-compliant (Lead-free, Halogen-free).
 The standard lead finish is NiPdAu.

14. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

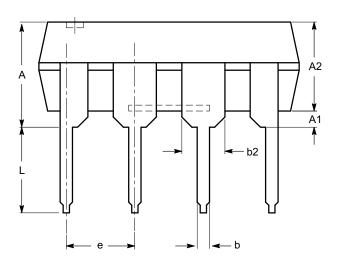
# PACKAGE DIMENSIONS

PDIP-8, 300 mils CASE 646AA ISSUE A



SYMBOL	MIN	NOM	MAX	
А			5.33	
A1	0.38			
A2	2.92	3.30	4.95	
b	0.36	0.46	0.56	
b2	1.14	1.52	1.78	
с	0.20	0.25	0.36	
D	9.02	9.27	10.16	
E	7.62	7.87	8.25	
E1	6.10	6.35	7.11	
е	2.54 BSC			
eB	7.87		10.92	
L	2.92	3.30	3.80	

TOP VIEW

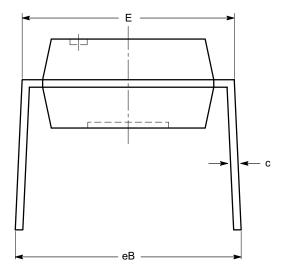


SIDE VIEW

# Notes:

(1) All dimensions are in millimeters.

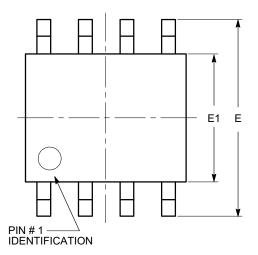
(2) Complies with JEDEC MS-001.



END VIEW

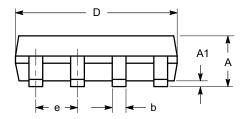
# PACKAGE DIMENSIONS

SOIC 8, 150 mils CASE 751BD ISSUE O



SYMBOL	MIN	NOM	MAX
А	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
с	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
е		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°

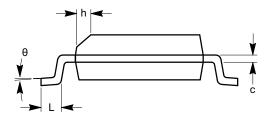
TOP VIEW



SIDE VIEW

# Notes:

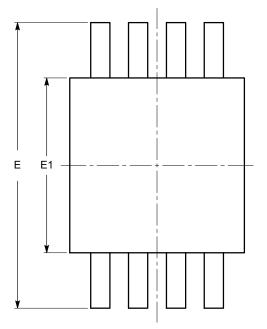
(1) All dimensions are in millimeters. Angles in degrees.
 (2) Complies with JEDEC MS-012.





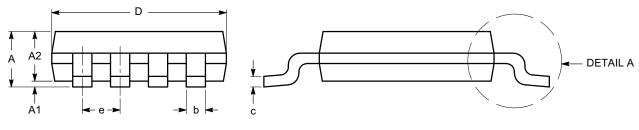
# PACKAGE DIMENSIONS

MSOP 8, 3x3 CASE 846AD ISSUE O



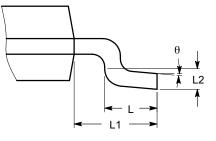
TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
с	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
е		0.65 BSC	
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°		6°



SIDE VIEW

END VIEW



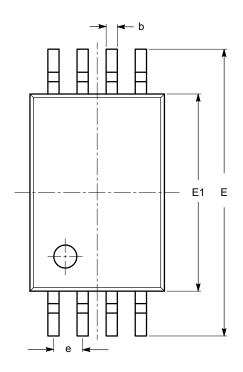


### Notes:

- All dimensions are in millimeters. Angles in degrees.
  Complies with JEDEC MO-187.

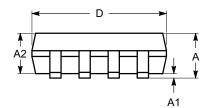
### PACKAGE DIMENSIONS

TSSOP8, 4.4x3 CASE 948AL ISSUE O



SYMBOL	MIN	NOM	MAX
А			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
с	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
е	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°

### TOP VIEW



SIDE VIEW



### Notes:

(1) All dimensions are in millimeters. Angles in degrees.

(2) Complies with JEDEC MO-153.

**ON Semiconductor** and **UD** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemic.om/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its product/patent coverage may be accessed at www.onsemic.om/site/pdf/Patent-Marking.pdf. SCILLC particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typical" must be validated for each customer application by customer's technical experts. SCILLC products are not designed, intended, or authorized for use as components insystems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and easonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Acti

### PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support: ON Semiconductor Website: www.onsemi.com

### cal Support: Order Literature: http://www.onsemi.com/orderlit

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5817-1050

For additional information, please contact your local Sales Representative