

AX-SFJK, AX-SFJK-API

Ultra-Low Power, AT Command / API Controlled, Sigfox[®] Compliant Transceiver IC for Up-Link and Down-Link



ON Semiconductor[®]

www.onsemi.com

OVERVIEW

Circuit Description

AX-SFJK and AX-SFJK-API are ultra-low power single chip solutions for a node on the Sigfox network with both up- and down-link functionality. The AX-SFJK chip is delivered fully ready for operation and contains all the necessary firmware to transmit and receive data from the Sigfox network in Japan (SIGFOX RCZ3a region). It connects to the customer product using a logic level RS232 UART. AT commands are used to send frames and configure radio parameters.

The AX-SFJK-API variant is intended for customers wishing to write their own application software based on the AX-SF-LIB-1-GEVK library.

Features

Functionality and Ecosystem

- Sigfox up-link and down-link functionality controlled by AT commands or API
- The AX-SFJK and AX-SFJK-API ICs are part of a whole development and product ecosystem available from ON Semiconductor for any Sigfox requirement. Other parts of the ecosystem include
 - ◆ Ready to go development kit DVK-SFJK-[API]-1-GEVK including a 2 year Sigfox subscription
 - ◆ Sigfox Ready[®] certified reference design for the AX-SFJK and AX-SFJK-API ICs

General Features

- QFN40 5 mm x 7 mm package
- Supply range 1.8 V*–3.6 V
- –40°C to 85°C
- Temperature sensor
- Supply voltage measurements

*The device is operational from 1.8 V to 3.6 V. However, a supply voltage below 2.0 V is considered an extreme condition. Details see Table 4.

- 10 GPIO pins
 - ◆ 2 GPIO pins with selectable voltage measure functionality, differential (1 V or 10 V range) or single ended (1 V range) with 10 bit resolution
 - ◆ 2 GPIO pins with selectable sigma delta DAC output functionality
 - ◆ 2 GPIO pins with selectable output clock
 - ◆ 3 GPIO pins selectable as SPI master interface
 - ◆ Integrated RX/TX switching with differential antenna pins

Power Consumption

- Ultra-low Power Consumption:
 - ◆ Charge required to send a Sigfox OOB packet at 13 dBm output power: 0.28 C
 - ◆ Deep Sleep mode current: 100 nA
 - ◆ Sleep mode current: 1.6 μ A
 - ◆ Standby mode current: 0.5 mA
 - ◆ Continuous radio RX-mode at 922.2 MHz: 15 mA
 - ◆ Continuous radio TX-mode at 923.2 MHz: 45 mA @ 13 dBm

High Performance Narrow-band Sigfox RF Transceiver

- Receiver
 - ◆ Carrier frequency 922.2 MHz
 - ◆ Data rate 600 bps FSK
 - ◆ Sensitivity –126 dBm @ 600 bps, 922.2 MHz, GFSK
 - ◆ 0 dBm maximum input power
- Transmitter
 - ◆ Carrier frequency 923.2 MHz
 - ◆ Data rate 100 bps PSK
 - ◆ High efficiency, high linearity integrated power amplifier
 - ◆ Maximum output power 13 dBm

Applications

Sigfox networks up-link and down-link.

AX-SFJK, AX-SFJK-API

BLOCK DIAGRAM

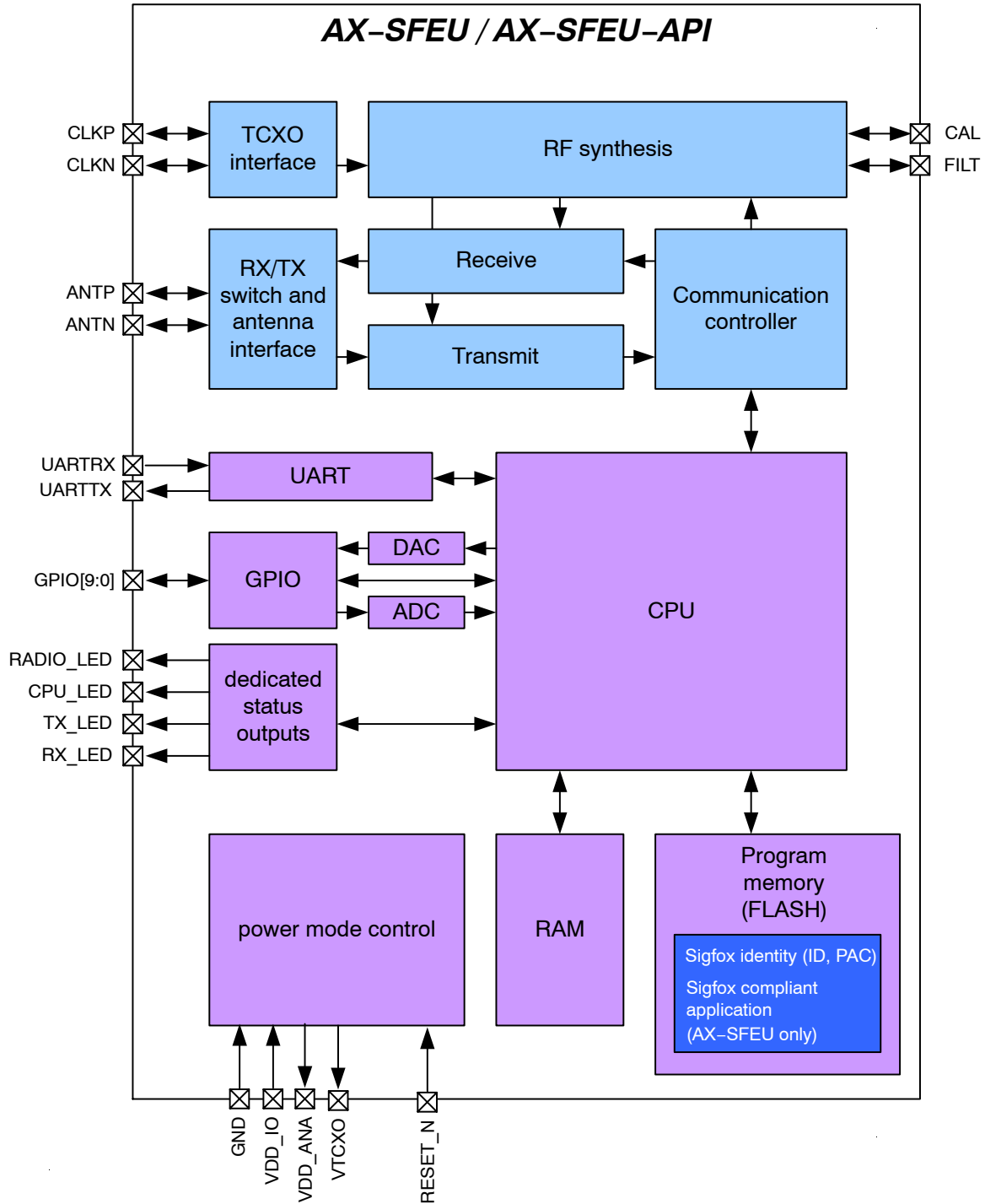


Figure 1. Functional Block Diagram of the AX-SFJK / AX-SFJK-API

AX-SFJK, AX-SFJK-API

Table 1. PIN FUNCTION DESCRIPTIONS

Symbol	Pin(s)	Type	Description
VDD_ANA	1	P	Analog power output, decouple to neighboring GND
GND	2	P	Ground, decouple to neighboring VDD_ANA
ANTP	3	A	Differential antenna input/output
ANTN	4	A	Differential antenna input/output
NC	5	N	Do not connect
GND	6	P	Ground, decouple to neighboring VDD_ANA
VDD_ANA	7	P	Analog power output, decouple to neighboring GND
GND	8	P	Ground
FILT	9	A	Synthesizer filter
L2	10	A	Must be connected to pin L1
L1	11	A	Must be connected to pin L2
NC	12	N	Do not connect
GPIO8	13	I/O/PU	General purpose IO
GPIO7	14	I/O/PU	General purpose IO, selectable SPI functionality (MISO)
GPIO6	15	I/O/PU	General purpose IO, selectable SPI functionality (MOSI)
GPIO5	16	I/O/PU	General purpose IO, selectable SPI functionality (SCK)
GPIO4	17	I/O/PU	General purpose IO, selectable $\Sigma\Delta$ DAC functionality, selectable clock functionality
CPU_LED	18	O	CPU activity indicator
RADIO_LED	19	O	Radio activity indicator
VTCXO	20	O	TCXO power
GPIO9	21	I/O/PU	General purpose IO, wakeup from deep sleep
UARTTX	22	O	UART transmit
UARTRX	23	I/PU	UART receive
RX_LED/ DBG_DATA	24	O I/O	Receive activity indicator in AX-SFJK Debugger data line in AX-SFJK-API
TX_LED/ DBG_CLK	25	O I	Transmit activity indicator in AX-SFJK Debugger clock line in AX-SFJK-API
NC/ DBG_EN	26	PD PD	Do not connect in AX-SFJK Debugger enable line in AX-SFJK-API
RESET_N	27	I/PU	Optional reset pin. Internal pull-up resistor is permanently enabled, nevertheless it is recommended to connect this pin to VDD_IO if it is not used.
GND	28	P	Ground
VDD_IO	29	P	Unregulated power supply
GPIO0	30	I/O/A/PU	General purpose IO, selectable ADC functionality, selectable $\Sigma\Delta$ DAC functionality, selectable clock functionality
GPIO1	31	I/O/A/PU	General purpose IO, selectable ADC functionality
GPIO2	32	I/O/A/PU	General purpose IO, selectable ADC functionality
NC	33	N	Do not connect
NC	34	N	Do not connect
GPIO3	35	I/O/A/PU	General purpose IO, selectable ADC functionality
VDD_IO	36	P	Unregulated power supply
CAL	37	A	Connect to FILT as shown in the application diagram
NC	38	N	Do not connect
CLKN	39	A	TCXO interface

AX-SFJK, AX-SFJK-API

Table 1. PIN FUNCTION DESCRIPTIONS (continued)

Symbol	Pin(s)	Type	Description
CLKP	40	A	TCXO interface
GND	Center pad	P	Ground on center pad of QFN, must be connected

A = analog input

I = digital input signal

O = digital output signal

PU = pull-up

I/O = digital input/output signal

N = not to be connected

P = power or ground

PD = pull-down

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible. Pins GPIO[3:0] must not be driven above VDD_IO, all other digital inputs are 5 V tolerant. All GPIO pins and UARTRX start up as input with pull-up. For explanations on how to use the GPIO pins, see chapter “AT Commands”.

Table 2.

Pin	Possible GPIO Modes
GPIO0	0, 1, Z, U, A, T
GPIO1	0, 1, Z, U, A
GPIO2	0, 1, Z, U, A
GPIO3	0, 1, Z, U, A
GPIO4	0, 1, Z, U, T
GPIO5	0, 1, Z, U
GPIO6	0, 1, Z, U
GPIO7	0, 1, Z, U
GPIO8	0, 1, Z, U
GPIO9	0, 1, Z, U

0 = pin drives low

1 = pin drives high

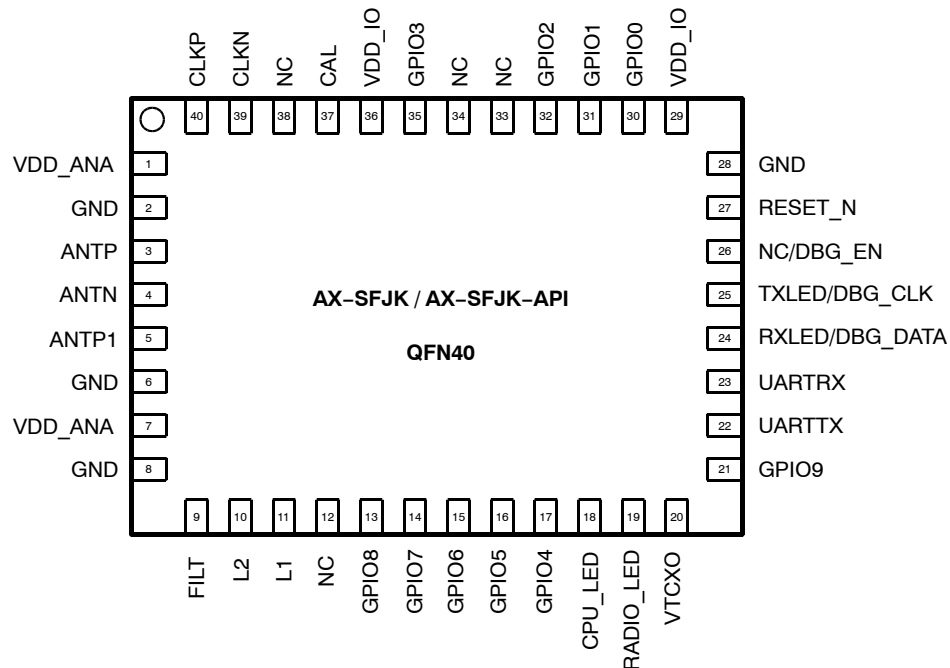
Z = pin is high impedance input

U = pin is input with pull-up

A = pin is analog input

T = pin is driven by clock or DAC

Pinout Drawing



NOTE: Pins 24–26 have different functionalities in AT command and API versions, so for these pins AX-SFJK/AX-SFJK-API explanations are shown respectively.

Figure 2. Pinout Drawing (Top View)

SPECIFICATIONS

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Condition	Min	Max	Units
VDD_IO	Supply voltage		-0.5	5.5	V
IDD	Supply current			200	mA
P _{tot}	Total power consumption			800	mW
P _i	Absolute maximum input power at receiver input	ANTP and ANTN pins in RX mode		10	dBm
I _{I1}	DC current into any pin except ANTP, ANTN, ANTP1		-10	10	mA
I _{I2}	DC current into pins ANTP, ANTN, ANTP1		-100	100	mA
I _O	Output Current			40	mA
V _{ia}	Input voltage ANTP, ANTN, ANTP1 pins		-0.5	5.5	V
	Input voltage digital pins		-0.5	5.5	V
V _{es}	Electrostatic handling	HBM	-2000	2000	V
T _{amb}	Operating temperature		-40	85	°C
T _{stg}	Storage temperature		-65	150	°C
T _j	Junction Temperature			150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AX-SFJK, AX-SFJK-API

DC Characteristics

Table 4. SUPPLIES

Conditions for all current and charge values unless otherwise specified are for the hardware configuration described in the AX-SFJK Application Note: Sigfox Compliant Reference Design.

Symbol	Description	Condition	Min	Typ	Max	Units
T _{AMB}	Operational ambient temperature		-40	27	85	°C
VDD _{IO}	I/O and voltage regulator supply voltage		1.8*	3.3	3.6	V
VDD _{IO_R1}	I/O voltage ramp for reset activation (Note 1)	Ramp starts at VDD_IO ≤ 0.1 V	0.1			V/ms
VDD _{IO_R2}	I/O voltage ramp for reset activation (Note 1)	Ramp starts at 0.1 V < VDD_IO < 0.7 V	3.3			V/ms
I _{DS}	Deep Sleep mode current	AT\$P=2		350		nA
I _{SLEEP}	Sleep mode current	AT\$P=1		1.6		μA
I _{STDBY}	Standby mode current (Note 2)			0.5		mA
I _{RX_CONT}	Current consumption continuous RX	AT\$TM=3,255		10		mA
Q _{SFX_OOB_14}	Charge to send a Sigfox out of band message, 13 dBm	AT\$SO		0.28		C
Q _{SFX_BIT_14}	Charge to send a bit, 13 dBm	AT\$SB=0		0.21		C
Q _{SFX_BITDL_14}	Charge to send a bit with downlink receive, 13 dBm	AT\$SB=0,1		0.56		C
Q _{SFX_LFR_14}	Charge to send the longest possible Sigfox frame (12 byte) , 13 dBm	AT\$SF=00112233445566778899aabb		0.34		C
Q _{SFX_LFRDL_14}	Charge to send the longest possible Sigfox frame (12 byte) with downlink receive, 13 dBm	AT\$SF=00112233445566778899aabb,1		0.67		C
I _{TXMOD14AVG}	Modulated Transmitter Current	Pout=13 dBm; average		45		mA

*The device is operational from 1.8 V to 3.6 V. However, a supply voltage below 2.0 V is considered an extreme condition and operation can lead to reduced output power and increased spurious emission.

1. If VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended, see the AX8052 Application Note: Power On Reset
2. Internal 20 MHz oscillator, voltage conditioning and supervisory circuit running.

Battery Life Examples

Scenario:

- 2 AAA Alkaline batteries in series
- One OOB frame transmitter per day at Pout=13 dBm
- Four maximum length frames with downlink receive per day at Pout=13 dBm
- Device in Sleep
- Neglecting battery self discharge

2 AAA alkaline capacity	1500 mAh * 3600 s/h	5400 C
Sleep charge per day	1.8 μA * 86400 s	0.16 C/day
OOB frame transmission		0.34 C/day
Frame transmission with downlink	4 * 0.67 C/day	2.68 C/day
Total Charge consumption		3.18 C/day
Battery life		4.7 Years

AX-SFJK, AX-SFJK-API

Table 5. LOGIC

Symbol	Description	Condition	Min	Typ	Max	Units
Digital Inputs						
V _{T+}	Schmitt trigger low to high threshold point	VDD_IO = 3.3 V		1.55		V
V _{T-}	Schmitt trigger high to low threshold point			1.25		V
V _{IL}	Input voltage, low				0.8	V
V _{IH}	Input voltage, high		2.0			V
V _{IPA}	Input voltage range, GPIO[3:0]		-0.5		VDD_IO	V
V _{IPBC}	Input voltage range, GPIO[9:4], UARTTX		-0.5		5.5	V
I _L	Input leakage current		-10		10	μA
R _{PU}	Programmable Pull-Up Resistance			65		kΩ
Digital Outputs						
I _{OH}	Output Current, high Ports GPIO[9:0], UARTTX, TXLED, RXLED, TXLED, CPULED	V _{OH} = 2.4 V	8			mA
I _{OL}	Output Current, low GPIO[9:0], UARTTX, TXLED, RXLED, TXLED, CPULED	V _{OL} = 0.4 V	8			mA
I _{oz}	Tri-state output leakage current		-10		10	μA

AC Characteristics

Table 6. TCXO REFERENCE INPUT

Symbol	Description	Condition	Min	Typ	Max	Units
f _{TCXO}	TCXO frequency	A passive network between the TCXO output and the pins CLKP and CLKN is required. For detailed TCXO network recommendations depending on the TCXO output swing refer to the AX5043 Application Note: Use with a TCXO Reference Clock. For TCXO recommendations see the AX-SFJK Application Note: Sigfox Compliant Reference Design		48		MHz

Table 7. TRANSMITTER

Conditions for transmitter specifications unless otherwise specified with the antenna network from AX-SFJK Application Note: Sigfox Compliant Reference Design and at 923.2 MHz.

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate			100		bps
PTX	Highest Transmitter output power	AT\$CW=923200000,1		13		dBm
dTX _{temp}	Transmitter power variation vs. temperature	-40°C to +85°C		±0.5		dB
dTX _{Vdd}	Transmitter power variation vs. VDD_IO	1.8 to 3.6 V		±0.5		dB
PTX _{harm2}	Emission @ 2 nd harmonic			-50		dBc
PTX _{harm3}	Emission @ 3 rd harmonic			-67		
PTX _{harm4}	Emission @ 4 th harmonic			-65		

AX-SFJK, AX-SFJK-API

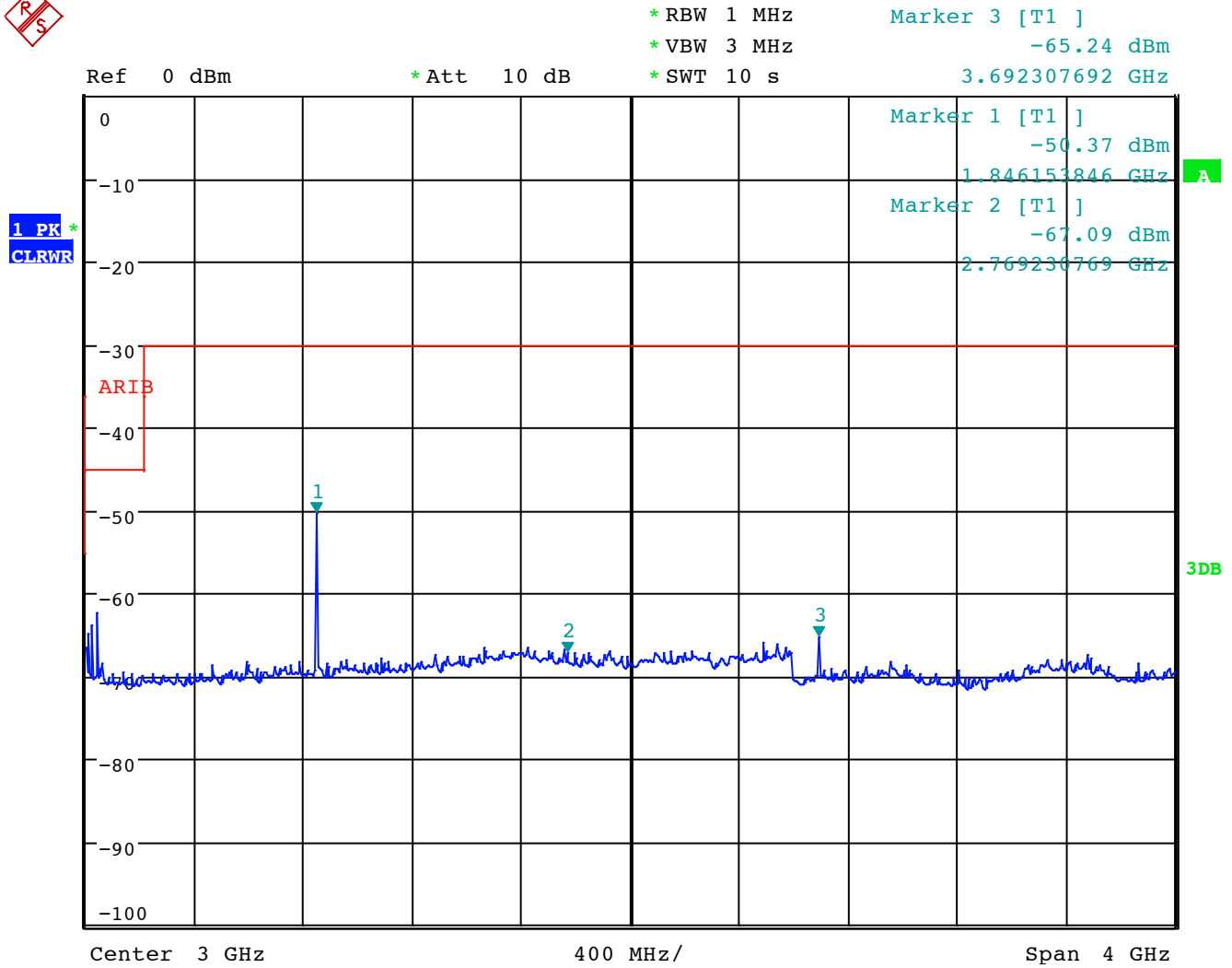


Figure 3. Typical Spectrum with Harmonics at 13 dBm Output Power

Table 8. RECEIVER

Conditions for receiver specifications unless otherwise specified with the antenna network from AX-SFJK Application Note: Sigfox Compliant Reference Design and at 922.2 MHz.

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate			600		bps
IS _{BER905}		AT\$SB=x,1, AT\$SF=x,1, AT\$TM=3,x PER < 0.1		-126		dBm
BLK ₉₀₅	Blocking at ±10 MHz offset	Channel/Blocker @ PER = 0.1, wanted signal level is +3 dB above the typical sensitivity, the blocker signal is CW		78		dB

AX-SFJK, AX-SFJK-API

Table 9. ADC / TEMPERATURE SENSOR

Symbol	Description	Condition	Min	Typ	Max	Units
ADCRES	ADC resolution			10		Bits
V _{ADCREf}	ADC reference voltage		0.95	1	1.05	V
Z _{ADC00}	Input capacitance				2.5	pF
DNL	Differential nonlinearity			± 1		LSB
INL	Integral nonlinearity			± 1		LSB
OFF	Offset			3		LSB
GAIN_ERR	Gain error			0.8		%

ADC in Differential Mode

V _{ABS_DIFF}	Absolute voltages & common mode voltage in differential mode at each input		0		VDD_IO	V
V _{FS_DIFF01}	Full swing input for differential signals	Gain x1	-500		500	mV
V _{FS_DIFF10}		Gain x10	-50		50	mV

ADC in Single Ended Mode

V _{MID_SE}	Mid code input voltage in single ended mode			0.5		V
V _{IN_SE00}	Input voltage in single ended mode		0		VDD_IO	V
V _{FS_SE01}	Full swing input for single ended signals	Gain x1	0		1	V

Temperature Sensor

AT\$RL _{NG}	Temperature range	AT\$T?	-40		85	°C
T _{ERR_CAL}	Temperature error	AT\$T?	-2		2	°C

COMMAND INTERFACE

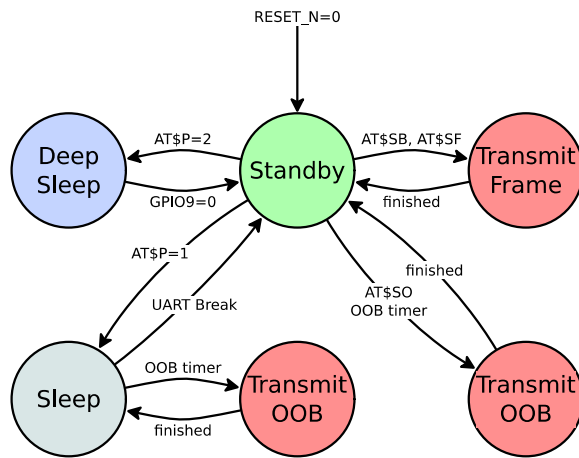
General Information

The chapter “Command Interface” is a documentation of the AT-Command set for devices which do not have an API-interface. To see whether the device is capable of receiving AT-Commands, please refer to the table “[Device Versions](#)”. If the device has been shipped with the API-Interface, please refer to the SW manual and “apiexample” code delivered with AX-SF-LIB-1-GEVK for an introduction on how to setup a project and how to use the API-Interface.

Serial Parameters: 9600, 8, N, 1

The AX-SFJK uses the UART (pins UARTTX, UARTRX) to communicate with a host and uses a bitrate of **9600 baud**, no parity, 8 data bits and one stop bit.

Power Modes



Standby

After Power-Up and after finishing a SIGFOX transmission, AX-SFJK enters Standby mode. In Standby mode, AX-SFJK listens on the UART for commands from the host. Also, OOB frames are transmitted whenever the OOB timer fires. To conserve power, the AX-SFJK can be put into Sleep or turned off (Deep Sleep) completely.

Sleep

The command **AT\$P=1** is used to put the AX-SFJK into Sleep mode. In this mode, only the wakeup timer for out-of-band messages is still running. To wake the AX-SFJK up from Sleep mode toggle the serial UARTRX pin, e.g. by sending a break (break is an RS232 framing violation, i.e. at least 10 bit durations low). When an Out of Band (OOB) message is due, AX-SFJK automatically wakes up to transmit the message, and then returns to Sleep mode.

Deep Sleep

In Deep Sleep mode, the AX-SFJK is completely turned off and only draws negligible leakage current. Deep Sleep mode can be activated with **AT\$P=2**. To wake-up from Deep Sleep mode, GPIO9 is pulled to GND.

When using Deep Sleep mode, keep two things in mind: Everything is turned off, timers are not running at all and all settings will be lost (use **AT\$WR** to save settings to flash before entering Deep Sleep mode). Out-of-band messages will therefore not be sent. The pins states are frozen in Deep Sleep mode. The user must ensure that this will not result in condition which would draw a lot of current.

AT Commands

Numerical Syntax

```

hexdigit ::= [0-9A-Fa-f]
hexnum  ::= "0x" hexdigit+
decnum   ::= "0" | [1-9] [0-9]*
octnum   ::= "0" [0-7]+
binnum   ::= "0b" [01]+
bit      ::= [01]
optnum   ::= "-1"
frame    ::= (hexdigit hexdigit)+
uint     ::= hexnum | decnum | octnum | binnum
uint_opt ::= uint | optnum
    
```

Command Syntax

A command starts with ‘AT’ (everything is case sensitive!), continues with the actual command followed by parameters (if any) and ends with any kind of whitespace (space, tab, newline etc.)

If incorrect syntax is detected (“parsing error”) all input is ignored up until the next whitespace character.

Also note that any number can be entered in any format (Hexadecimal, Decimal, Octal and binary) by adding the corresponding prefix (‘0x’, ‘0’, ‘0b’). The only exception is the ‘Send Frame’ command (**AT\$SF**) which expects a list of hexadecimal digits without any prefix.

Return Codes

A successful command execution is indicated by sending ‘OK’. If a command returns a value (e.g. by querying a register) only the value is returned.

Examples

Bold text is sent to AX-SFJK.

```

AT$I=0
AX-Sigfox 1.1-RCZ3
    
```

Here, we execute command ‘I’ to query some general information.

```

AT$SF=aabb1234
OK
    
```

This sends a Sigfox frame containing { 0xAA : 0xBB : 0x12 : 0x34 } without waiting for a response telegram.

```

AT$SF=0011223344,1
OK
RX=AA BB CC DD
    
```

This sends a Sigfox frame containing { 0x00 : 0x11 : 0x22 : 0x33 : 0x44 }, then waits for a downlink response telegram,

AX-SFJK, AX-SFJK-API

which in this example contains { 0xAA : 0xBB : 0xCC : 0xDD }.

AT\$CB=0xAA,1

OK

The 'CB' command sends out a continuous pattern of bits, in this case 0xAA = 0b10101010.

AT\$P=1

OK

This transitions the device into sleep mode. Out-of-band transmissions will still be triggered. The UART is powered down. The device can be woken up by a low level on the UART signal, i.e. by sending break.

Table 10. COMMANDS

Command	Name	Description												
AT	Dummy Command	Just returns 'OK' and does nothing else. Can be used to check communication.												
AT\$SB=bit[,bit]	Send Bit	Send a bit status (0 or 1). Optional bit flag indicates if AX-SFJK should receive a downlink frame.												
AT\$SF=frame[,bit]	Send Frame	Send payload data, 1 to 12 bytes. Optional bit flag indicates if AX-SFJK should receive a downlink frame.												
AT\$SO	Manually send out of band message	Send the out-of-band message.												
AT\$TR?	Get the transmit repeat	Returns the number of transmit repeats. Default: 2												
AT\$TR=?	Get transmit repeat range	Returns the allowed range of transmit repeats.												
AT\$TR=uint	Set transmit repeat	Sets the transmit repeat, sets only for transmit with downlink frame.												
AT\$uint?	Get Register	Query a specific configuration register's value. See the table "Registers" for a list of registers.												
AT\$uint=uint	Set Register	Change a configuration register.												
AT\$uint=?	Get Register Range	Returns the range of allowed register values.												
AT\$IF=uint	Set TX Frequency	Set the output carrier macro channel for Sigfox frames.												
AT\$IF?	Get TX Frequency	Get the currently chosen TX frequency.												
AT\$DR=uint	Set RX Frequency	Set the reception carrier macro channel for Sigfox frames.												
AT\$DR?	Get RX Frequency	Get the currently chosen RX frequency.												
AT\$CW=uint,bit[,uint_opt]	Continuous Wave	<p>To run emission tests for Sigfox certification it is necessary to send a continuous wave, i.e. just the base frequency without any modulation. Parameters:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Name</th> <th>Range</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Frequency</td> <td>800000000–999999999, 0</td> <td>Continuous wave frequency in Hz. Use 923200000 for Sigfox or 0 to keep previous frequency.</td> </tr> <tr> <td>Mode</td> <td>0, 1</td> <td>Enable or disable carrier wave.</td> </tr> <tr> <td>Power</td> <td>14</td> <td>dBm of signal Default: 14</td> </tr> </tbody> </table>	Name	Range	Description	Frequency	800000000–999999999, 0	Continuous wave frequency in Hz. Use 923200000 for Sigfox or 0 to keep previous frequency.	Mode	0, 1	Enable or disable carrier wave.	Power	14	dBm of signal Default: 14
Name	Range	Description												
Frequency	800000000–999999999, 0	Continuous wave frequency in Hz. Use 923200000 for Sigfox or 0 to keep previous frequency.												
Mode	0, 1	Enable or disable carrier wave.												
Power	14	dBm of signal Default: 14												
AT\$CB=uint_opt,bit	Test Mode: TX constant byte	<p>For emission testing it is useful to send a specific bit pattern. The first parameter specifies the byte to send. Use '-1' for a (pseudo-)random pattern. Parameters:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Name</th> <th>Range</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Pattern</td> <td>0–255, -1</td> <td>Byte to send. Use '-1' for a (pseudo-)random pattern.</td> </tr> <tr> <td>Mode</td> <td>0, 1</td> <td>Enable or disable pattern test mode.</td> </tr> </tbody> </table>	Name	Range	Description	Pattern	0–255, -1	Byte to send. Use '-1' for a (pseudo-)random pattern.	Mode	0, 1	Enable or disable pattern test mode.			
Name	Range	Description												
Pattern	0–255, -1	Byte to send. Use '-1' for a (pseudo-)random pattern.												
Mode	0, 1	Enable or disable pattern test mode.												
AT\$T?	Get Temperature	Measure internal temperature and return it in 1/10 th of a degree Celsius.												
AT\$V?	Get Voltages	Return current voltage and voltage measured during the last transmission in mV.												

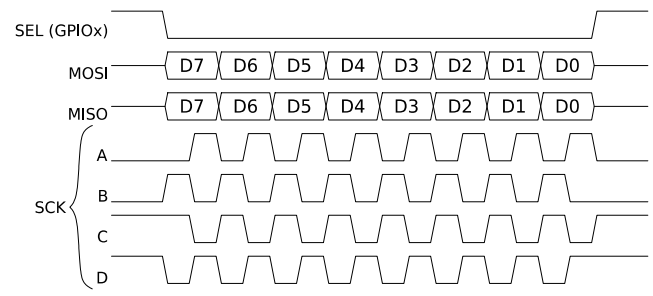
AX-SFJK, AX-SFJK-API

Table 10. COMMANDS (continued)

Command	Name	Description																		
AT\$I=uint	Information	<p>Display various product information:</p> <p>0: Software Name & Version Example Response: AX-Sigfox 1.1 RCZ3</p> <p>1: Contact Details Example Response: support@axsem.com</p> <p>2: Silicon revision lower byte Example Response: 8F</p> <p>3: Silicon revision upper byte Example Response: 51</p> <p>4: Major Firmware Version Example Response: 1</p> <p>5: Minor Firmware Version Example Response: 1</p> <p>7: Firmware Variant (Frequency Band etc. (EU/US)) Example Response: RCZ3</p> <p>9: SIGFOX Library Version Example Response: UDL1-1.8.9</p> <p>10: Device ID Example Response: 00012345</p> <p>11: PAC Example Response: 0123456789ABCDEF</p>																		
AT\$P=uint	Set Power Mode	<p>To conserve power, the AX-SFJK can be put to sleep manually. Depending on power mode, you will be responsible for waking up the AX-SFJK again!</p> <p>0: software reset (settings will be reset to values in flash)</p> <p>1: sleep (send a break to wake up)</p> <p>2: deep sleep (toggle GPIO9 or RESET_N pin to wake up; the AX-SFJK is not running and all settings will be reset!)</p>																		
AT\$WR	Save Config	<p>Write all settings to flash (RX/TX frequencies, registers) so they survive reset/deep sleep or loss of power.</p> <p>Use AT\$P=0 to reset the AX-SFJK and load settings from flash.</p>																		
AT:Pn?	Get GPIO Pin	<p>Return the setting of the GPIO Pin <i>n</i>; <i>n</i> can range from 0 to 9. A character string is returned describing the mode of the pin, followed by the actual value. If the pin is configured as analog pin, then the voltage (range 0...1 V) is returned. The mode characters have the following meaning:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Pin drives low</td> </tr> <tr> <td>1</td> <td>Pin drives high</td> </tr> <tr> <td>Z</td> <td>Pin is high impedance input</td> </tr> <tr> <td>U</td> <td>Pin is input with pull-up</td> </tr> <tr> <td>A</td> <td>Pin is analog input (GPIO pin 0...3 only)</td> </tr> <tr> <td>T</td> <td>Pin is driven by clock or DAC (GPIO pin 0 and 4 only)</td> </tr> </tbody> </table> <p>The default mode after exiting reset is U on all GPIO pins.</p>	Mode	Description	0	Pin drives low	1	Pin drives high	Z	Pin is high impedance input	U	Pin is input with pull-up	A	Pin is analog input (GPIO pin 0...3 only)	T	Pin is driven by clock or DAC (GPIO pin 0 and 4 only)				
Mode	Description																			
0	Pin drives low																			
1	Pin drives high																			
Z	Pin is high impedance input																			
U	Pin is input with pull-up																			
A	Pin is analog input (GPIO pin 0...3 only)																			
T	Pin is driven by clock or DAC (GPIO pin 0 and 4 only)																			
AT:Pn=?	Get GPIO Pin Range	<p>Print a list of possible modes for a pin. The table below lists the response.</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Pin</th> <th>Modes</th> </tr> </thead> <tbody> <tr> <td>P0</td> <td>0, 1, Z, U, A, T</td> </tr> <tr> <td>P1</td> <td>0, 1, Z, U, A</td> </tr> <tr> <td>P4</td> <td>0, 1, Z, U, T</td> </tr> <tr> <td>P5</td> <td>0, 1, Z, U</td> </tr> <tr> <td>P6</td> <td>0, 1, Z, U</td> </tr> <tr> <td>P7</td> <td>0, 1, Z, U</td> </tr> <tr> <td>P8</td> <td>0, 1, Z, U</td> </tr> <tr> <td>P9</td> <td>0, 1, Z, U</td> </tr> </tbody> </table>	Pin	Modes	P0	0, 1, Z, U, A, T	P1	0, 1, Z, U, A	P4	0, 1, Z, U, T	P5	0, 1, Z, U	P6	0, 1, Z, U	P7	0, 1, Z, U	P8	0, 1, Z, U	P9	0, 1, Z, U
Pin	Modes																			
P0	0, 1, Z, U, A, T																			
P1	0, 1, Z, U, A																			
P4	0, 1, Z, U, T																			
P5	0, 1, Z, U																			
P6	0, 1, Z, U																			
P7	0, 1, Z, U																			
P8	0, 1, Z, U																			
P9	0, 1, Z, U																			
AT:Pn=mode	Set GPIO Pin	<p>Set the GPIO pin mode.</p> <p>For a list of the modes see the command AT:Pn?</p>																		

AX-SFJK, AX-SFJK-API

Table 10. COMMANDS (continued)

Command	Name	Description															
AT:ADC Pn[-Pn[(1V 10V)]]?	Get GPIO Pin Analog Voltage	Measure the voltage applied to a GPIO pin. The command also allows measurement of the voltage difference across two GPIO pins. In differential mode, the full scale range may also be specified as 1 V or 10 V. Note however that the pin input voltages must not exceed the range 0..VDD _{IO} . The command returns the result as fraction of the full scale range (1 V if none is specified). The GPIO pins referenced should be initialized to analog mode before issuing this command.															
AT:SPI[(A B C D)]=bytes	SPI Transaction	<p>This command clocks out <i>bytes</i> on the SPI port. The clock frequency is 312.5 kHz. The command returns the bytes read on MISO during output. Optionally the clocking mode may be specified (default is A):</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Mode</th> <th>Clock Inversion</th> <th>Clock Phase</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>normal</td> <td>normal</td> </tr> <tr> <td>B</td> <td>normal</td> <td>alternate</td> </tr> <tr> <td>C</td> <td>inverted</td> <td>normal</td> </tr> <tr> <td>D</td> <td>inverted</td> <td>alternate</td> </tr> </tbody> </table>  <p>Note that SEL, if needed, is not generated by this command, and must instead be driven using standard GPIO commands (AT:Pn=0 1).</p>	Mode	Clock Inversion	Clock Phase	A	normal	normal	B	normal	alternate	C	inverted	normal	D	inverted	alternate
Mode	Clock Inversion	Clock Phase															
A	normal	normal															
B	normal	alternate															
C	inverted	normal															
D	inverted	alternate															
AT:CLK=freq,refreq	Set Clock Generator	Output a square wave on the pin(s) set to T mode. The frequency of the square wave is $(\text{freq} / 2^{16}) \times \text{refreq}$. Possible values for refreq are 20000000, 10000000, 5000000, 2500000, 1250000, 625000, 312500, 156250. Possible values for freq are 0...65535.															
AT:CLK=OFF	Turn off Clock Generator	Switch off the clock generator															
AT:CLK?	Get Clock Generator	Return the settings of the clock generator. Two numbers are returned, freq and refreq.															
AT:DAC=value	Set $\Sigma\Delta$ DAC	Output a $\Sigma\Delta$ DAC value on the pin(s) set to T mode. Parameter value may be in the range -32768...32767. The average output voltage is $(1/2 + \text{value} / 2^{17}) \times VDD$. An external low pass filter is needed to get smooth output voltages. The modulation frequency is 20 MHz. A possible low pass filter choice is a simple RC low pass filter with R = 10 k Ω and C = 1 μ F.															
AT:DAC=OFF	Turn off $\Sigma\Delta$ DAC	Switch off the DAC															
AT:DAC?	Get $\Sigma\Delta$ DAC	Return the DAC value															

AX-SFJK, AX-SFJK-API

Table 10. COMMANDS (continued)

Command	Name	Description
AT\$TM=mode,config	Activates the Sigfox Testmode	Available test modes: 0. TX BPSK Send only BPSK with Synchro Bit + Synchro frame + PN sequence: No hopping centered on the TX_frequency. Config bits 0 to 6 define the number of repetitions. Setting config bit 7 to 1 removes the delay between frames. 1. TX Protocol: Tx mode with full protocol with Sigfox key: Send Sigfox protocol frames with initiate downlink flag = True. Config defines the number of repetitions. 2. RX Protocol: This mode tests the complete downlink protocol in Downlink only. Config defines the number of repetitions. 3. RX GFSK: RX mode with known pattern with SB + SF + Pattern on RX_frequency (internal comparison with received frame ↔ known pattern = AA AA B2 27 1F 20 41 84 32 68 C5 BA AE 79 E7 F6 DD 9B. Config defines the RX on time in seconds. 4. RX Sensitivity: Does uplink + downlink frame with Sigfox key and specific timings. This test is specific to SIGFOX's test equipments & softwares. 5. TX Synthesis: Does one uplink frame on each Sigfox channel to measure frequency synthesis step
AT\$SE	Starts AT\$TM=3,255 indefinitely	Convenience command for sensitivity tests
AT\$SL[=frame]	Send local loop	Sends a local loop frame with optional payload of 1 to 12 bytes. Default payload: 0x84, 0x32, 0x68, 0xC5, 0xBA, 0x53, 0xAE, 0x79, 0xE7, 0xF6, 0xDD, 0x9B.
AT\$RL	Receive local loop	Starts listening for a local loop.

Table 11. REGISTERS

Number	Name	Description	Default	Range	Units
300	Out Of Band Period	AX-SFJK sends periodic static messages to indicate that they are alive. Set to 0 to disable.	24	0-24	hours
400	LBT Mask	LBT configurations to be used.	<1> <15000> <0>,0		
410	Encryption Key Configuration	Set to zero for normal operation. Set to one for use with the SIGFOX Network Emulator Kit (SNEK)	0	0-1	0: private key 1: public key
800	LBT RSSI Offset	Shifts the carrier sense threshold. Positive values result in a lower threshold.	0	-128-127	dB

AX-SFJK, AX-SFJK-API

APPLICATION INFORMATION

Typical Application Diagrams

Typical AX-SFJK / AX-SFJK-API Application Diagram

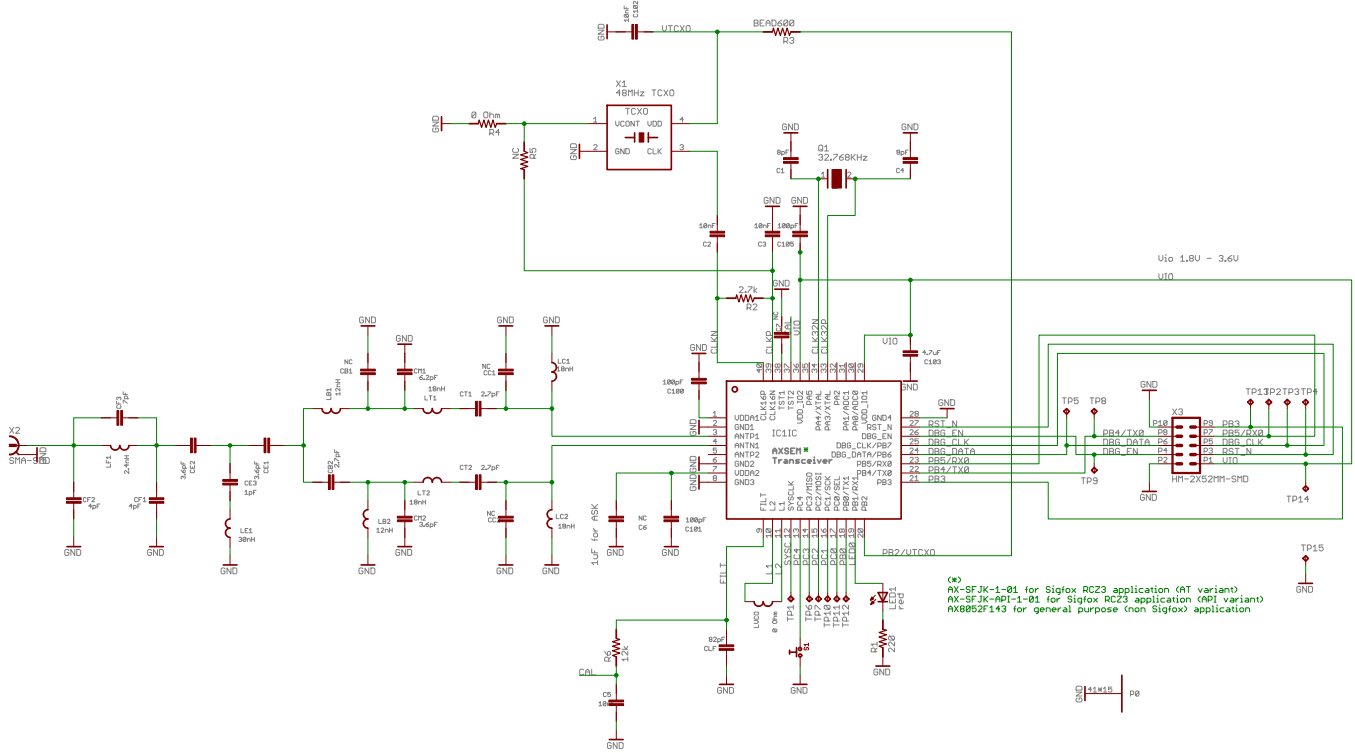


Figure 4. Typical Application Diagram

For detailed application configuration and BOM see the AX-SFJK Application Note: Sigfox Compliant Reference Design.

AX-SFJK, AX-SFJK-API

QFN40 Soldering Profile

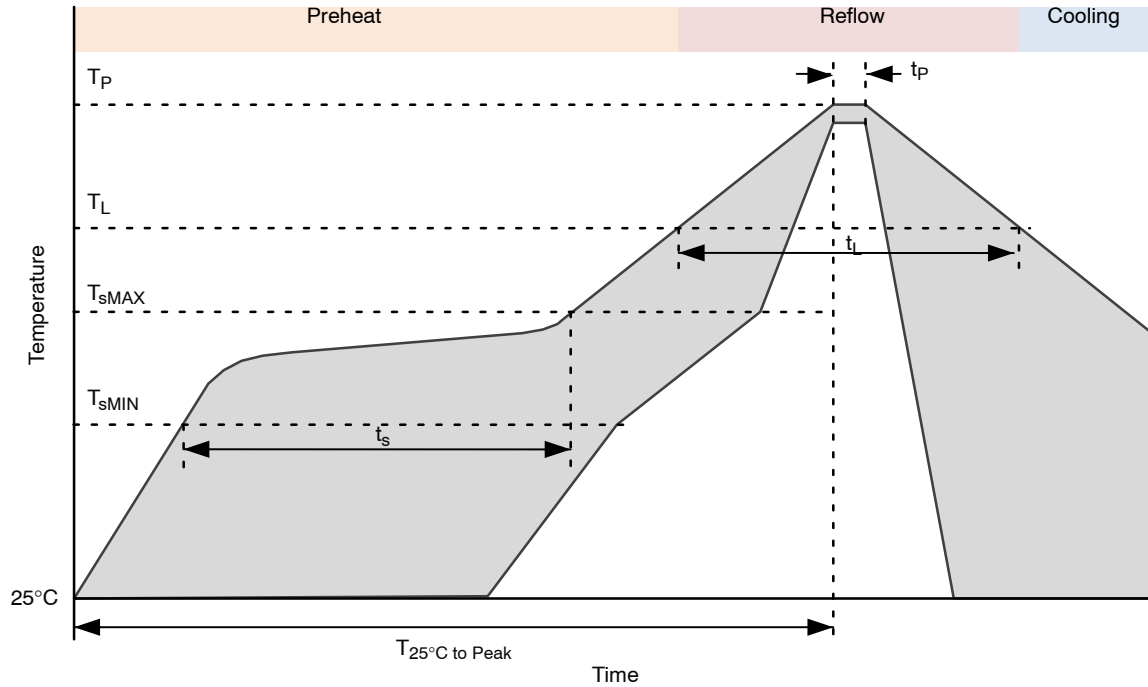


Figure 5. QFN40 Soldering Profile

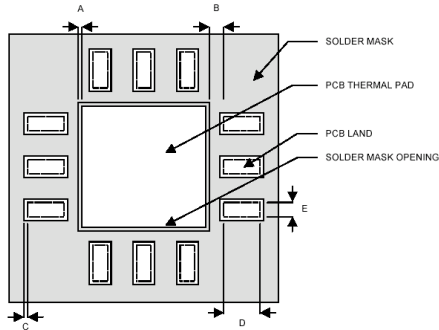
Table 12.

Profile Feature	Pb-Free Process
Average Ramp-Up Rate	3°C/s max.
Preheat Preheat	
Temperature Min	T_{sMIN} 150°C
Temperature Max	T_{sMAX} 200°C
Time (T_{sMIN} to T_{sMAX})	t_s 60–180 sec
Time 25°C to Peak Temperature	$T_{25^\circ\text{C to Peak}}$ 8 min max.
Reflow Phase	
Liquidus Temperature	T_L 217°C
Time over Liquidus Temperature	t_L 60–150 s
Peak Temperature	t_p 260°C
Time within 5°C of actual Peak Temperature	T_p 20–40 s
Cooling Phase	
Ramp-down rate	6°C/s max.

1. All temperatures refer to the top side of the package, measured on the package body surface.

QFN40 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 6.



- A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
- B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
- C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads.
- D = PCB land length = QFN solder pad length + 0.1 mm
- E = PCB land width = QFN solder pad width + 0.1 mm

Figure 6. PCB Land and Solder Mask Recommendations

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.
3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PCB under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

Assembly Process

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.

3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 7.
4. The aperture opening for the signal pads should be between 50–80% of the QFN pad area as shown in Figure 8.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.
7. No-clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water-soluble flux is used.

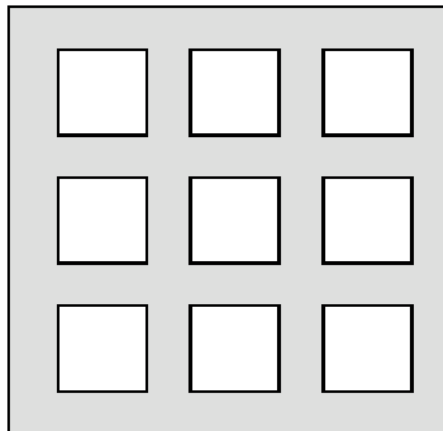


Figure 7. Solder Paste Application on Exposed Pad

AX-SFJK, AX-SFJK-API

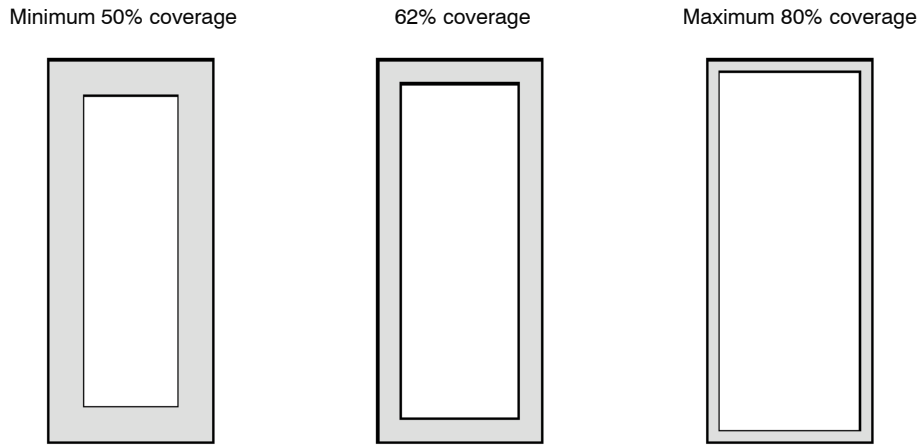


Figure 8. Solder Paste Application on Pins

Life Support Applications

This product is not designed for use in life support appliances, devices, or in systems where malfunction of this product can reasonably be expected to result in personal injury. ON Semiconductor customers using or selling this product for use in such applications do so at their own risk

and agree to fully indemnify ON Semiconductor for any damages resulting from such improper use or sale.

Device Information

The following device information can be queried using the AT-Commands AT\$I=4, AT\$I=5 for the APP version and AT\$I=2, AT\$I=3 for the chip version.

Table 13. DEVICE VERSIONS

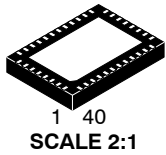
Product	Part Number	APP Version		Chip Version	
		[0]	[1]	[0]	[1]
AX-SFJK	AX-SFJK-1-01-XXXX ¹	0x01	0x01	0x8F	0x51
AX-SFJK-API	AX-SFJK-API-1-01-XXXX ¹	0x01	0x01	0x8F	0x51

1. TB05 for Reel 500, TX30 for Reel 3000 reel

MECHANICAL CASE OUTLINE

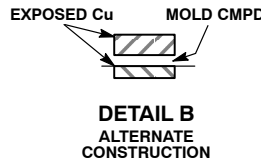
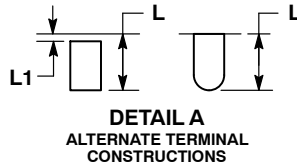
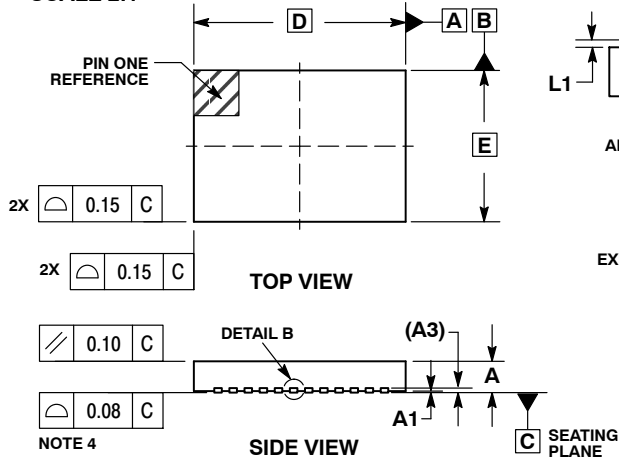
PACKAGE DIMENSIONS

ON Semiconductor®



QFN40 7x5, 0.5P
CASE 485EG
ISSUE B

DATE 26 APR 2017

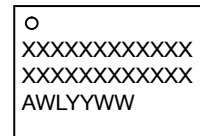


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

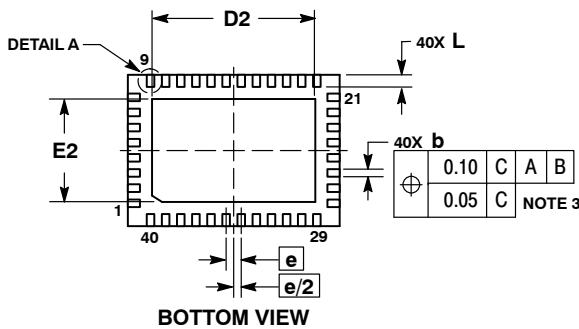
DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	7.00 BSC	
D2	5.30	5.50
E	5.00 BSC	
E2	3.30	3.50
e	0.50 BSC	
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

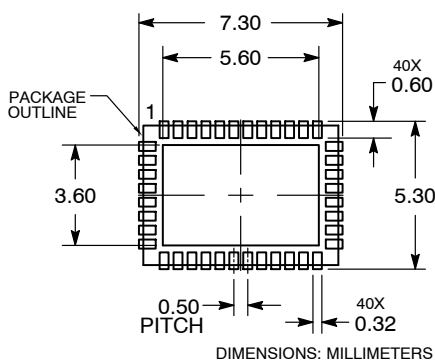


XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON04197G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	QFN40 7X5, 0.5P	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative