

# MOSFET - Single N-Channel

## 80 V, 21 mΩ, 24 A

### NTTFD021N08C

#### General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q2) and synchronous (Q1) have been designed to provide optimal power efficiency.

#### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 21 mΩ at  $V_{GS} = 10$  V,  $I_D = 7.8$  A
- Max  $r_{DS(on)}$  = 55 mΩ at  $V_{GS} = 6$  V,  $I_D = 3.9$  A

Q2: N-Channel

- Max  $r_{DS(on)}$  = 21 mΩ at  $V_{GS} = 10$  V,  $I_D = 7.8$  A
- Max  $r_{DS(on)}$  = 55 mΩ at  $V_{GS} = 6$  V,  $I_D = 3.9$  A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- RoHS Compliant

#### Applications

- Computing
- Communications
- General Purpose Point of Load

#### PIN DESCRIPTION

Pin	Name	Description
1, 11, 12	GND (LSS)	Low Side Source
2	LSG	Low Side Gate
3, 4, 5, 6	V + (HSD)	High Side Drain
7	HSG	High Side Gate
8, 9, 10	SW	Switching Node, Low Side Drain

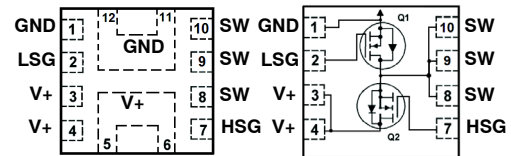


ON Semiconductor®

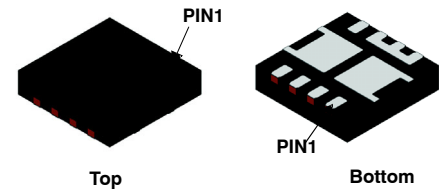
[www.onsemi.com](http://www.onsemi.com)

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
80 V	21 mΩ @ 10 V	24 A
	55 mΩ @ 6 V	

#### ELECTRICAL CONNECTION

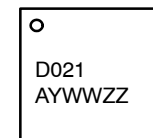


Dual N-Channel MOSFET



Power Clip 33 Symmetric (WQFN12)  
CASE 510CJ

#### MARKING DIAGRAM



D021 = Specific Device Code  
A = Assembly Plant Code  
Y = Numeric Year Code  
WW = Work Week Code  
ZZ = Assembly Lot Code

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NTTFD021N08C

## ORDERING INFORMATION AND PACKAGE MARKING

Device	Marking	Package	Shipping <sup>†</sup>
NTTFD021N08C	D021	WQFN12 (Pb-Free)	3000 Units/ Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MOSFET MAXIMUM RATINGS (T<sub>A</sub> = 25°C, Unless otherwise specified)

Symbol	Parameter	Q1	Q2	Units
V <sub>DS</sub>	Drain-to-Source Voltage	80	80	V
V <sub>GS</sub>	Gate-to-Source Voltage	±20	±20	V
I <sub>D</sub>	Drain Current –Continuous T <sub>C</sub> = 25°C (Note 4)	24	24	A
	–Continuous T <sub>C</sub> = 100°C (Note 4)	15	15	
	–Continuous T <sub>A</sub> = 25°C	6 (Note 1a)	6 (Note 1b)	
	–Pulsed T <sub>A</sub> = 25°C	349	349	
E <sub>AS</sub>	Single Pulse Avalanche Energy (L = 1 mH, I <sub>L(pk)</sub> = 7.9 A) (Note 3)	31	31	mJ
P <sub>D</sub>	Power Dissipation for Single Operation T <sub>C</sub> = 25°C	26	26	W
	Power Dissipation for Single Operation T <sub>A</sub> = 25°C	1.7 (Note 1a)	1.7 (Note 1b)	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +150		°C
T <sub>L</sub>	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	4.8	4.8	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	70 (Note 1a)	70 (Note 1b)	
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	135 (Note 1c)	135 (Note 1c)	

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	Q1	80			V
		I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	Q2	80			
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	Q1		68.2		mV/°C
		I <sub>D</sub> = 250 μA, referenced to 25°C	Q2		68.2		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	Q1			1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	Q2			1	
I <sub>GSS</sub>	Gate-to-Source Leakage Current, Forward	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	Q1			±100	nA
		V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	Q2			±100	

# NTTFD021N08C

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>ON CHARACTERISTICS</b>							
V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 44 μA	Q1	2	2.8	4	V
		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 44 μA	Q2	2	2.8	4	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate-to-Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 44 μA, referenced to 25°C	Q1		-8.86		mV/°C
		I <sub>D</sub> = 44 μA, referenced to 25°C	Q2		-8.86		
r <sub>DS(on)</sub>	Drain-to-Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.8 A	Q1		16.4	21	mΩ
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 3.9 A			26	55	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.8 A, T <sub>J</sub> = 125°C			28.9		
r <sub>DS(on)</sub>	Drain-to-Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.8 A	Q2		16.4	21	mΩ
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 3.9 A			26	55	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.8 A, T <sub>J</sub> = 125°C			28.9		
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 7.8 A	Q1		227		S
		V <sub>DS</sub> = 5 V, I <sub>D</sub> = 7.8 A	Q2		227		

## DYNAMIC CHARACTERISTICS

C <sub>ISS</sub>	Input Capacitance	Q1: V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 Mhz  Q2: V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz	Q1		572		pF
			Q2		572		
C <sub>OSS</sub>	Output Capacitance		Q1		227		pF
			Q2		227		
C <sub>RSS</sub>	Reverse Transfer Capacitance		Q1		11		pF
			Q2		11		
R <sub>G</sub>	Gate Resistance	T <sub>A</sub> = 25°C	Q1		0.6		Ω
			Q2		0.6		

## SWITCHING CHARACTERISTICS

t <sub>d(ON)</sub>	Turn-On Delay Time	Q1: V <sub>DD</sub> = 40 V, I <sub>D</sub> = 7.8 A, R <sub>GEN</sub> = 6 Ω  Q2: V <sub>DD</sub> = 40 V, I <sub>D</sub> = 7.8 A, R <sub>GEN</sub> = 6 Ω	Q1		8		ns	
			Q2		8			
t <sub>r</sub>	Rise Time		Q1		2		ns	
			Q2		2			
t <sub>d(OFF)</sub>	Turn-Off Delay Time		Q1		12		ns	
			Q2		12			
t <sub>f</sub>	Fall Time		Q1		3		ns	
			Q2		3			
Q <sub>g</sub>	Total Gate Charge		V <sub>GS</sub> = 0 V to 10 V	Q1		8.4		nC
				Q2		8.4		
Q <sub>g</sub>	Total Gate Charge		V <sub>GS</sub> = 0 V to 6 V	Q1		5.5		nC
				Q2		5.5		
Q <sub>gs</sub>	Gate-to-Source Gate Charge	Q1: V <sub>DD</sub> = 40 V, I <sub>D</sub> = 7.8 A Q2: V <sub>DD</sub> = 40 V, I <sub>D</sub> = 7.8 A	Q1		2.5		nC	
			Q2		2.5			
Q <sub>gd</sub>	Gate-to-Drain "Miller" Charge	Q1: V <sub>DD</sub> = 40 V, I <sub>D</sub> = 7.8 A Q2: V <sub>DD</sub> = 40 V, I <sub>D</sub> = 7.8 A	Q1		1.8		nC	
			Q2		1.8			

# NTTFD021N08C

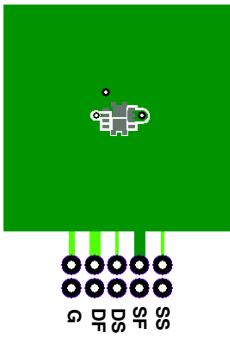
## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>							
$V_{SD}$	Source-to-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 7.8\text{ A}$ (Note 2)	Q1		0.82	1.5	V
		$V_{GS} = 0\text{ V}, I_S = 7.8\text{ A}$ (Note 2)	Q2		0.82	1.5	
$t_{rr}$	Reverse Recovery Time	Q1: $I_F = 7.8\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$ Q2: $I_F = 7.8\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1		31		ns
			Q2		31		
$Q_{rr}$	Reverse Recovery Charge	$I_F = 7.8\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1		33		nC
			Q2		33		
$t_{rr}$	Reverse Recovery Time	Q1: $I_F = 7.8\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$ Q2: $I_F = 7.8\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$	Q1		13		ns
			Q2		13		
$Q_{rr}$	Reverse Recovery Charge	$I_F = 7.8\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$	Q1		88		nC
			Q2		88		

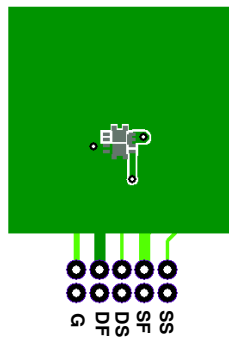
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

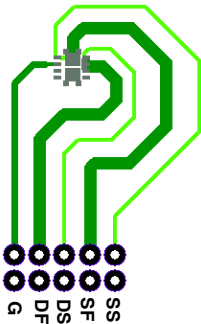
- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



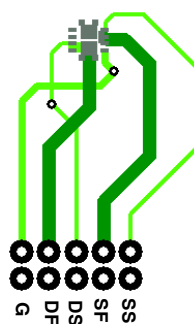
a) 70°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 70°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



c) 135°C/W when mounted on a minimum pad of 2 oz copper.



d) 135°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- Q1:  $E_{AS}$  of 31 mJ is based on starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 1\text{ mH}, I_{AS} = 7.9\text{ A}, V_{DD} = 80\text{ V}, V_{GS} = 15\text{ V}$ . 100% test at  $L = 1\text{ mH}, I_{AS} = 8\text{ A}$ .
- Q2:  $E_{AS}$  of 31 mJ is based on starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 1\text{ mH}, I_{AS} = 7.9\text{ A}, V_{DD} = 80\text{ V}, V_{GS} = 15\text{ V}$ . 100% test at  $L = 1\text{ mH}, I_{AS} = 8\text{ A}$ .
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

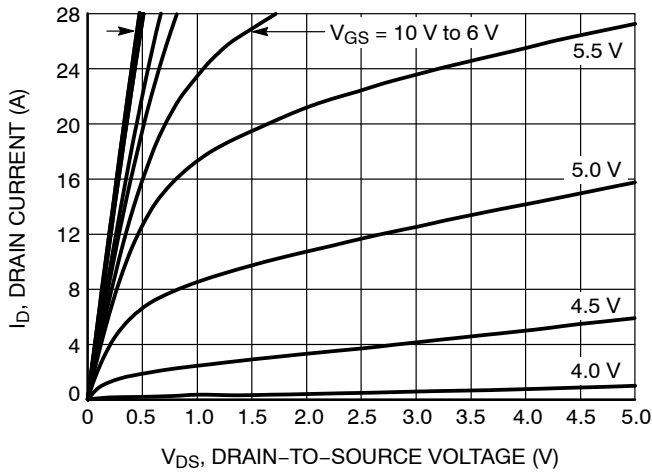


Figure 1. On-Region Characteristics

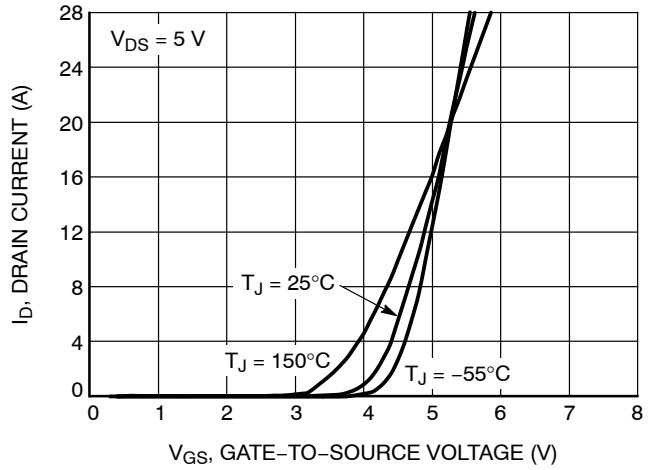


Figure 2. Transfer Characteristics

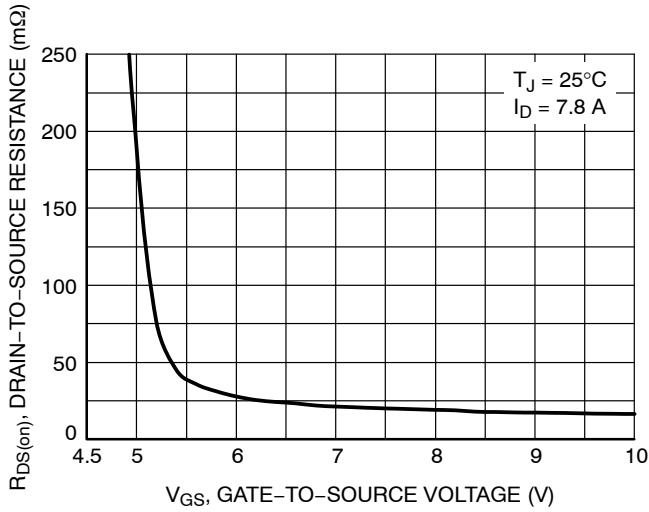


Figure 3. On-Resistance vs. Gate-to-Source Voltage

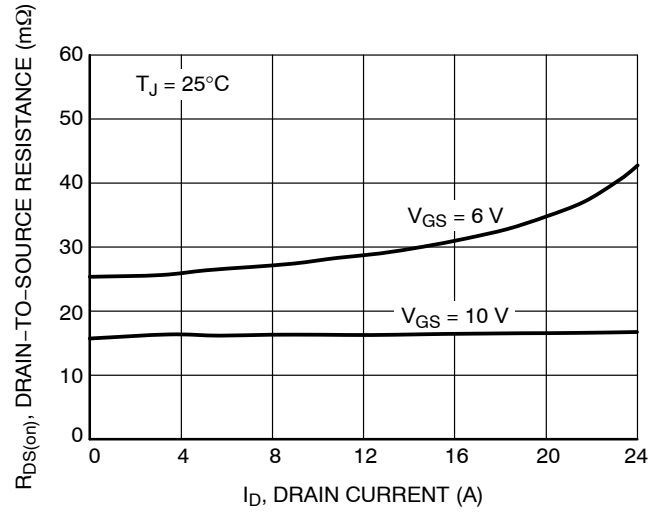


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

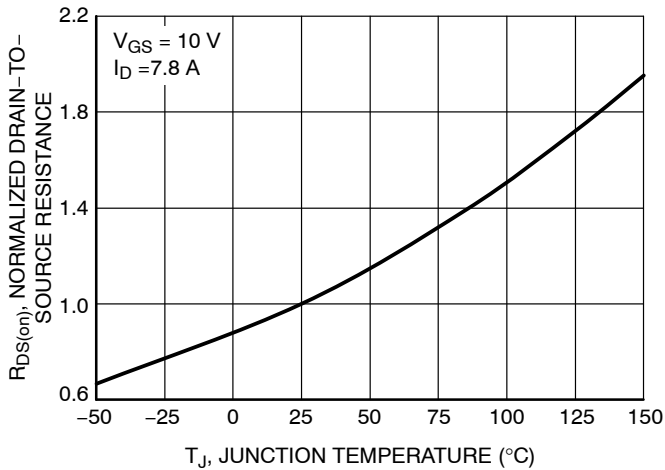


Figure 5. On-Resistance Variation with Temperature

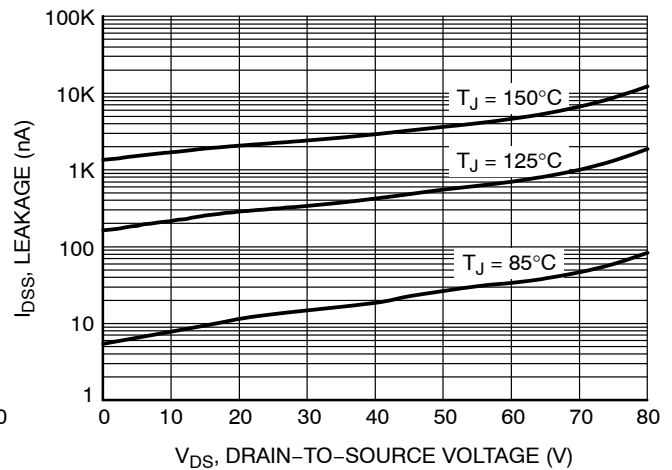


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

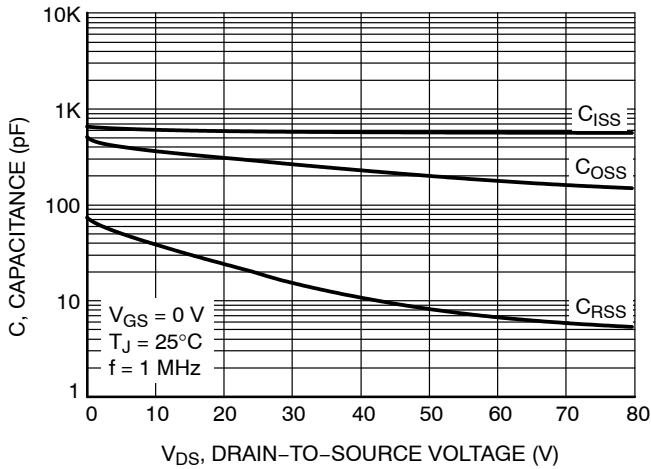


Figure 7. Capacitance Variation

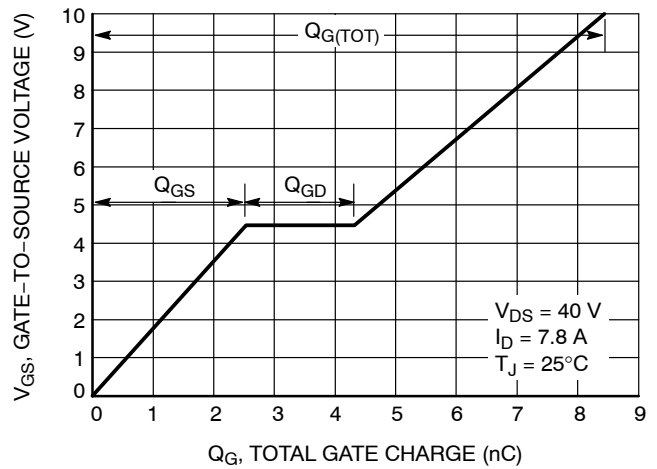


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

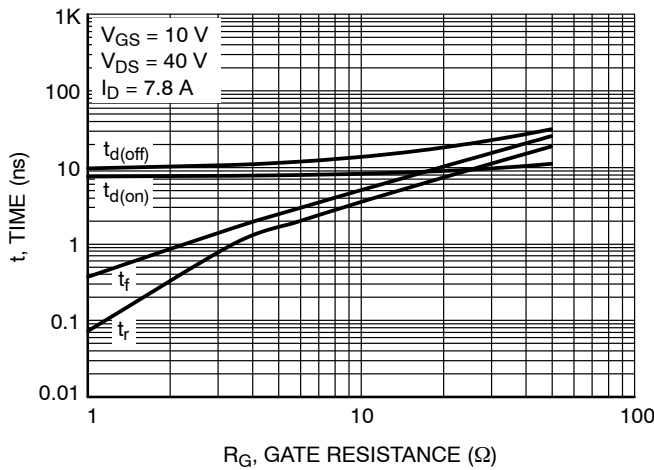


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

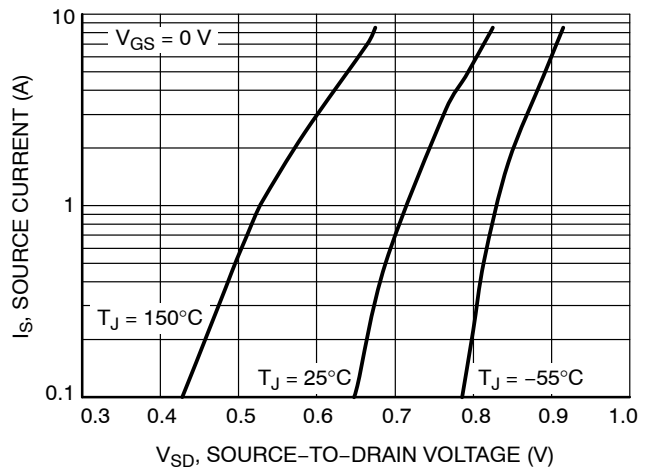


Figure 10. Diode Forward Voltage vs. Current

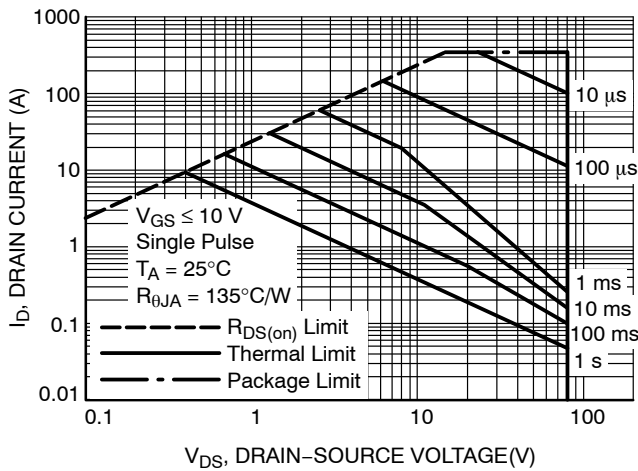


Figure 11. Safe Operating Area

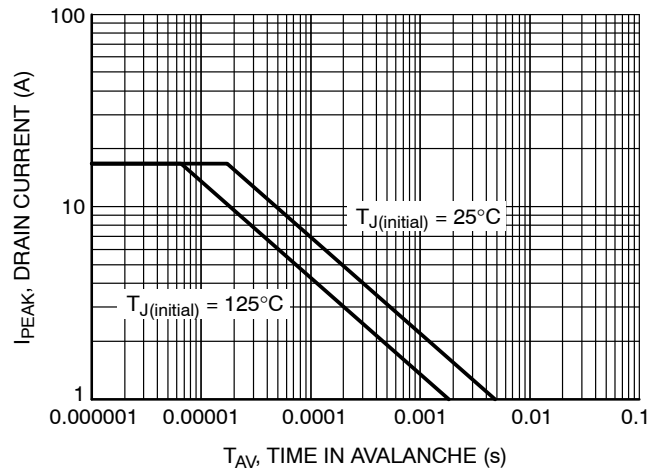


Figure 12. IPEAK vs. Time in Avalanche

TYPICAL CHARACTERISTICS

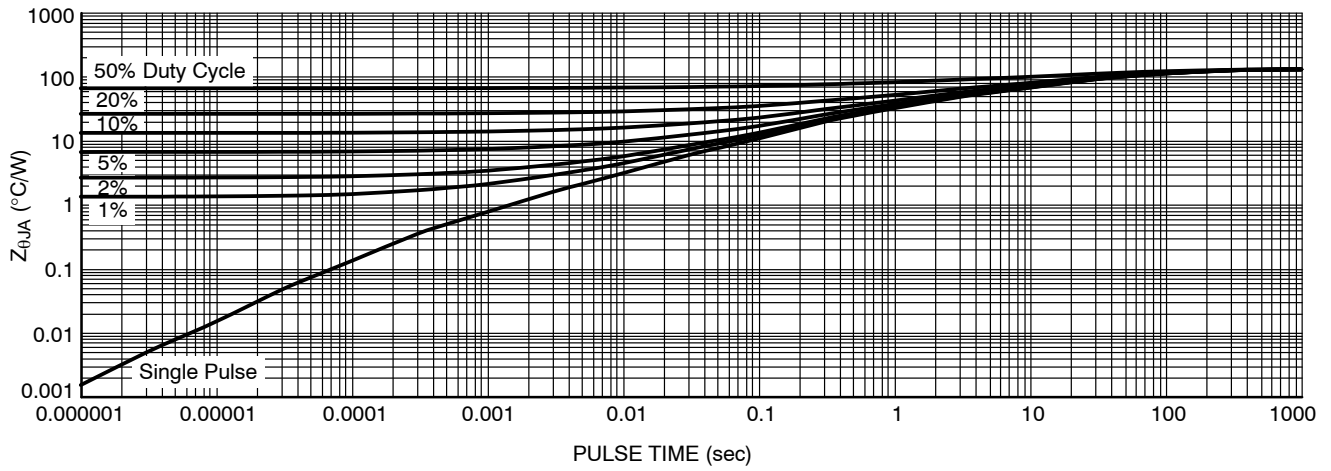
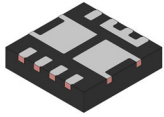


Figure 13. Thermal Characteristics

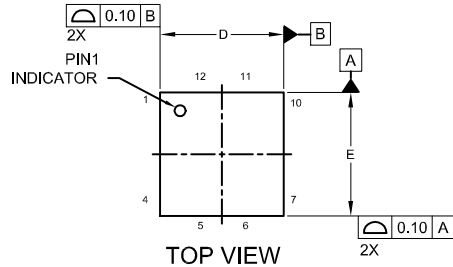
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

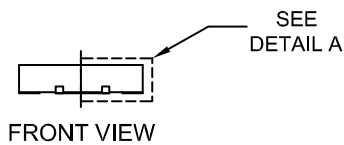


**WQFN12 3.3X3.3, 0.65P**  
**CASE 510CJ**  
**ISSUE A**

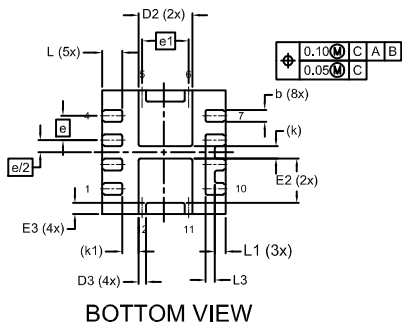
DATE 08 AUG 2022



TOP VIEW

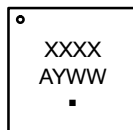


FRONT VIEW



BOTTOM VIEW

### GENERIC MARKING DIAGRAM\*

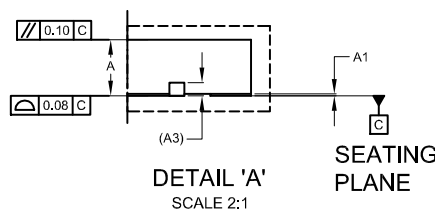


- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

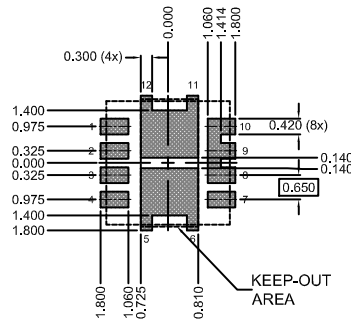
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
5. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DETAIL 'A'

SCALE 2:1



### LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	1.34	1.44	1.54
D3	0.10	0.20	0.30
E	3.20	3.30	3.40
E2	1.09	1.19	1.29
E3	0.20	0.30	0.40
e	0.65 BSC		
e/2	0.325 BSC		
e1	1.24 BSC		
k	0.33 REF		
k1	0.43 REF		
L	0.44	0.54	0.64
L1	0.19	0.29	0.39
L3	0.15	0.25	0.35

<b>DOCUMENT NUMBER:</b>	<b>98AON13806G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WQFN12 3.3X3.3, 0.65P</b>	<b>PAGE 1 OF 1</b>

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative