

MOSFET - Power, Single N-Channel

80 V, 1.1 mΩ, 335 A



ON Semiconductor®

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NTMTS1D2N08H

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|--|--|---------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DSS} | 80 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3) | Steady State | $T_C = 25^\circ\text{C}$ | I_D 335 | A |
| | | $T_C = 100^\circ\text{C}$ | 237 | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | Steady State | $T_C = 25^\circ\text{C}$ | P_D 300 | W |
| | | $T_C = 100^\circ\text{C}$ | 150 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3) | Steady State | $T_A = 25^\circ\text{C}$ | I_D 41 | A |
| | | $T_A = 100^\circ\text{C}$ | 29 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_A = 25^\circ\text{C}$ | P_D 5 | W |
| | | $T_A = 100^\circ\text{C}$ | 2.5 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} 900 | A | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 335 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($L = 3 \text{ mH}, I_{L(pk)} = 34 \text{ A}$) | E_{AS} | 1734 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

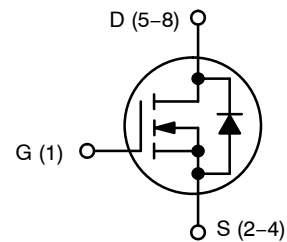
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

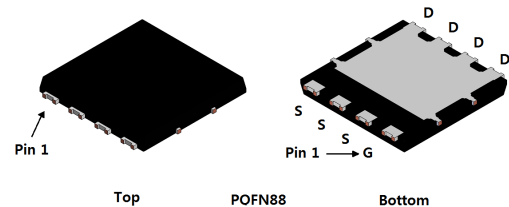
| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case - Steady State | $R_{\theta JC}$ | 0.5 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient - Steady State (Note 2) | $R_{\theta JA}$ | 30 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

| $V_{(BR)DSS}$ | $R_{DS(ON) MAX}$ | $I_D MAX$ |
|---------------|------------------|-----------|
| 80 V | 1.1 mΩ @ 10 V | 335 A |

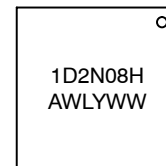


N-CHANNEL MOSFET



DFNW8 CASE 507AP

MARKING DIAGRAM



- A = Assembly Location
- WL = 2-digit Wafer Lot Code
- Y = Year Code
- WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|--------------------------------------|--|------------------------|----|-----|-------|
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 80 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} /T _J | | | 57 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 80 V | T _J = 25 °C | | 10 | μA |
| | | | T _J = 125°C | | 250 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = 20 V | | | 100 | nA |

ON CHARACTERISTICS (Note 4)

| | | | | | | |
|-----------------------------------|-------------------------------------|---|-----------------------|------|-----|-------|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 590 μA | 2.0 | 2.9 | 4.0 | V |
| Threshold Temperature Coefficient | V _{GS(TH)} /T _J | | | -7.6 | | mV/°C |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 90 A | 0.93 | 1.1 | mΩ |
| | | V _{GS} = 6 V | I _D = 59 A | 1.28 | 1.6 | |
| Forward Transconductance | g _{FS} | V _{DS} = 15 V, I _D = 90 A | | 400 | | S |

CHARGES, CAPACITANCES & GATE RESISTANCE

| | | | | | | |
|------------------------------|---------------------|---|--|-------|--|----|
| Input Capacitance | C _{ISS} | V _{GS} = 0 V, f = 500 kHz, V _{DS} = 40 V | | 10100 | | pF |
| Output Capacitance | C _{OSS} | | | 1455 | | |
| Reverse Transfer Capacitance | C _{RSS} | | | 43 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 64 V; I _D = 90 A | | 147 | | nC |
| Threshold Gate Charge | Q _{G(TH)} | | | 27 | | |
| Gate-to-Source Charge | Q _{GS} | | | 41 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 32 | | |
| Plateau Voltage | V _{GP} | | | 4 | | |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---------------------|---------------------|---|--|----|--|----|
| Turn-On Delay Time | t _{d(ON)} | V _{GS} = 10 V, V _{DS} = 64 V, I _D = 90 A, R _G = 2.5 Ω | | 29 | | ns |
| Rise Time | t _r | | | 14 | | |
| Turn-Off Delay Time | t _{d(OFF)} | | | 66 | | |
| Fall Time | t _f | | | 19 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | |
|-------------------------|-----------------|--|------------------------|-----|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 90 A | T _J = 25°C | 0.8 | 1.2 | V |
| | | | T _J = 125°C | 0.6 | | |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 90 A | | 84 | | ns |
| Reverse Recovery Charge | Q _{RR} | | | 189 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

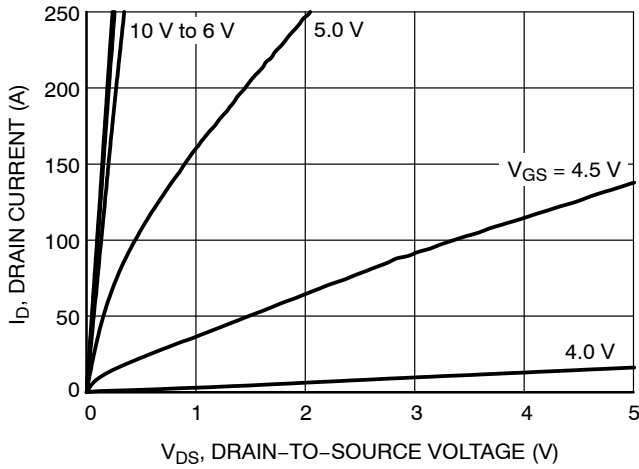


Figure 1. On-Region Characteristics

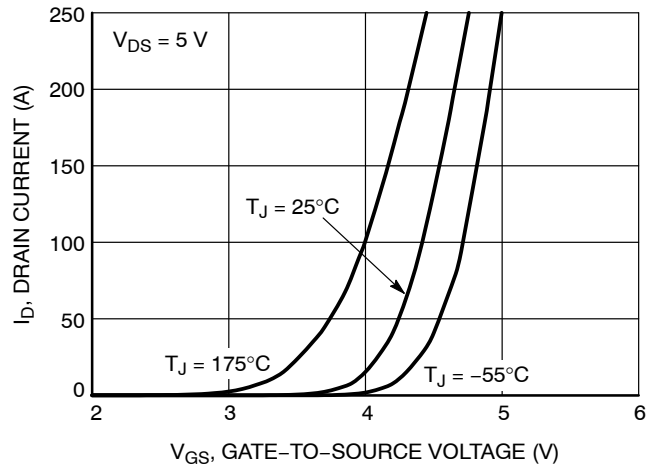


Figure 2. Transfer Characteristics

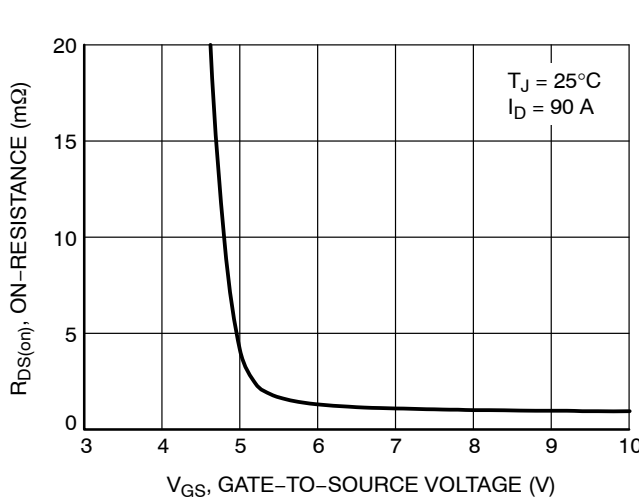


Figure 3. On-Resistance vs. Gate-to-Source Voltage

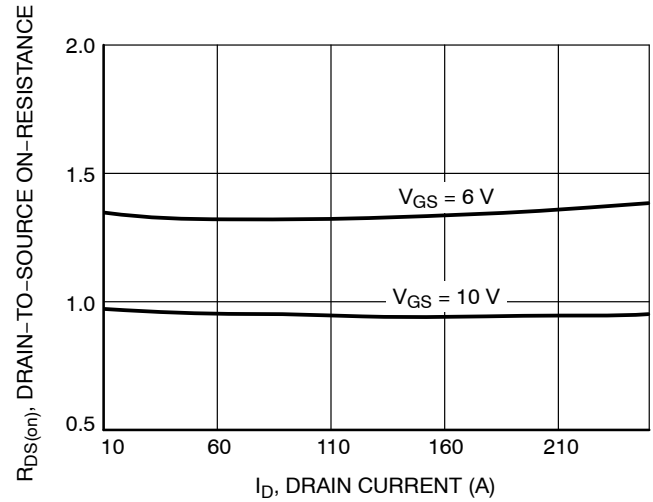


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

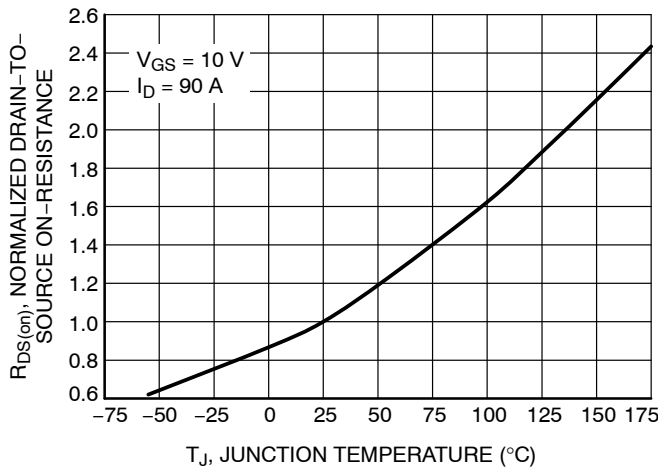


Figure 5. On-Resistance Variation with Temperature

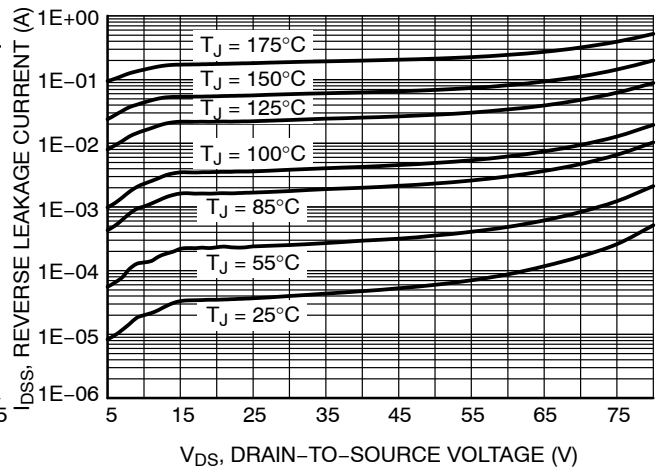


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

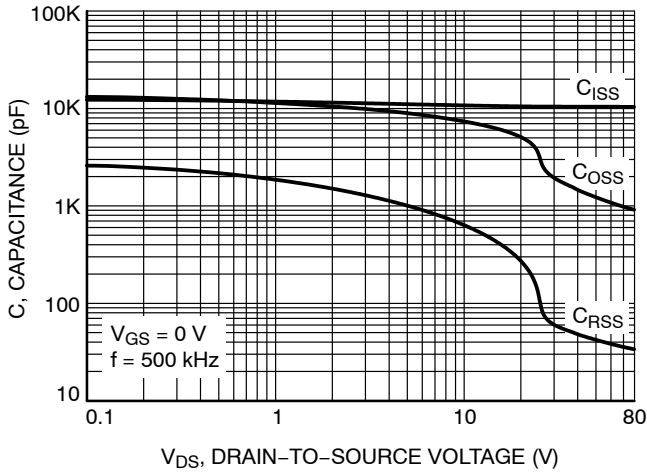


Figure 7. Capacitance Variation

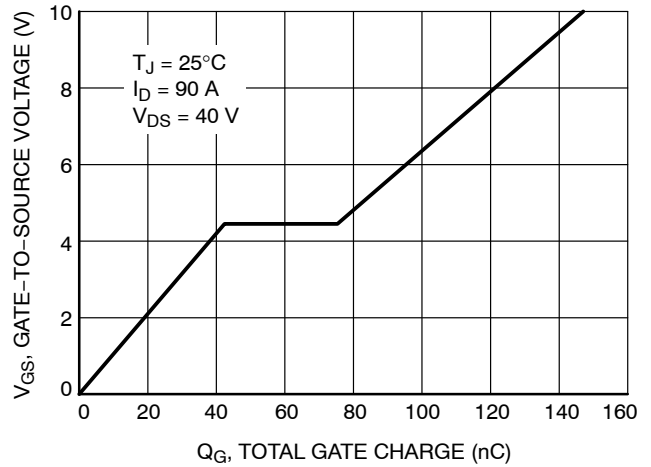


Figure 8. Gate-to-Source Voltage vs. Total Charge

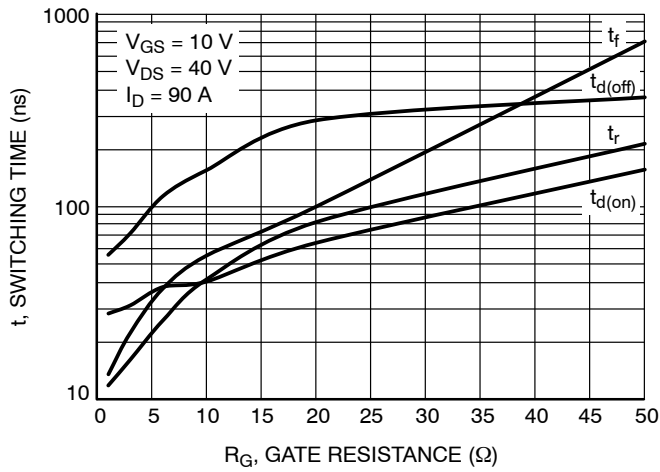


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

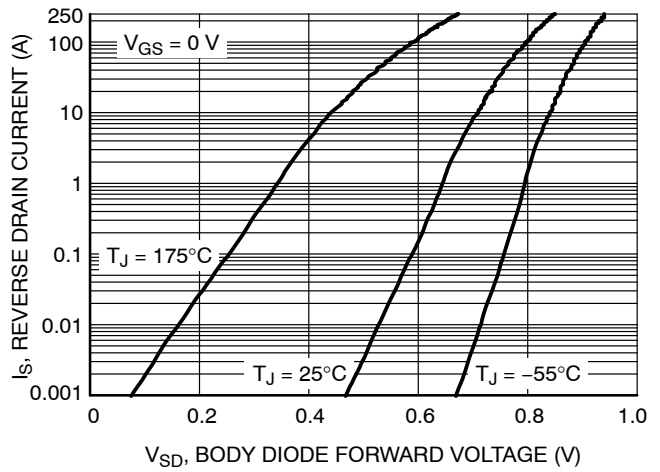


Figure 10. Diode Forward Voltage vs. Current

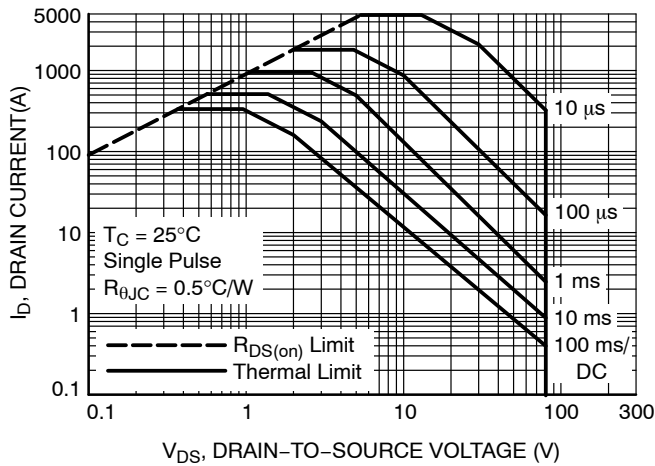


Figure 11. Maximum Rated Forward Biased Safe Operating Area

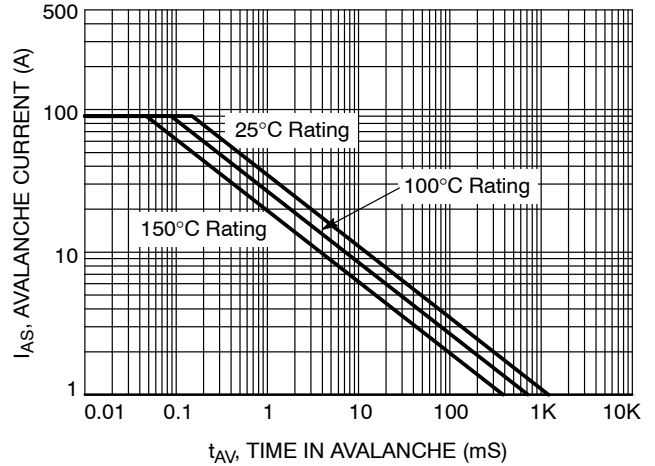


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

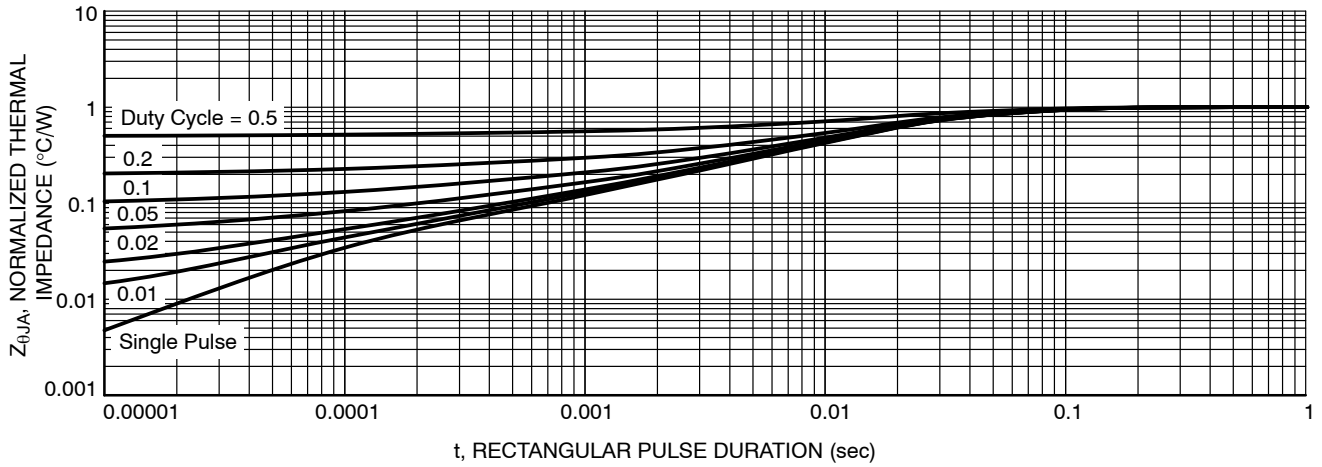


Figure 13. Transient Thermal Impedance

DEVICE ORDERING INFORMATION

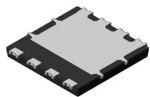
| Device | Marking | Package | Shipping† |
|--------------|--------------|--------------------|--------------------|
| NTMTS1D2N08H | NTMTS1D2N08H | DFNW8 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

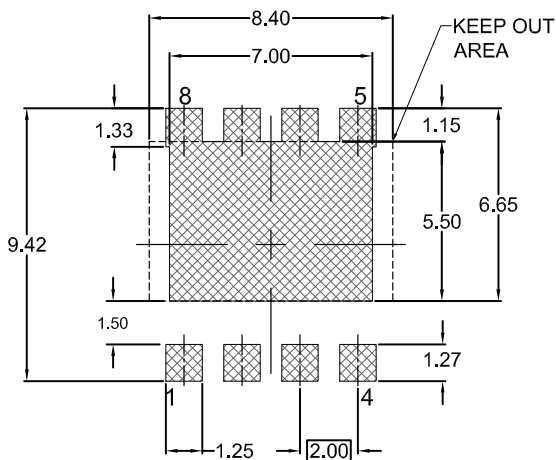
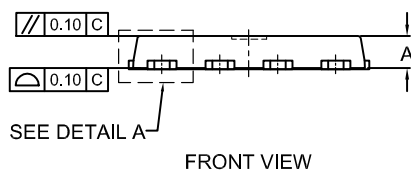
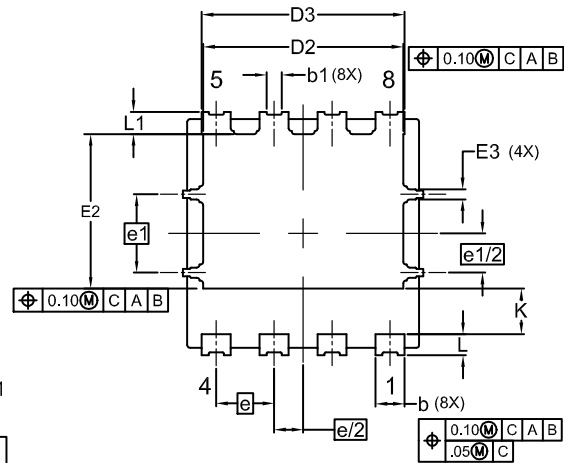
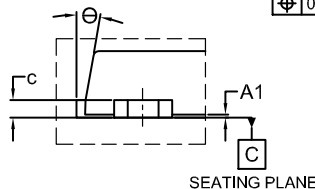
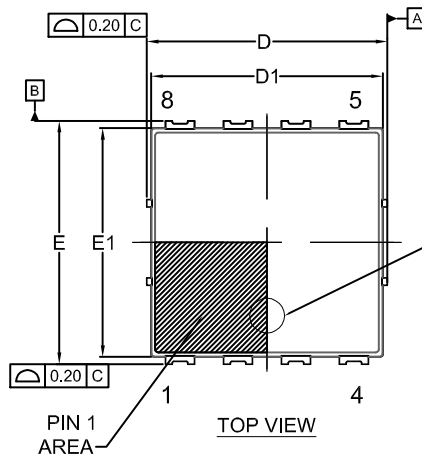
PACKAGE DIMENSIONS

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TDFNW8 8.3x8.4, 2.0P, SINGLE COOL CASE 507AP ISSUE D

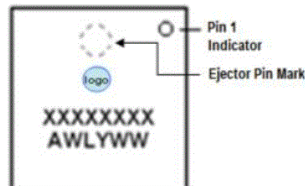
DATE 29 MAR 2021



RECOMMENDED LAND PATTERN*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | | |
|------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 1.00 | 1.10 | 1.20 |
| A1 | 0.00 | --- | 0.05 |
| b | 0.90 | 1.00 | 1.10 |
| b1 | 0.35 | 0.45 | 0.55 |
| c | 0.23 | 0.28 | 0.33 |
| D | 8.20 | 8.30 | 8.40 |
| D1 | 7.90 | 8.00 | 8.10 |
| D2 | 6.80 | 6.90 | 7.00 |
| D3 | 6.90 | 7.00 | 7.10 |
| E | 8.30 | 8.40 | 8.50 |
| E1 | 7.80 | 7.90 | 8.00 |
| E2 | 5.24 | 5.34 | 5.44 |
| E3 | 0.25 | 0.35 | 0.45 |
| e | 2.00 BSC | | |
| e/2 | 1.00 BSC | | |
| e1 | 2.70 BSC | | |
| e1/2 | 1.35 BSC | | |
| K | 1.50 | 1.57 | 1.70 |
| L | 0.64 | 0.74 | 0.84 |
| L1 | 0.67 | 0.77 | 0.87 |
| Θ | 0° | --- | 12° |

| | | |
|-------------------------|--|--|
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| DESCRIPTION: | TDFNW8 8.3x8.4, 2.0P, SINGLE COOL | PAGE 1 OF 1 |

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