# NSS40601CF8T1G

# 40 V, 8.0 A, Low $V_{CE(sat)}$ NPN Transistor

ON Semiconductor's $e^2$PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows $e^2$PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

- This is a Pb-Free Device

## MAXIMUM RATINGS ($T_A$ = 25°C)

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | 40 | Vdc |
| Collector-Base Voltage | $V_{CBO}$ | 40 | Vdc |
| Emitter-Base Voltage | $V_{EBO}$ | 6.0 | Vdc |
| Collector Current - Continuous | $I_C$ | 6.0 | Adc |
| Collector Current - Peak | $I_{CM}$ | 8.0 | A |
| Electrostatic Discharge | ESD | HBM Class 3B MM Class C | |

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation, $T_A$ = 25°C<br>Derate above 25°C | $P_D$ (Note 1) | 830<br>6.7 | mW<br>mW/°C |
| Thermal Resistance,<br>Junction-to-Ambient | $R_{\theta JA}$ (Note 1) | 150 | °C/W |
| Total Device Dissipation, $T_A$ = 25°C<br>Derate above 25°C | $P_D$ (Note 2) | 1.4<br>11.1 | W<br>mW/°C |
| Thermal Resistance,<br>Junction-to-Ambient | $R_{\theta JA}$ (Note 2) | 90 | °C/W |
| Thermal Resistance,<br>Junction-to-Lead #1 | $R_{\theta JL}$ (Note 2) | 15 | °C/W |
| Junction and Storage<br>Temperature Range | $T_J$, $T_{stg}$ | -55 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
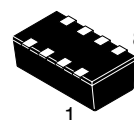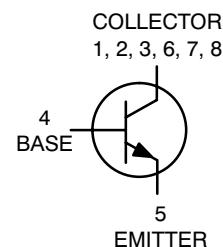1. FR-4 @ 100 mm$^2$, 1 oz copper traces.
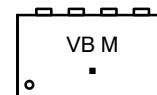2. FR-4 @ 500 mm$^2$, 1 oz copper traces.

## ON Semiconductor®

**40 VOLTS, 8.0 AMPS**
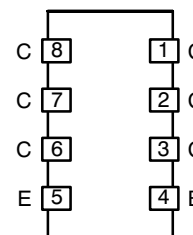**NPN LOW $V_{CE(sat)}$ TRANSISTOR**
**EQUIVALENT $R_{DS(on)}$ 31 mΩ**



COLLECTOR
1, 2, 3, 6, 7, 8

4
BASE

5
EMITTER



**ChipFET™**
**CASE 1206A**
**STYLE 4**

## MARKING DIAGRAM



VB M

VB = Specific Device Code
M = Month Code
■ = Pb-Free Package

## PIN CONNECTIONS



C [8]       [1] C
C [7]       [2] C
C [6]       [3] C
E [5]       [4] B

## ORDERING INFORMATION

| Device | Package | Shipping[†] |
|---|---|---|
| NSS40601CF8T1G | ChipFET (Pb-Free) | 3000/ Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NSS40601CF8T1G

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector-Emitter Breakdown Voltage ($I_C$ = 10 mAdc, $I_B$ = 0) | $V_{(BR)CEO}$ | 40 | - | - | Vdc |
| Collector-Base Breakdown Voltage ($I_C$ = 0.1 mAdc, $I_E$ = 0) | $V_{(BR)CBO}$ | 40 | - | - | Vdc |
| Emitter-Base Breakdown Voltage ($I_E$ = 0.1 mAdc, $I_C$ = 0) | $V_{(BR)EBO}$ | 6.0 | - | - | Vdc |
| Collector Cutoff Current ($V_{CB}$ = 40 Vdc, $I_E$ = 0) | $I_{CBO}$ | - | - | 0.1 | μAdc |
| Emitter Cutoff Current ($V_{EB}$ = 6.0 Vdc) | $I_{EBO}$ | - | - | 0.1 | μAdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain (Note 3) ($I_C$ = 10 mA, $V_{CE}$ = 2.0 V) ($I_C$ = 500 mA, $V_{CE}$ = 2.0 V) ($I_C$ = 1.0 A, $V_{CE}$ = 2.0 V) ($I_C$ = 2.0 A, $V_{CE}$ = 2.0 V) ($I_C$ = 3.0 A, $V_{CE}$ = 2.0 V) | $h_{FE}$ | 200 200 200 200 200 | - - 395 - - | - - - - - | |
| Collector-Emitter Saturation Voltage (Note 3) ($I_C$ = 0.1 A, $I_B$ = 0.010 A) ($I_C$ = 1.0 A, $I_B$ = 0.100 A) ($I_C$ = 1.0 A, $I_B$ = 0.010 A) ($I_C$ = 2.0 A, $I_B$ = 0.020 A) ($I_C$ = 3.0 A, $I_B$ = 0.030 A) ($I_C$ = 4.0 A, $I_B$ = 0.400 A) | $V_{CE(sat)}$ | - - - - - - | 0.008 0.031 0.060 0.075 0.100 0.090 | 0.010 0.075 0.075 0.110 0.150 0.135 | V |
| Base-Emitter Saturation Voltage (Note 3) ($I_C$ = 1.0 A, $I_B$ = 0.01 A) | $V_{BE(sat)}$ | - | 0.760 | 0.900 | V |
| Base-Emitter Turn-on Voltage (Note 3) ($I_C$ = 2.0 A, $V_{CE}$ = 2.0 V) | $V_{BE(on)}$ | - | 0.720 | 0.900 | V |
| Cutoff Frequency ($I_C$ = 100 mA, $V_{CE}$ = 5.0 V, f = 100 MHz) | $f_T$ | 140 | - | - | MHz |
| Input Capacitance ($V_{EB}$ = 0.5 V, f = 1.0 MHz) | Cibo | - | - | 1200 | pF |
| Output Capacitance ($V_{CB}$ = 3.0 V, f = 1.0 MHz) | Cobo | - | - | 100 | pF |
| **SWITCHING CHARACTERISTICS** | | | | | |
| Delay ($V_{CC}$ = 30 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_d$ | - | - | 110 | ns |
| Rise ($V_{CC}$ = 30 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_r$ | - | - | 130 | ns |
| Storage ($V_{CC}$ = 30 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_s$ | - | - | 1400 | ns |
| Fall ($V_{CC}$ = 30 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_f$ | - | - | 130 | ns |

3. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.
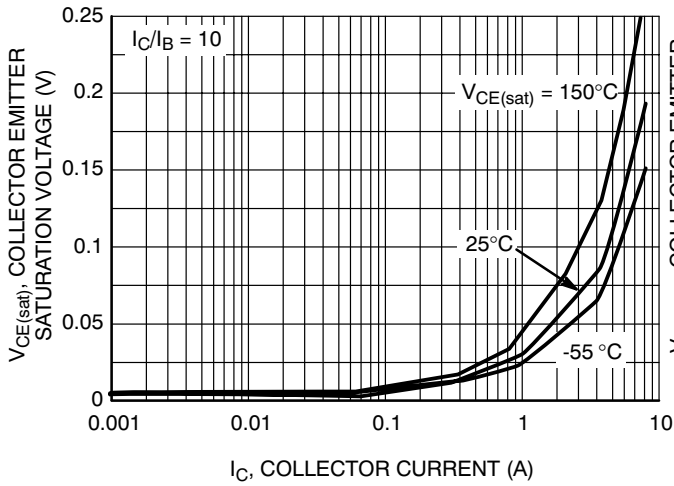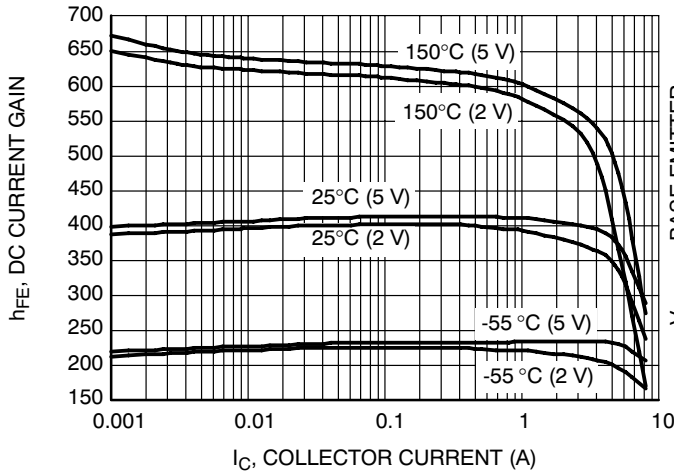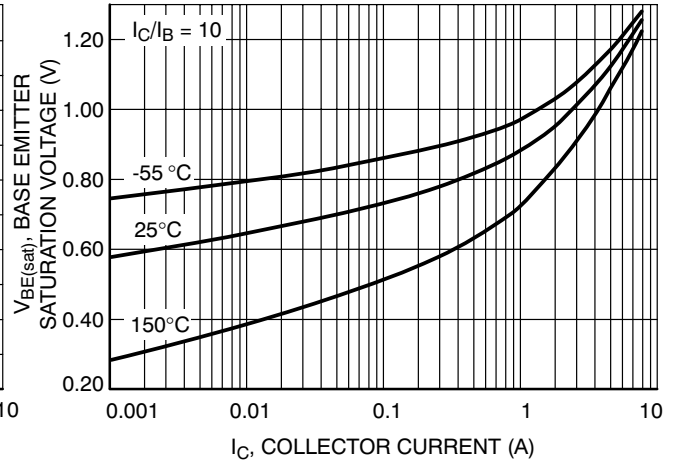
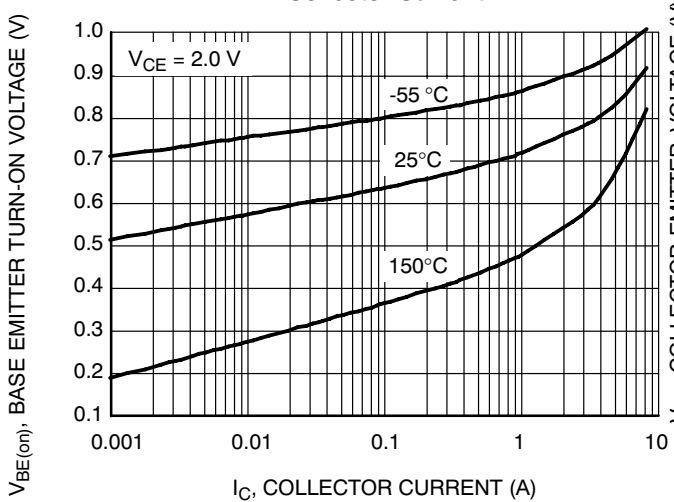**Figure 1. Collector Emitter Saturation Voltage vs. Collector Current**
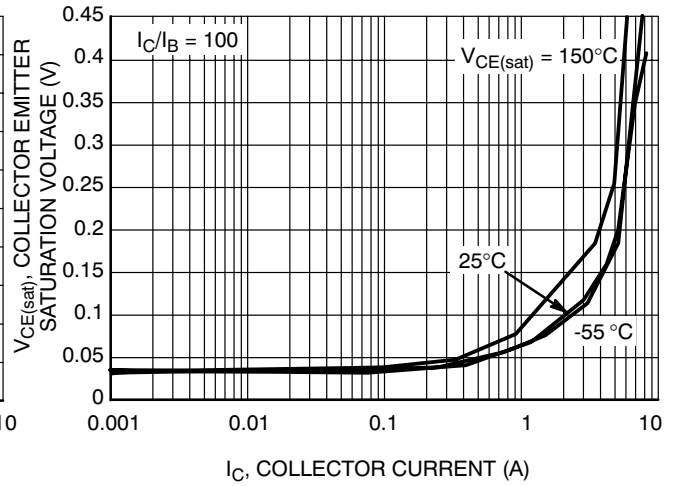
**Figure 2. Collector Emitter Saturation Voltage vs. Collector Current**
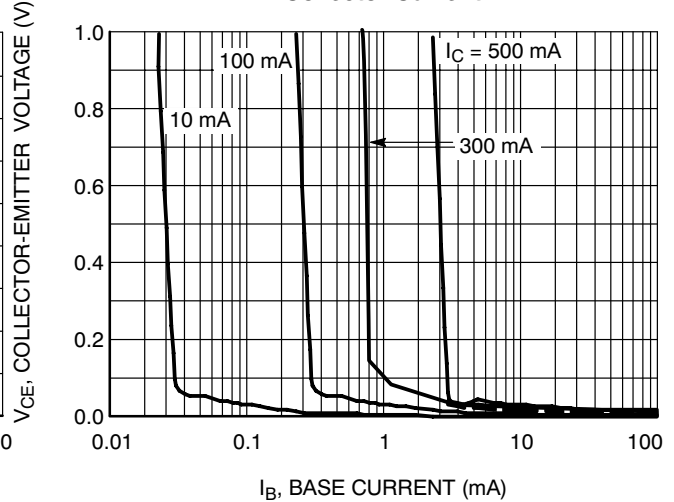
**Figure 3. DC Current Gain vs. Collector Current**

**Figure 4. Base Emitter Saturation Voltage vs. Collector Current**

**Figure 5. Base Emitter Turn-On Voltage vs. Collector Current**

**Figure 6. Saturation Region**

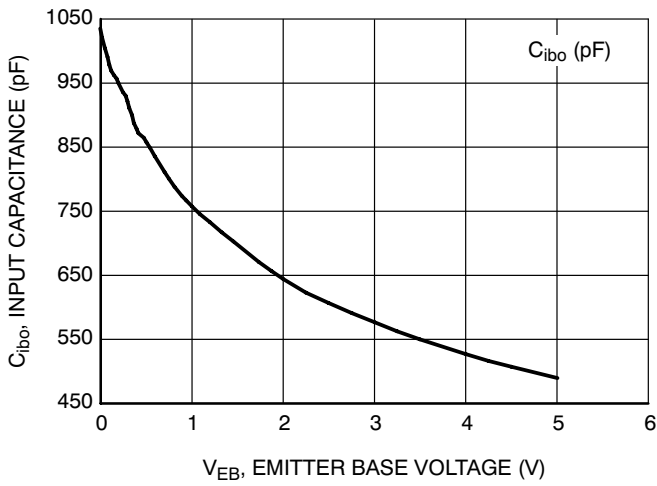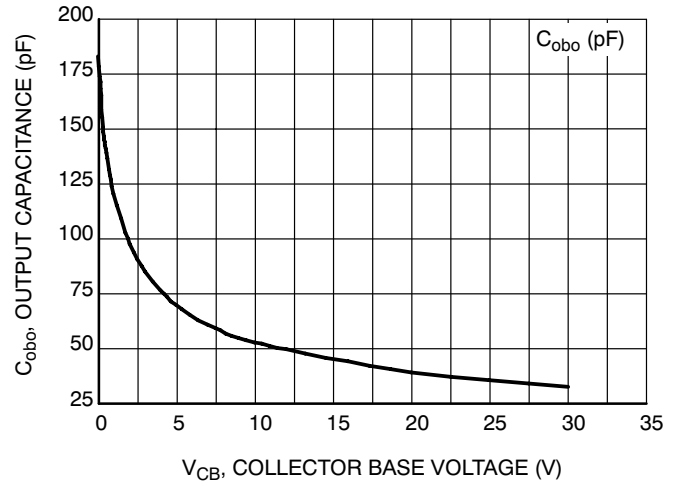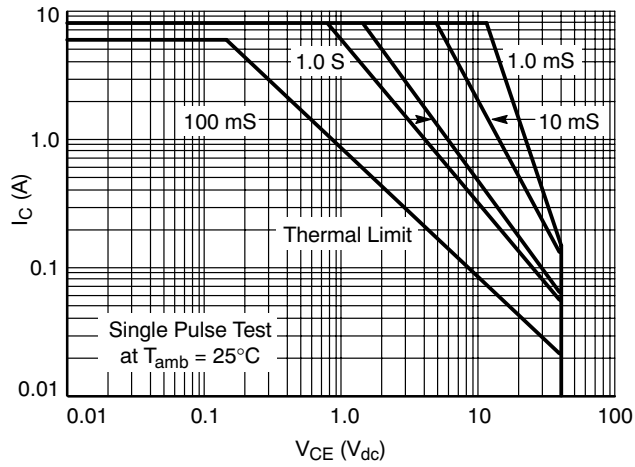**Figure 7. Input Capacitance**



**Figure 8. Output Capacitance**



**Figure 9. Safe Operating Area**

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**ChipFET™**
CASE1206A–03
ISSUE K

DATE 19 MAY 2009

**SCALE 1:1**

**RESET**
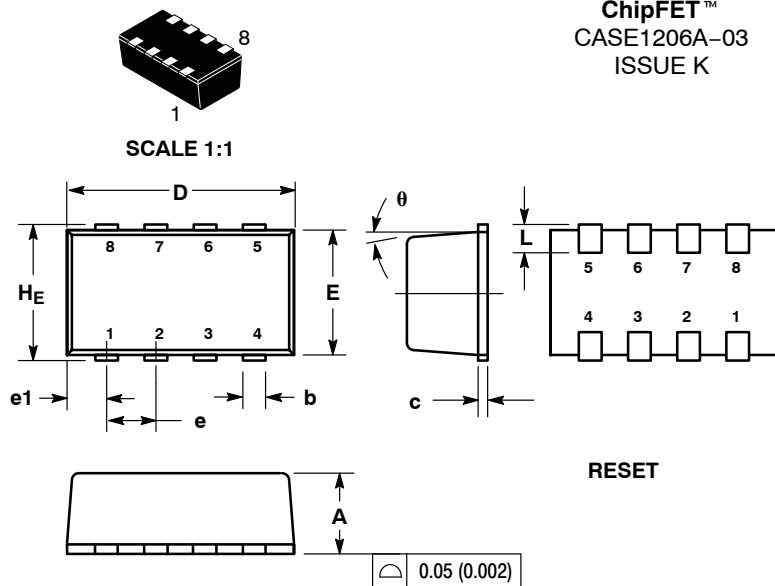
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-----|-----|-----|-----|-----|-----|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.00 | 1.05 | 1.10 | 0.039 | 0.041 | 0.043 |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 2.95 | 3.05 | 3.10 | 0.116 | 0.120 | 0.122 |
| E | 1.55 | 1.65 | 1.70 | 0.061 | 0.065 | 0.067 |
| e | 0.65 BSC | | | 0.025 BSC | | |
| e1 | 0.55 BSC | | | 0.022 BSC | | |
| L | 0.28 | 0.35 | 0.42 | 0.011 | 0.014 | 0.017 |
| $H_E$ | 1.80 | 1.90 | 2.00 | 0.071 | 0.075 | 0.079 |
| θ | 5° NOM | | | 5° NOM | | |

△ 0.05 (0.002)

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

## SOLDERING FOOTPRINT

2.032 / 0.08

2.362 / 0.093

0.65 / 0.025 PITCH

8X 0.457 / 0.018

8X 0.66 / 0.026

( mm / inches )

**Basic Style**

## GENERIC MARKING DIAGRAM*

xxx M▪
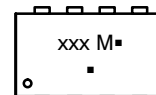
xxx = Specific Device Code
M = Month Code
▪ = Pb–Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪ ", may or may not be present.

## OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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|---|---|---|---|
| DESCRIPTION: | ChipFET | | PAGE 1 OF 2 |

ChipFET ™
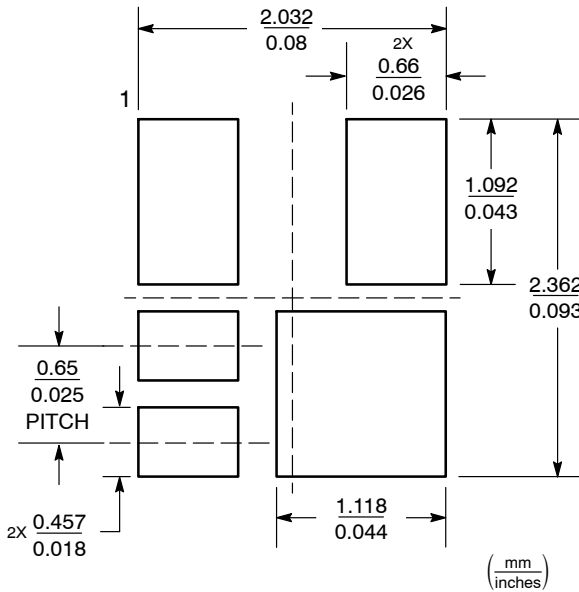CASE 1206A–03
ISSUE K

## ADDITIONAL SOLDERING FOOTPRINTS*



**Styles 1 and 4**
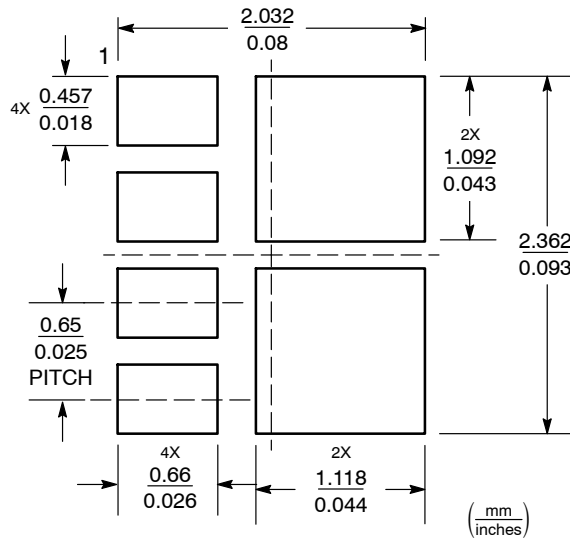


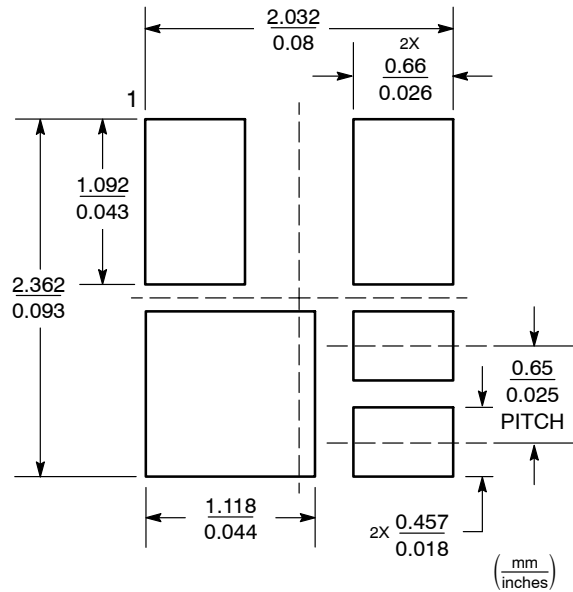**Style 2**



**Style 3**



**Style 5**

*For additional information on our Pb–Free strategy and soldering
details, please download the ON Semiconductor Soldering and
Mounting Techniques Reference Manual, SOLDERRM/D.

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## PUBLICATION ORDERING INFORMATION

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