NCP81241

Single-Phase Controller with SVID Interface for Desktop and Notebook CPU Applications

The NCP81241 Single−Phase buck solution is optimized for Intel® VR12.1 compatible CPUs. The controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed−forward, and adaptive voltage positioning to provide accurately regulated power for both Desktop and Notebook applications. The single phase controller uses DCR current sensing providing the fastest initial response to dynamic load events at reduced system cost.

The NCP81241 incorporates an internal MOSFET driver for improved system efficiency. High performance operational error amplifiers are provided to simplify compensation of the system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed−loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate digital current monitoring.

Features

- Meets Intel VR12.1 Specifications
- High Performance Operational Error Amplifier
- Digital Soft Start Ramp
- Dynamic Reference Injection
- “Lossless” DCR Current Sensing
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 250 kHz – 1.2 MHz
- VIN Range 4.5 V − 25 V
- Startup into Pre−Charged Load While Avoiding False OVP
- Vin Feed Forward Ramp Slope
- Pin Programming for Internal SVID parameters
- Over Voltage Protection (OVP) and Under Voltage Protection (UVP)
- Over Current Protection (OCP)
- VR−RDY Output with Internal Delays
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Desktop and Notebook Processors

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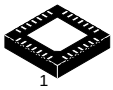


QFN28
CASE 485AR

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

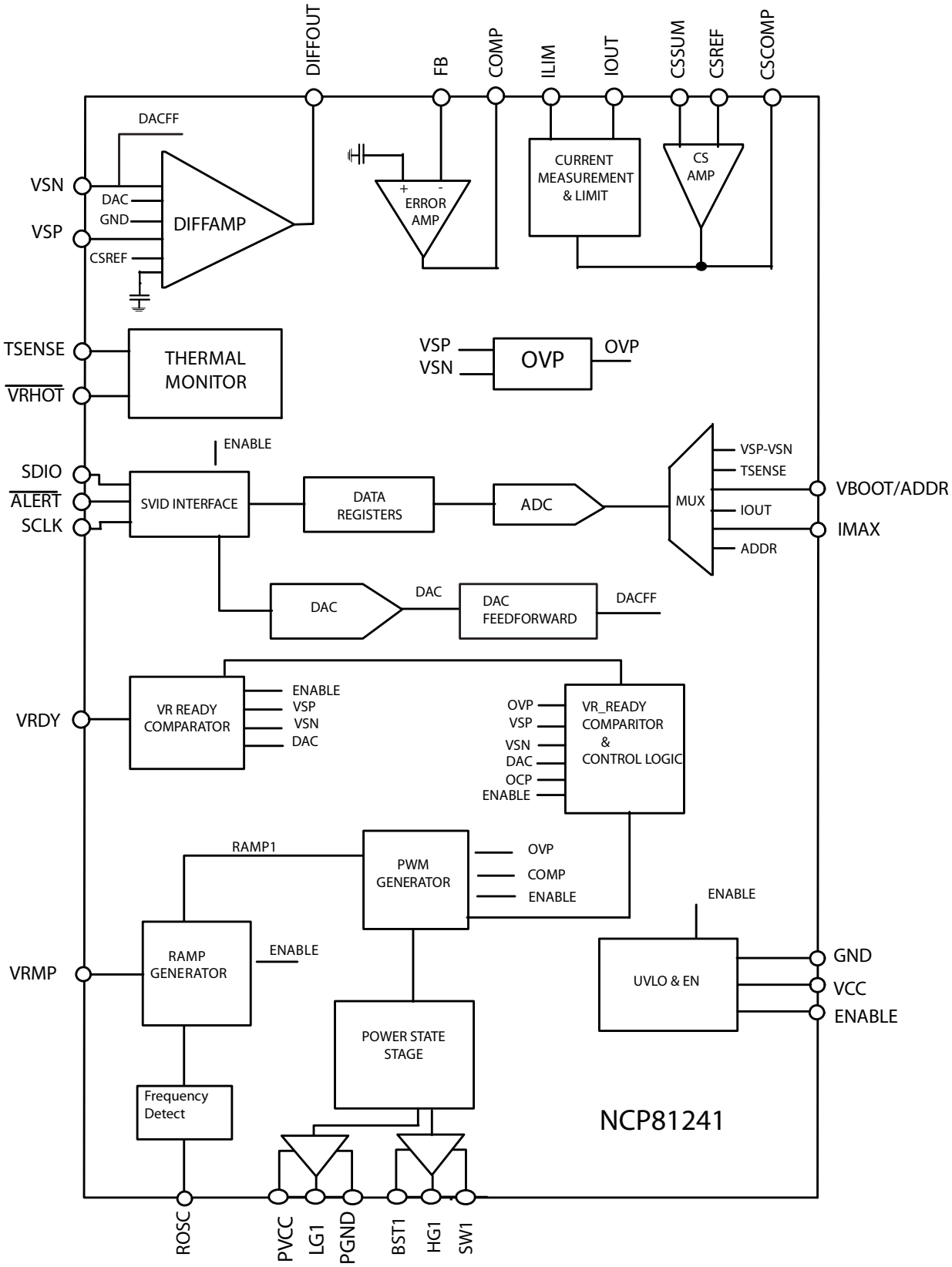


Figure 1. Block Diagram for NCP81241

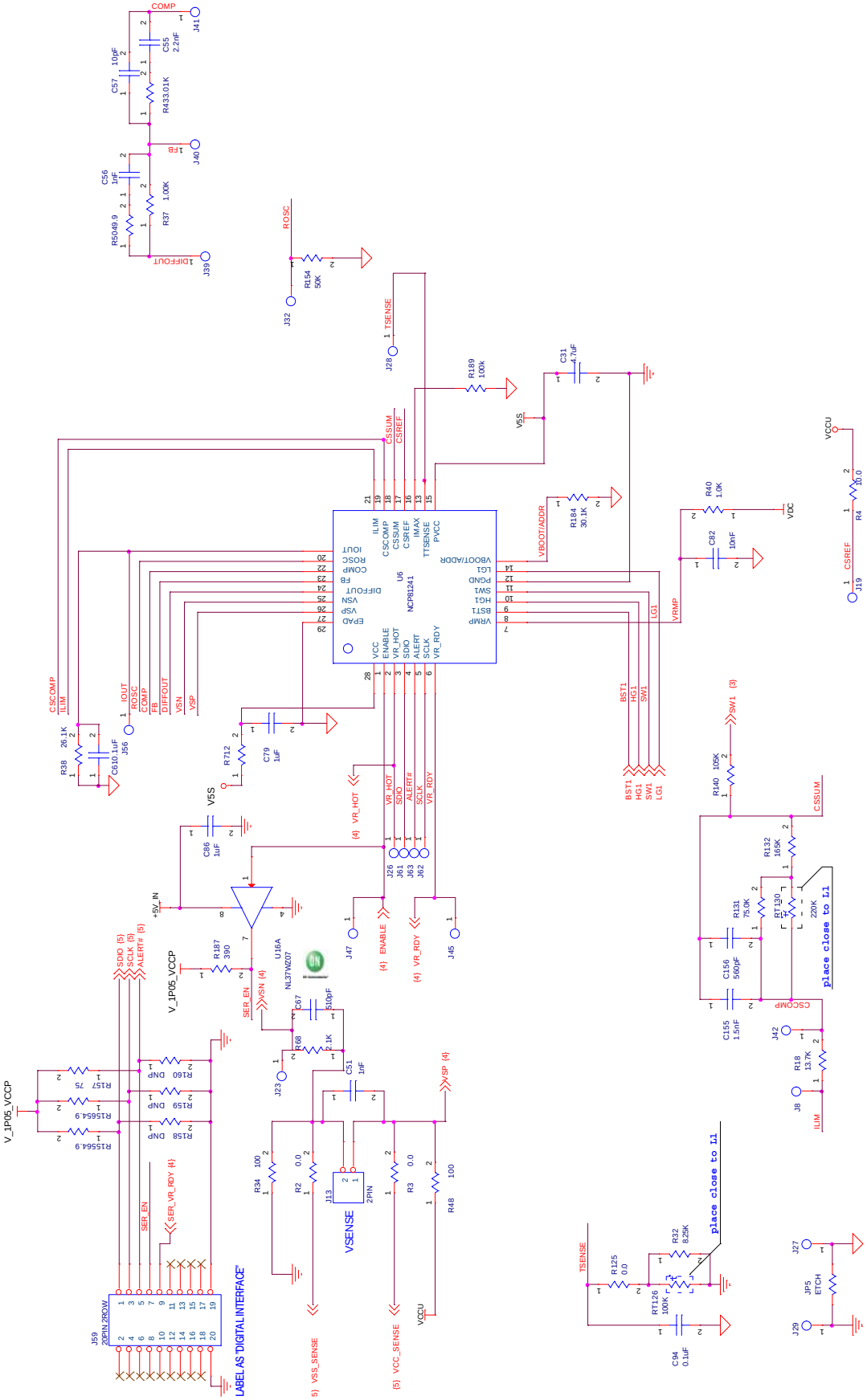


Figure 2. Controller Application Schematic

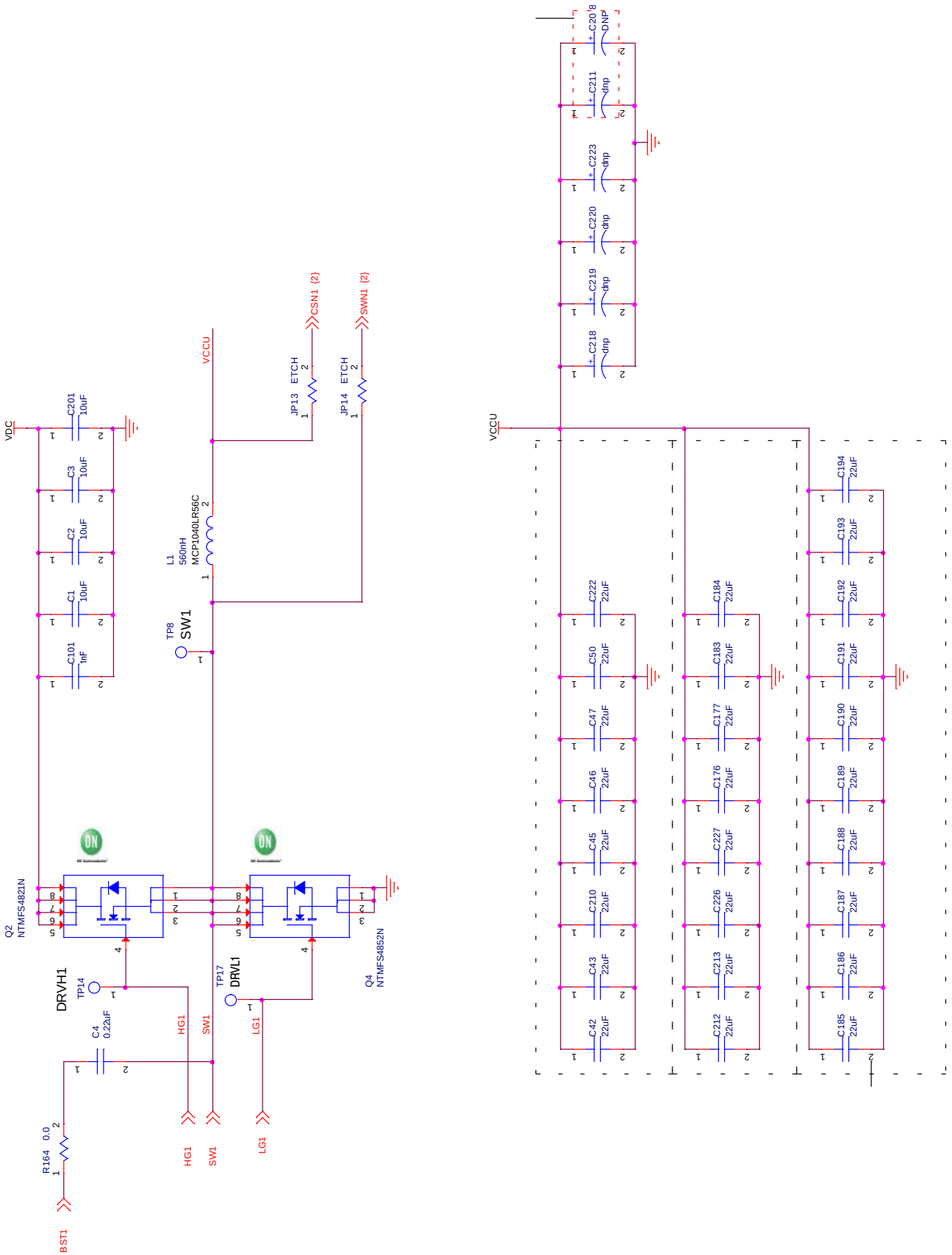


Figure 3. Power Stage Typical Schematic

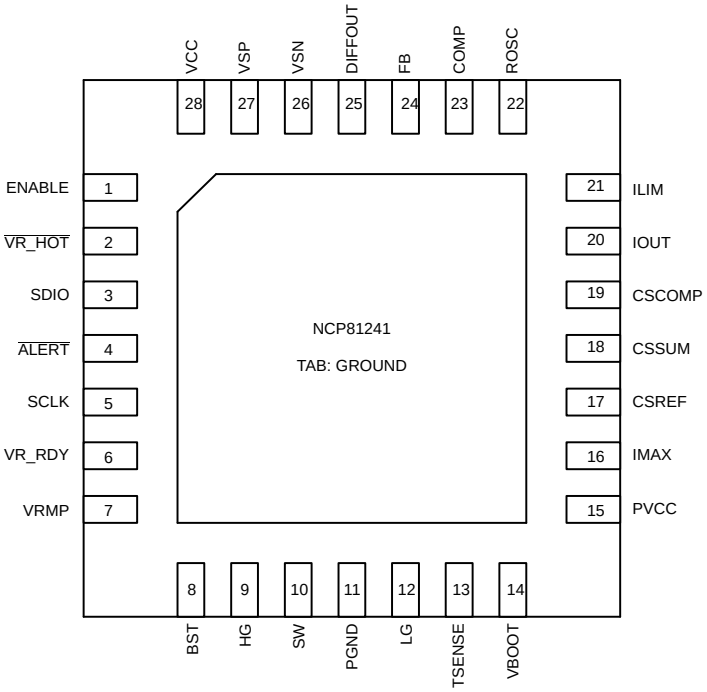


Figure 4. NCP81241 Pin Configurations

Table 1. NCP81241 SINGLE ROW PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	ENABLE	Logic input. Logic high enables both outputs and logic low disables both outputs
2	VR_HOT#	Thermal logic output for over temperature
3	SDIO	Serial VID data interface
4	ALERT#	Serial VID ALERT#.
5	SCLK	Serial VID clock
6	VR_RDY	Open drain output. High indicates that the output is regulating
7	VRMP	Feed−forward input of Vin for the ramp slope compensation. The current fed into this pin is used to control the ramp of PWM slope
8	BST	High−Side bootstrap supply for phase 1.
9	HG	High side gate driver output for phase 1
10	SW	Current return for high side gate driver 1
11	PGND	Power Ground for gate driver
12	LG	Low−Side gate driver output for phase 1
13	TSENSE	Temp Sense input for the single phase converter
14	VBOOT/ADDR	An input pin to adjust the boot−up voltage. During start up it is used to program VBOOT and SVID address with a resistor to ground
15	PVCC	Power Supply for gate driver, recommended decoupling 2.2uF
16	IMAX	Imax Input Pin. During start up it is used to program IMAX with a resistor to ground
17	CSREF	Total output current sense amplifier reference voltage input
18	CSSUM	Inverting input of total current sense amplifier
19	CSCOMP	Output of total current sense amplifier
20	IOUT	Total output current monitor.
21	ILIM	Over current shutdown threshold setting. Resistor to CSCOMP to set threshold

Table 1. NCP81241 SINGLE ROW PIN DESCRIPTIONS

22	ROSC	A resistance from this pin to ground programs the oscillator frequency
23	COMP	Output of the error amplifier and the inverting input of the PWM comparator
24	FB	Error amplifier voltage feedback
25	DIFFOUT	Output of the differential remote sense amplifier
26	VSN	Inverting input to differential remote sense amplifier
27	VSP	Non−inverting input to the differential remote sense amplifier
28	Vcc	Power for the internal control circuits. A 1uF decoupling capacitor is connected from this pin to ground
29	FLAG/GND	

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	V_{MAX}	V_{MIN}	Isource	Isink
COMP	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMP	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VSN	GND + 300 mV	GND – 300 mV	1 mA	1 mA
DIFFOUT	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VR_RDY	VCC + 0.3 V	−0.3 V	N/A	2 mA
VCC	6.5 V	−0.3 V	N/A	N/A
ROSC	VCC + 0.3 V	−0.3 V		
IOUT	2.0 V	−0.3 V		
VRMP	+25 V	−0.3 V		
SW	35 V 40 V ≤ 50 ns	−5 V −10 V ≤ 200 ns		
BST	35 V wrt/ GND 40 V ≤ 50 ns wrt/GND 6.5 V wrt/ SW	−0.3 V wrt/SW		
LG	VCC + 0.3 V	−0.3 V −5 V ≤ 200 ns		
HG	BST + 0.3 V	−0.3 V wrt/ SW −2 V ≤ 200 ns wrt/SW		
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*All signals referenced to GND unless noted otherwise.

Table 3. THERMAL INFORMATION

Thermal Characteristic QFN Package (Note 1)	$R_{\theta JA}$	68	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−40 to 125	°C
Operating Ambient Temperature Range	T_A	−40 to 100	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	
ESD Human Body Model	HBM	2000	V
ESD Machine Model	MM	200	V
ESD Charged Device Model	CDM	1000	V

*The maximum package power dissipation must be observed.
1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −40°C < T_A < 100°C; Vcc = 5 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
ERROR AMPLIFIER					
Input Bias Current	@ 1.3 V	−1.5		1.5	uA
Open Loop DC Gain	CL = 20 pF to GND, RL = 10 KΩ to GND		80		dB
Open Loop Unity Gain Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND		20		MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V, ΔVout = 1.5 V – 2.5 V, CL = 20 pF to GND, DC Load = 10 k to GND		25		V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.5	−	−	V
Minimum Output Voltage	I_{SINK} = 2.0 mA	−	−	1	V
DIFFERENTIAL VOLTAGE−SENSE AMPLIFIER					
Input Bias Current	VSP, CSREF = 1.3 V	−15	−	15	μA
VSP Input Voltage Range		−0.3	−	3.0	V
VSN Input Voltage Range		−0.3	−	0.3	V
−3 dB Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND		10		MHz
Closed Loop DC gain	VS+ to VS− = 0.5 to 1.3 V		1.0		V/V
DIFFERENTIAL CURRENT−SENSE AMPLIFIER					
Offset Voltage (Vos) (Note 3)		−300		300	μV
Input Bias Current	CSSUM = CSREF = 1.2 V	−10		+10	μA
Open Loop Gain			80		dB
Current Sense Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 KΩ to GND		10		MHz
INPUT SUPPLY					
Supply Voltage Range		4.75		5.25	V
VCC Quiescent Current Controller + Driver	EN = high, PS0, PS1,PS2	−	15	18	mA
	EN = high, PS3 Mode	−	8	10	mA
	EN = high, PS4 Mode (at 25°C)	−		200	μA
	EN = low	−	−	80	μA
UVLO Threshold	VCC rising	−		4.5	V
	VCC falling	4	4.08	−	V
VCC UVLO Hysteresis			275		mV
UVLO Threshold	VRMP Rising			4.05	V
	VRMP Falling	3.0			V
DAC SLEW RATE					
Soft Start Slew Rate			Fast_SR/4		mV/μs
Slew Rate Slow			Fast_SR/2 Fast_SR/4 (default) Fast_SR/8 Fast_SR/16		mV/μs
Slew Rate Fast			10		mV/μs

3. Guaranteed by design or characterization data, not in production test.

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −40°C < T_A < 100°C; Vcc = 5 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
ENABLE INPUT					
Enable High Input Leakage Current	External 1 K pull−up to 3.3 V	−		1.0	μA
Upper Threshold	V_{UPPER}	0.8			V
Lower Threshold	V_{LOWER}			0.3	V
Total Hysteresis	$V_{UPPER} - V_{LOWER}$		90		mV
IOUT OUTPUT					
Input Referred Offset Voltage	Ilimit to CSREF	−7.5		7.5	mV
Output Source Current				850	μA
Current Gain	($IOUT_{CURRENT}$) / ($ILIMIT_{CURRENT}$), R_{ILIM} = 20 k, R_{IOUT} = 5.0 k, DAC = 0.8 V, 1.25 V, 1.52 V	9.75	10	10.25	
OSCILLATOR					
Switching Frequency Range		250	−	1200	KHz
ZERO CURRENT DETECT (ZCD)					
ZCD threshold, DCM detection	SW wrt PGND		0		mV
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Absolute Over Voltage Threshold During Soft Start	CSREF	2.4	2.5	2.6	V
Over Voltage Threshold Above DAC	VSP rising	350	400	440	mV
Over Voltage Delay	VSP rising		50		ns
Under−voltage Delay	Ckt in development		5		μs
OVERCURRENT PROTECTION					
ILIM Threshold Current (OCP shutdown after 50 μs delay)	(PS0) Rlim = 20 k	9.0	10	11.0	μA
ILIM Threshold Current (immediate OCP shutdown)	(PS0) Rlim = 20 k	13.5	15	16.5	μA
ILIM Threshold Current (OCP shutdown after 50 μs delay)	(PS1, PS2, PS3) Rlim = 20 k		10		μA
ILIM Threshold Current (immediate OCP shutdown)	(PS1, PS2, PS3) Rlim = 20 k, PS0 mode		15		μA
VR_HOT#					
Output Low Voltage	$I_{\_VRHOT}$ = −4 mA			0.3	V
Output Leakage Current	High Impedance State	−1.0	−	1.0	μA
TSENSE					
Alert# Assert Threshold			508		mV
Alert# De−assert Threshold			490		mV
VRHOT Assert Threshold			488		mV
VRHOT Rising Threshold			470		mV
TSENSE Bias Current		115	120	127	μA
ADC					
Voltage Range		0		2	V
Total Unadjusted Error (TUE)		−1.25		1.25	%
Differential Nonlinearity (DNL)	8−bit, No missing codes			1	LSB

3. Guaranteed by design or characterization data, not in production test.

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −40°C < T_A < 100°C; Vcc = 5 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
ADC					
Power Supply Sensitivity			±1		%
Conversion Time			30		μs
Round Robin			90		μs
VR_RDY,(Power Good) OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = 4 mA	−	−	0.3	V
Rise Time	External pull−up of 1 KΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%	−	100		ns
Fall Time	External pull−up of 1 KΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 90% to 10%		10		ns
Output Voltage at Power−up	VR_RDY pulled up to 5 V via 2 KΩ	−	−	1.2	V
Output Leakage Current When High	VR_RDY= 5.0 V	−1.0	−	1.0	μA
VR_RDY Delay (rising)	DAC = TARGET to VR_RDY		8		μs
VR_RDY Delay (falling)	From OCP	−	5	−	μs
HIGH−SIDE MOSFET DRIVER					
Pull−up Resistance, Sourcing Current	BST = PVCC		1.2	2.8	Ω
High Side Driver Sourcing Current	BST = PVCC		4.17		A
Pull−down Resistance, Sinking Current	BST = PVCC		0.8	2.0	Ω
High Side Driver Sinking Current	BST = PVCC		6.25		A
HG Rise Time	VCC = 5 V, 3 nF load, BST − SW = 5 V	6	16	30	ns
HG Fall Time	VCC = 5 V, 3 nF load, BST − SW = 5 V	6	11	30	ns
DRVH Turn−Off Propagation Delay tpdhDRVH	CLOAD = 3 nF	7.0		30	ns
HG Turn on Propagation Delay $tpdl_{DRVH}$	CLOAD = 3 nF	7.0		30	ns
SW Pull−Down Resistance	SW to PGND		2		KΩ
HG Pull−Down Resistance	HG to SWBST−SW = 0 V		295		KΩ
LOW−SIDE MOSFET DRIVER					
Pull−up Resistance, Sourcing Current			0.9	2.8	Ω
Low Side Driver Sourcing Current			5.56		A
Pull−down Resistance, Sinking Current			0.8	2	Ω
Low Side Driver Sinking Current			12.5		A
LG Rise Time	3 nF load	6	16	30	ns
LG Fall Time	3 nF load	6	11	30	ns
LG Turn−On Propagation Delay tpdhDRVL	CLOAD = 3 nF		11	30	ns
PVCC Quiescent Current	EN = L (Shutdown) EN = H, no switching		1.0 490	10	μA
BOOTSTRAP RECTIFIER SWITCH					
On Resistance	EN=L or EN=H with DRVL=H	5	9	22	Ω

3. Guaranteed by design or characterization data, not in production test.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

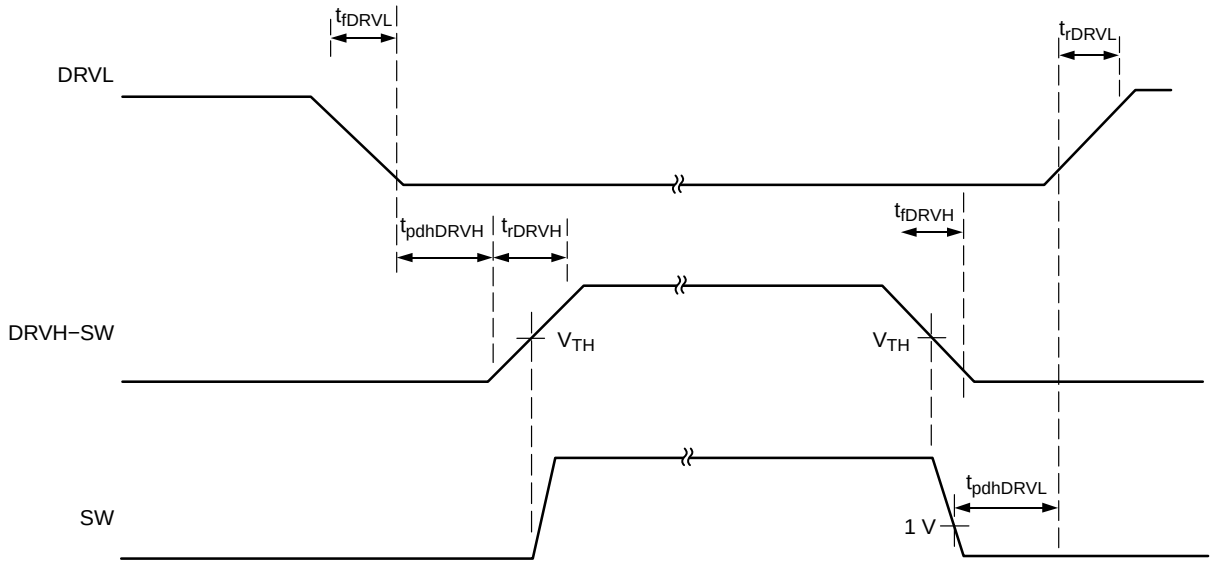


Figure 5. Driver Timing Diagram

NOTE: Timing is referenced to the 90% and the 10% points, unless otherwise stated.

Table 5. STATE TRUTH TABLE

STATE	VR_RDY Pin	Error AMP Comp Pin	OVP & UVP	Method of Reset
POR 0<VCC<UVLO	N/A	N/A	N/A	
Disabled EN < threshold UVLO >threshold	Low	Low	Disabled	
Start up Delay & Calibration EN> threshold UVLO>threshold	Low	Low	Disabled	
Soft Start EN > threshold UVLO >threshold	Low	Operational	Active / No latch	
Normal Operation EN > threshold UVLO >threshold	High	Operational	Active / Latching	N/A
Over Voltage	Low	N/A	DAC+OVP Limit	
Over Current	Low	Operational	Last DAC Code	
V_{OUT} = 0 V	Low: if Reg34h:bit0=0; High:if Reg34h:bit0=1;	Clamped at 0.9 V	Disabled	

General

The NCP81241 is a single phase PWM controller with integrated driver, designed to meet the Intel VR12.1 specifications with a serial SVID control interface.

The NCP81241 has one internal Driver: DRV1. Internally, there is a single PWM signal: PWM1. DRV1 is driven by PWM1.

SVID Address and Boot Voltage Programming

The NCP81241 has a Vboot voltage register that can be externally programmed. The boot voltage for the NCP81241 is set using VBOOT/ADDR pin on power up. A 10 uA current is sourced from the VBOOT/ADDR pin and the resulting voltage is measured. This is compared with the thresholds in the table below and the corresponding values for Vboot and SVID address are configured. These values are programmed on power up and cannot be changed after the initial power up sequence is complete.

For SVID Interface communication details please contact Intel Inc.

Table 6. SVID ADDRESS AND BOOT VOLTAGE TABLE

VBOOT/ADDR Resistor (Ohm)	SVID Address	Vboot (V)
0	0x0	1.0
14.0 k	0x1	1.0
22.1 k	0x2	1.0
30.1 k	0x3	1.0
39.2 k	0x4	1.0
48.7 k	0x5	1.0
57.6 k	0x6	1.0
68.1 k	0x7	1.0
78.7 k	0x8	1.1
88.7 k	0x0	1.1
100 k	0x1	1.1
113 k	0x2	1.1
124 k	0x3	1.1
137 k	0x4	1.1
150 k	0x5	1.1
165 k	0x6	1.1
182 k	0x7	1.1
196 k	0x8	1.1

Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3\ V - V_{DAC}) + (V_{CSCOMP} - V_{CSREF})$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non−inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

Remote Sense Amplifier

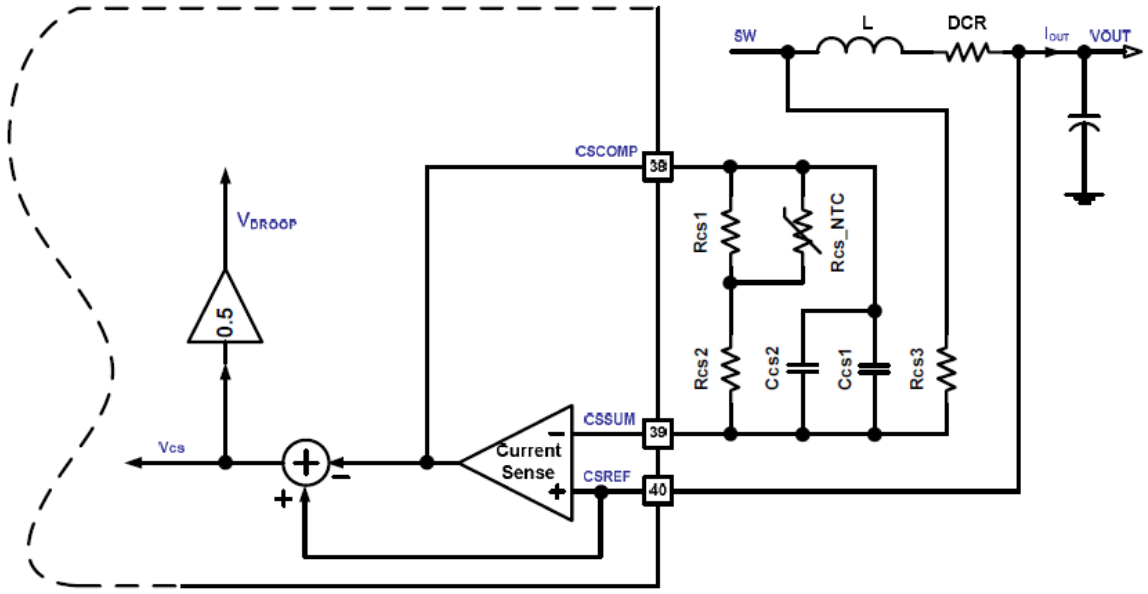
The differential current−sense circuit diagram is shown in the figure below. An internally−used voltage signal Vcs, representing the inductor current level, is the voltage difference between CSREF and CSCOMP. The output side of the inductor is used to create a low impedance virtual ground. The current−sense amplifier actively filters and gains up the voltage applied across the inductor to recover the voltage drop across the inductor's DC resistance(DCR). RCS_NTC is placed close to the inductor to sense the temperature. This allows the filter time constant and gain to be a function of the Rth_NTC resistor and compensate for the change in the DCR with temperature.

The DC gain in the current sensing loop is

GCS = VCS/VDCR = (VCSREF−VSCOMP) / (Iout * DCR) = RCS/RCS3

Where

RCS=RCS2+((RCS1*RCS_NTC)/(RCS1+RCS_NTC))

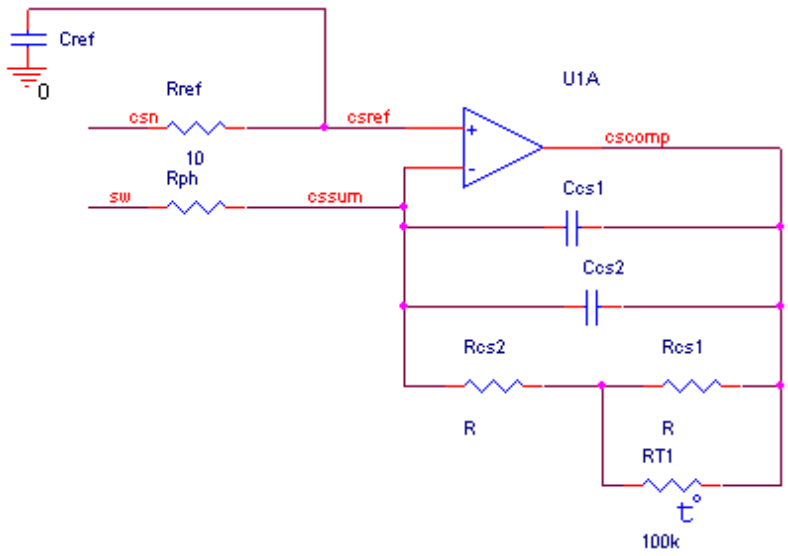


High Performance Voltage Error Amplifier

A high performance error amplifier is provided for high bandwidth transient performance. A standard type 3 compensation circuit is normally used to compensate the system.

Current Sense Amplifier

The outut current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The output side of the inductor is used to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductor to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near the inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.



The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = -\frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot \left(Iout_{Total} \cdot DCR\right)$$

Set the gain by adjusting the value of the Rph resistor. The DC gain should be set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100 mV at ICCMAX then it is recommend increasing the gain of the CSCOMP amp. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100 mV across the current limit programming resistor at full load. The values of Rcs1 and Rcs2 are set based on the 100 k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed close to the inductor.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. Ccs1 and Ccs2 are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_Z = \frac{DCR@25C}{2 \cdot PI \cdot L_{Phase}}$$

Programming Current Limit

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10 μA for 50 μs. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15 μA. Set the value of the current limit resistor based on the CSCOMP−CSREF voltage as shown below. To recover from an OCP fault the EN pin must be cycled low.

$$R_{LIMIT} = \frac{\left[2 \cdot \left(Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}\right) \cdot \left(Iout_{LIMIT} \cdot DCR\right)\right]}{Rph} \cdot \frac{}{10\ \mu}$$

or

$$R_{LIMIT} = \frac{\left(2 \cdot V_{CSCOMP-CSREF@ILIMIT}\right)}{10\ \mu}$$

Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.0\ V \cdot R_{LIMIT}}{10 \cdot \left(\frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot \left(Iout_{ICC\_MAX} \cdot DCR\right) \cdot 2\right)}$$

Programming ICC_MAX

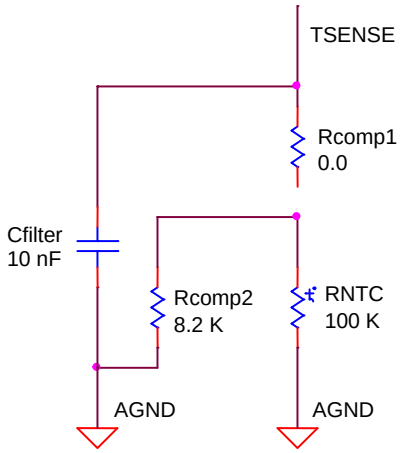
A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor.

$$ICC\_MAX_{21h} = \frac{R \cdot 10\ \mu A \cdot 64\ A}{2\ V}$$

Programming TSENSE

A temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense network. The

voltage on the temperature sense input is sampled by the internal A/D converter. A 100 k NTC similar to the VISHAY ERT−J1VS104JA should be used. Rcomp1 is mainly used for noise. See the specification table for the thermal sensing voltage thresholds and source current.



Precision Oscillator

Switching frequency is programmed by a resistor ROSC to ground at the ROSC pin. The typical frequency range is from 500 KHz to 1.2 MHz. The FREQ pin provides approximately 2 V out and the source current is mirrored into the internal ramp generator. The switching frequency can be found in figure below with a given ROSC. The frequency shown in the figure is under condition of 10 A output current at VID = 1 V.

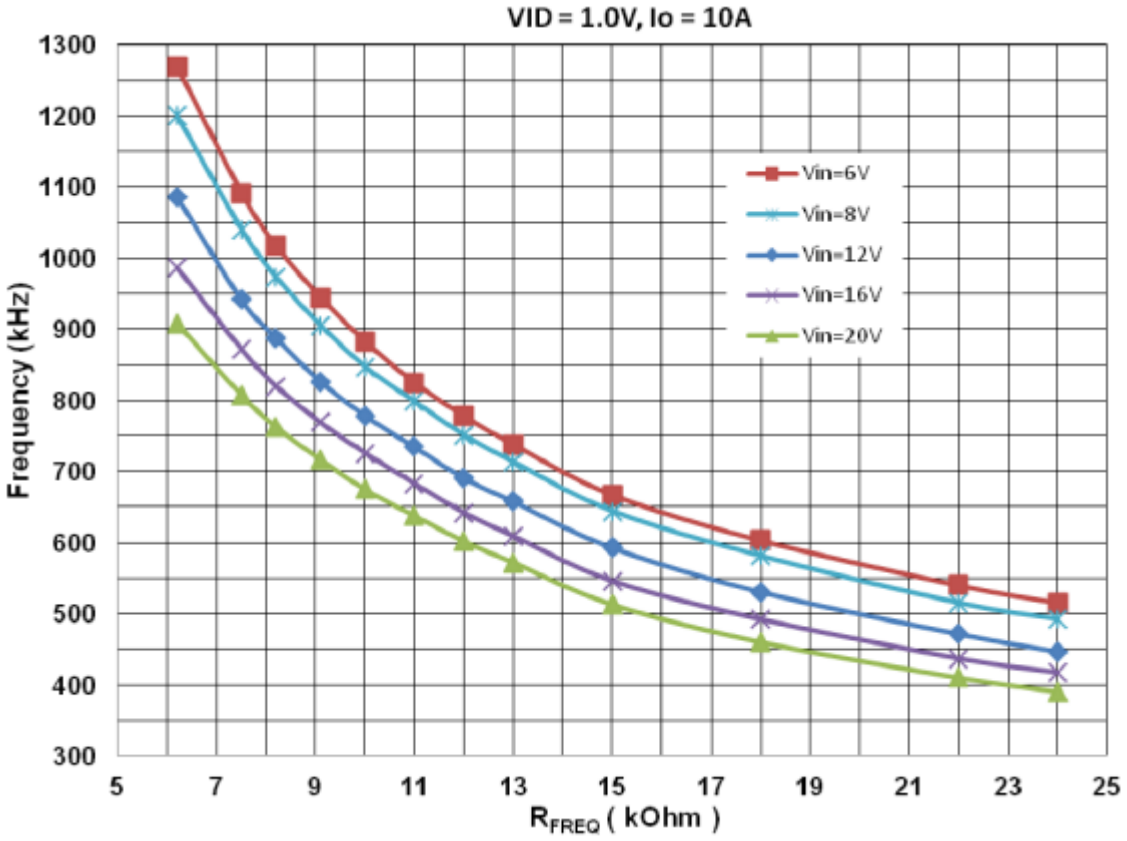


Figure 6. Switching Frequency vs. R_{FREQ}

The frequency has a variation over VID voltage and loading current this allows the NCP81241 to maintain similar output ripple voltage over different operation condition. The Figure below shws frequency variation over the VID voltage range.

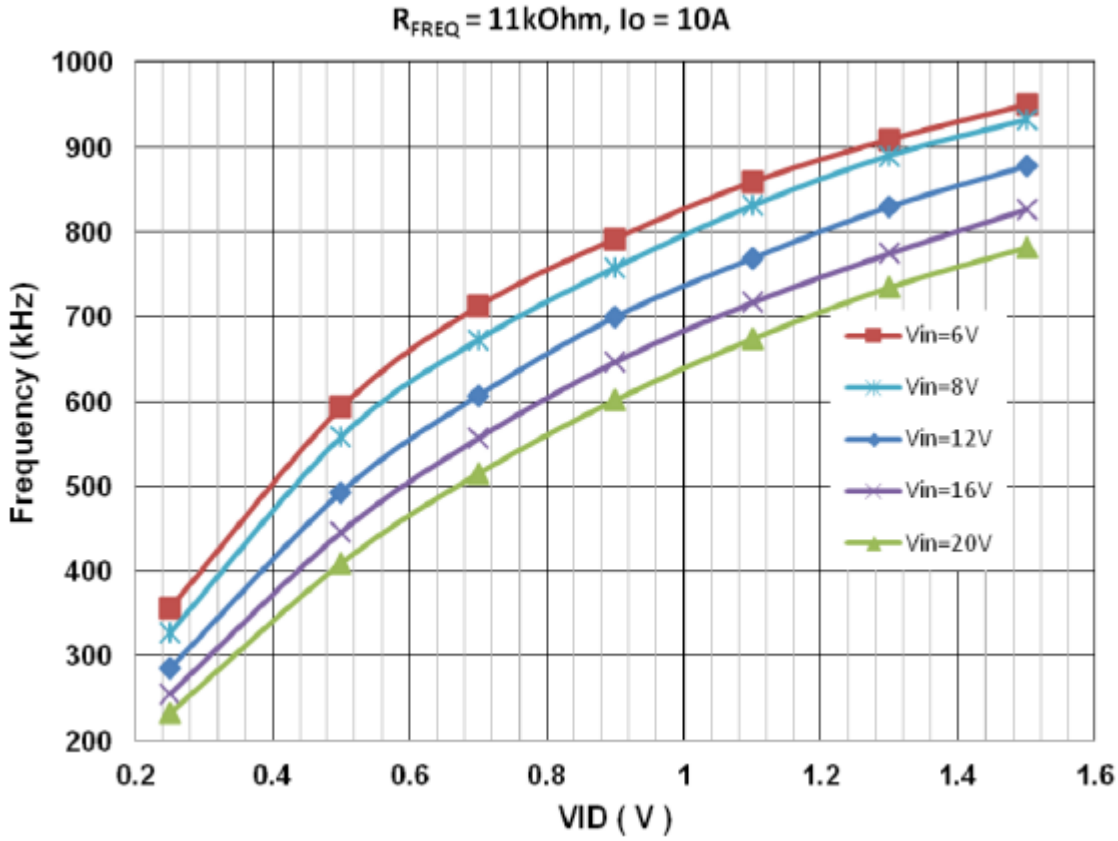


Figure 7. Switching Frequency vs. VID Voltage

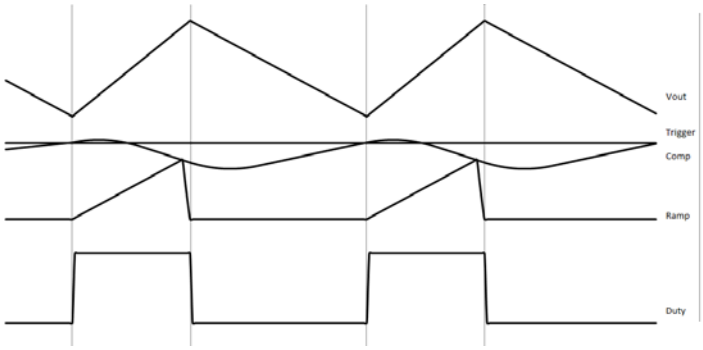
The oscillator generates a triangular ramp that is 0.5~2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation.

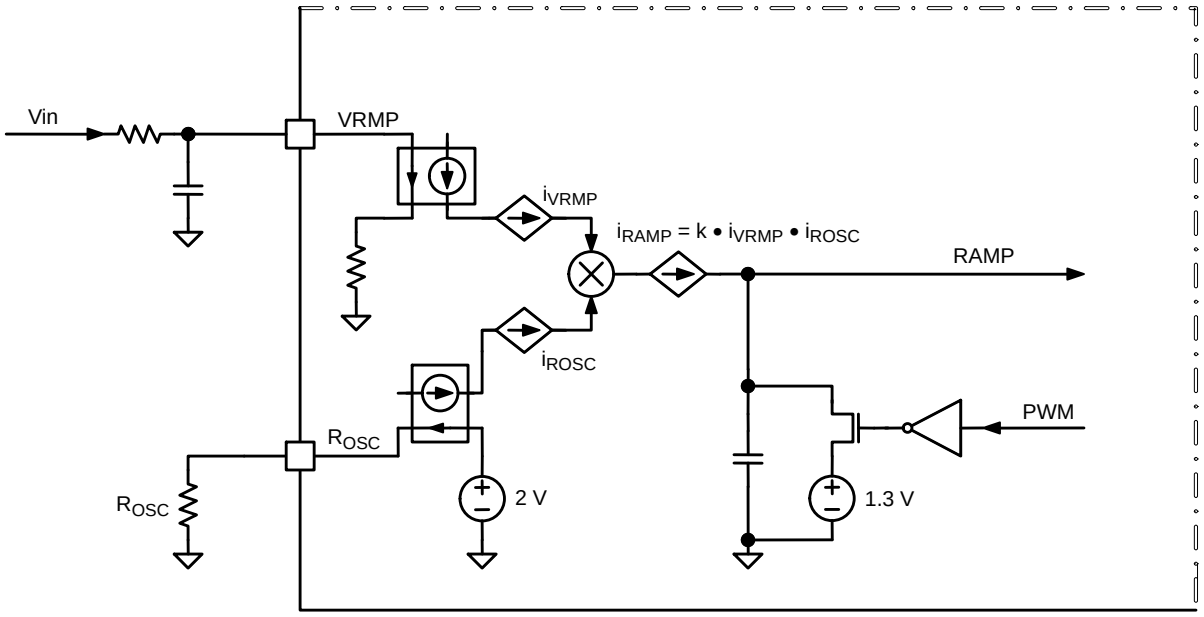
Programming the Ramp Feed−Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed−forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 3.2 V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

The PWM ramp time is changed according to the following,

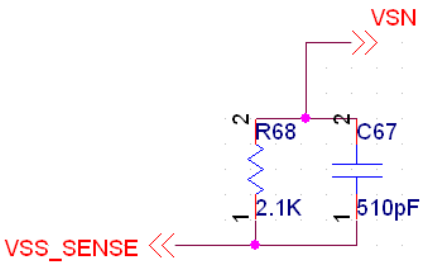
$$V_{RAMPpk=pk_{PP}} = 0.1 \cdot V_{VRMP}$$





Programming DAC Feed−Forward Filter

The DAC feed−forward implementation is realized by having a filter on the VSN pin. Programming Rvsn sets the gain of the DAC feed−forward and Cvsn provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance and Rout is the output impedance of the system.

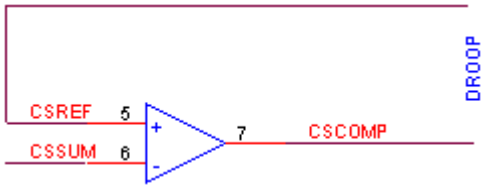


$$Rvsn = Cout \cdot Rout \cdot 453.6 \times 10^{6}$$

$$Cvsn = \frac{Rout \cdot Cout}{Rvsn}$$

Programming DROOP

The signals CSCOMP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage.



Droop = DCR * (R_{CS} / R_{ph})

Phase Comparator

The noninverting input of the comparator for phase one is connected to the output of the error amplifier (COMP) and the phase current (I_L*DCR*Phase Balance Gain Factor). The inverting input is connected to the oscillator ramp voltage with a 1.3 V offset. The operating input voltage range of the comparator is from 0 V to 3.0 V and the output of the comparator generates the PWM signal which is applied to the input of the internal driver.

During steady state operation, the duty cycle is centered on the valley of the sawtooth ramp waveform. The steady state duty cycle is still calculated by approximately Vout/Vin.

Protection Features

Undervoltage Lockout

There are several under voltage monitors in the system. Hysteresis is incorporated within the comparators. NCP81241 monitors the VCC Shunt supply. The gate driver monitors both the gate driver VCC and the BST voltage.

Soft Start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined rate in the spec table.

Over Current Latch−Off Protection

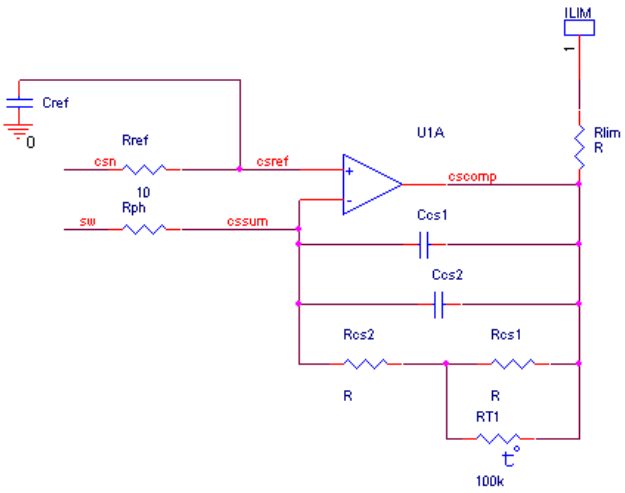
The NCP81241 compares a programmable current−limit set point to the voltage from the output of the current−summing amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current limit current I_{CL}. If

the current generated through this resistor into the ILIM pin (Ilim) exceeds the internal current−limit threshold current (I_{CL}), an internal latch−off counter starts, and the controller shuts down if the fault is not removed after 50 μs (shut down immediately for 150% load current) after which the outputs will remain disabled until the Vcc voltage or EN is toggled.

The voltage swing seen on CSCOMP cannot go below ground. This limits the voltage drop across the DCR. The over−current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equation:

$$R_{ILIM} = \frac{\left(I_{LIM} \cdot DCR \cdot R_{CS}/R_{PH}\right) \cdot 2}{I_{CL}}$$

Where I_{CL} =10 μA



Under Voltage Monitor

The output voltage is monitored at the output of the differential amplifier for UVLO. If the output falls more than 300 mV below the DAC−DROOP voltage the UVLO comparator will trip sending the VR_RDY signal low. The 300 mV limit can be reprogrammed using the VR_Ready_Low Limit register

Over Voltage Protection

The output voltage is also monitored at the output of the differential amplifier for OVP. During normal operation, if the output voltage exceeds the DAC voltage by 400 mV, the VR_RDY flag goes low, and the DAC will be ramped down slowly. At the same time, the high side gate driver is turned off and the low side gate driver is turned on until the voltage falls to 100 mV. The part will stay in this mode until the Vcc voltage or EN is toggled. During start up, the OVP threshold is set to 2.5 V. This allows the controller to start up without false triggering the OVP.

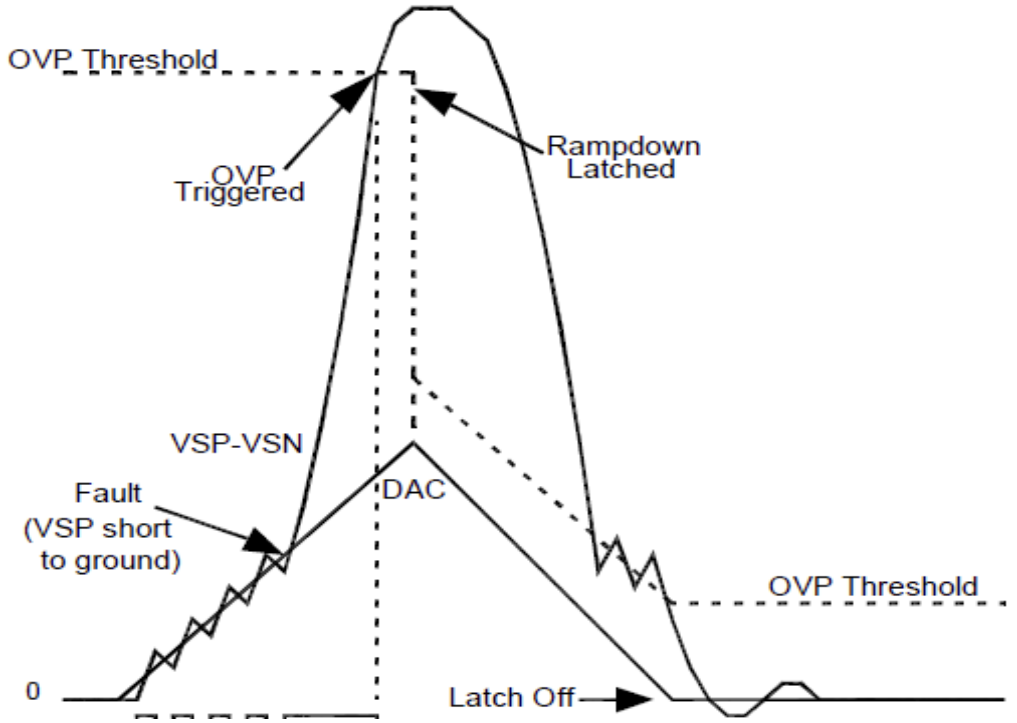


Figure 8. OVP Behavior at Startup

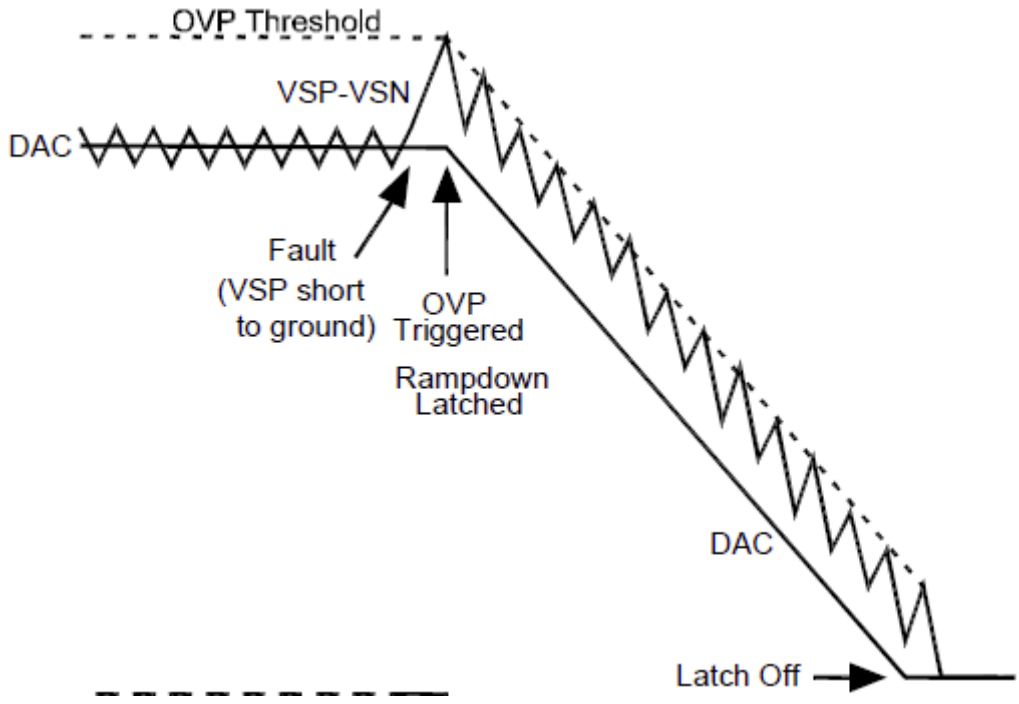


Figure 9. OVP During Normal Operation Mode

ORDERING INFORMATION

Device	Package	Shipping†
NCP81241MNTXG	QFN28 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

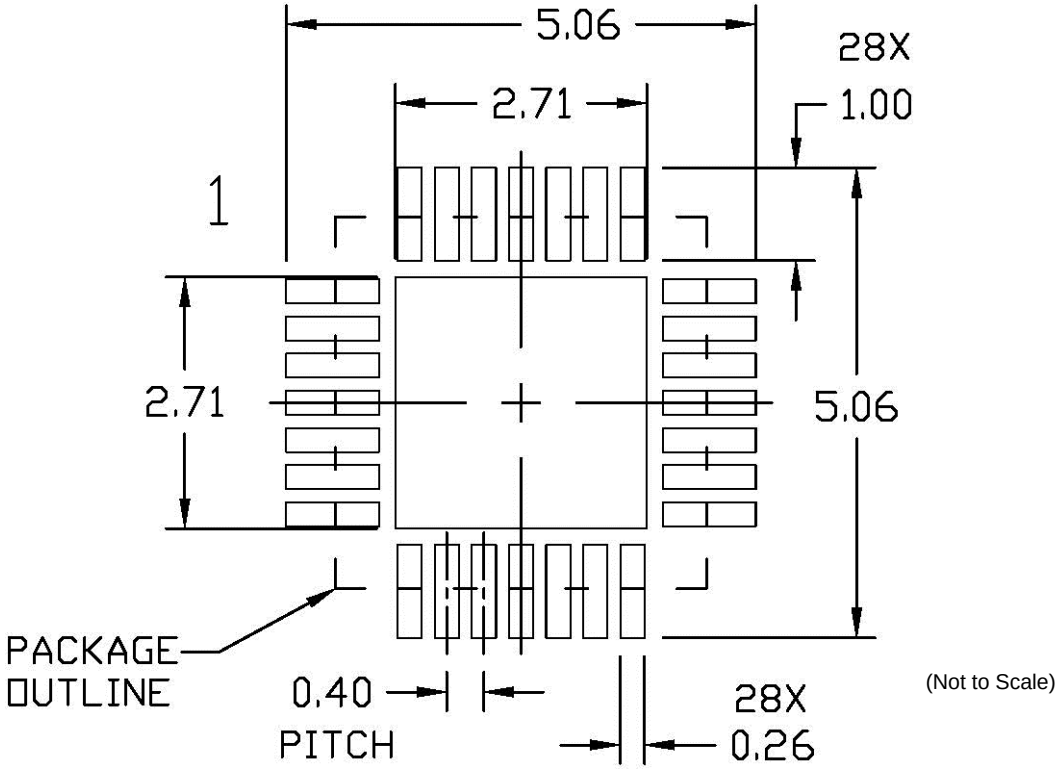
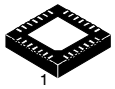


Figure 10. Alternative Extended Soldering Footprint

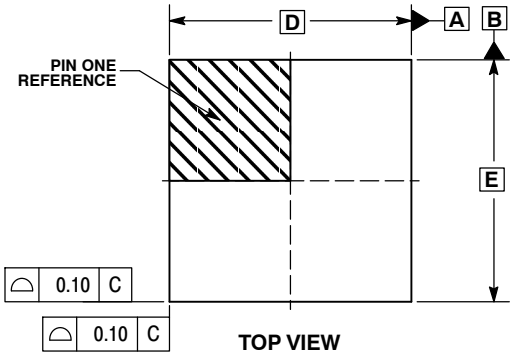
ON Semiconductor claims no responsibility for damage or usage beyond that of specific recommended soldering footprint

QFN28 4x4, 0.4P
CASE 485AR−01
ISSUE A

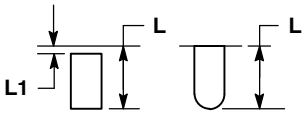
DATE 20 NOV 2009



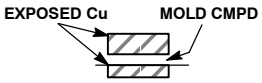
SCALE 2:1



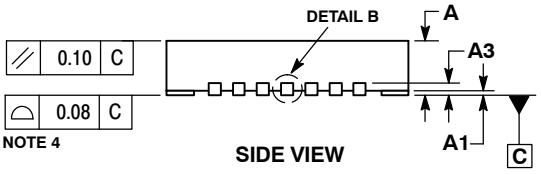
TOP VIEW



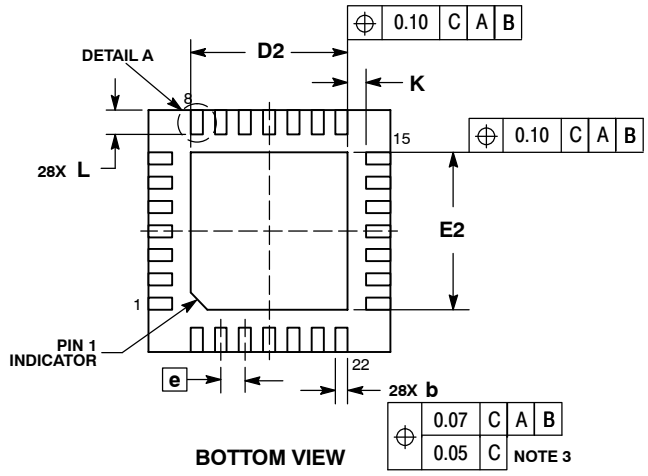
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW

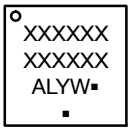


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	4.00 BSC	
D2	2.50	2.70
E	4.00 BSC	
E2	2.50	2.70
e	0.40 BSC	
K	0.30 REF	
L	0.30	0.50
L1	−−−	0.15

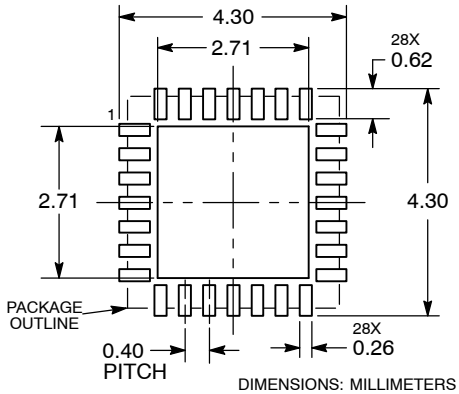
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY M. LIN.	15 MAY 2008
A	CHANGED DIMENSIONS D2, E2, K, L, MOUNTING FOOTPRINT AND MARKING DIAGRAM INFORMATION. REQ. BY J. LIU.	20 NOV 2009

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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