# Hex Buffer

# MC14049B, MC14050B

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P−Channel and N−Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage, $V_{DD}$.

The input−signal high level ($V_{IH}$) can exceed the $V_{DD}$ supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS−to−TTL/DTL converter ($V_{DD}$ = 5.0 V, $V_{OL} \le$ 0.4 V, $I_{OL} \ge$ 3.2 mA).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

### Features

- High Source and Sink Currents
- High−to−Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- $V_{IN}$ can exceed $V_{DD}$
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$)

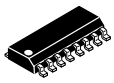
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$ | Input Voltage Range (DC or Transient) | −0.5 to +18.0 | V |
| $V_{out}$ | Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$ | Input Current (DC or Transient) per Pin | ±10 | mA |
| $I_{out}$ | Output Current (DC or Transient) per Pin | ±45 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1)<br>(Plastic)<br>(SOIC) | <br>825<br>740 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8−Second Soldering) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: See Figure 3.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the $V_{SS}$ pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high−impedance circuit. For proper operation, the ranges $V_{SS} \le V_{in} \le$ 18 V and $V_{SS} \le V_{out} \le V_{DD}$ are recommended.

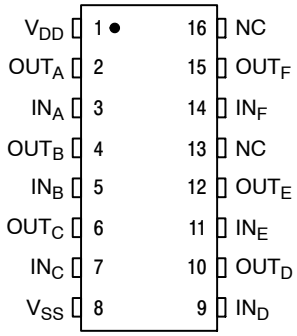
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.



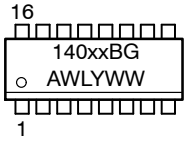
SOIC−16
D SUFFIX
CASE 751B

TSSOP−16
DT SUFFIX
CASE 948F

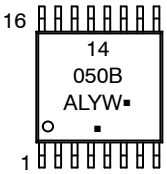
### PIN ASSIGNMENT




### MARKING DIAGRAMS




SOIC−16




TSSOP−16

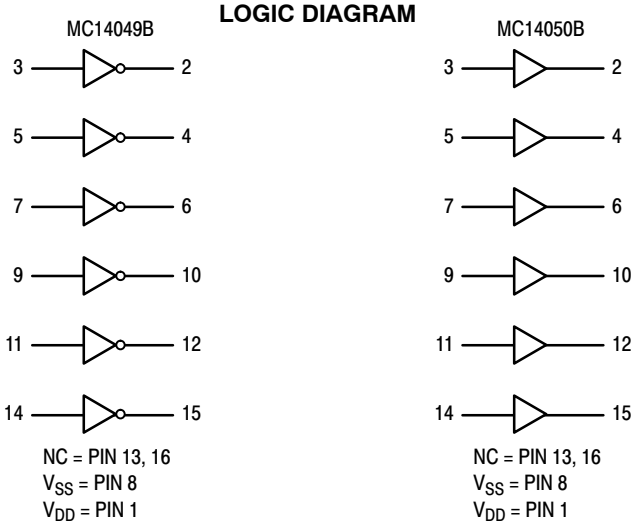
| | |
|---|---|
| xx | = Specific Device Code |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Indicator |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## LOGIC DIAGRAM




## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC14049BDG | SOIC−16<br>(Pb−Free) | 48 Units / Rail |
| MC14049BDR2G | SOIC−16<br>(Pb−Free) | 2500 Units / Tape & Reel |
| NLV14049BDR2G* | SOIC−16<br>(Pb−Free) | 2500 Units / Tape & Reel |
| MC14050BDG | SOIC−16<br>(Pb−Free) | 48 Units / Rail |
| MC14050BDR2G | SOIC−16<br>(Pb−Free) | 2500 Units / Tape & Reel |
| NLV14050BDR2G* | SOIC−16<br>(Pb−Free) | 2500 Units / Tape & Reel |
| MC14050BDTR2G | TSSOP−16<br>(Pb−Free) | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | –55°C Min | –55°C Max | +25°C Min | +25°C Typ (Note 2) | +25°C Max | +125°C Min | +125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level | $V_{OL}$ | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| $V_{in} = V_{DD}$ | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| “1” Level | $V_{OH}$ | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| $V_{in} = 0$ | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | |
| | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | |
| Input Voltage “0” Level | $V_{IL}$ | | | | | | | | | Vdc |
| ($V_O$ = 4.5 Vdc) | | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | |
| ($V_O$ = 9.0 Vdc) | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | |
| ($V_O$ = 13.5 Vdc) | | 15 | – | 4.0 | – | 6.75 | 4.0 | – | 4.0 | |
| “1” Level | $V_{IH}$ | | | | | | | | | Vdc |
| ($V_O$ = 0.5 Vdc) | | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | |
| ($V_O$ = 1.0 Vdc) | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | |
| ($V_O$ = 1.5 Vdc) | | 15 | 11 | – | 11 | 8.25 | – | 11 | – | |
| Output Drive Current | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | –1.6 | – | –1.25 | –2.5 | – | –1.0 | – | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | –1.6 | – | –1.30 | –2.6 | – | –1.0 | – | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | –4.7 | – | –3.75 | –10 | – | –3.0 | – | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 3.75 | – | 3.2 | 6.0 | – | 2.6 | – | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 10 | – | 8.0 | 16 | – | 6.6 | – | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 30 | – | 24 | 40 | – | 19 | – | |
| Input Current | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±1.0 | μAdc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | – | – | – | – | 10 | 20 | – | – | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | – | 1.0 | – | 0.002 | 1.0 | – | 30 | μAdc |
| | | 10 | – | 2.0 | – | 0.004 | 2.0 | – | 60 | |
| | | 15 | – | 4.0 | – | 0.006 | 4.0 | – | 120 | |
| Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, per package) ($C_L$ = 50 pF on all outputs, all buffers switching | $I_T$ | 5.0 | $I_T = (1.8\ \mu A/kHz)\ f + I_{DD}$ | | | | | | | μAdc |
| | | 10 | $I_T = (3.5\ \mu A/kHz)\ f + I_{DD}$ | | | | | | | |
| | | 15 | $I_T = (5.3\ \mu A/kHz)\ f + I_{DD}$ | | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at +25°C
4. To calculate total supply current at loads other than 50 pF:

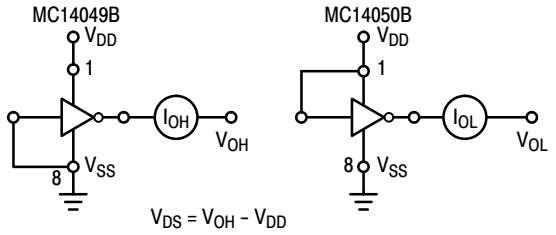
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

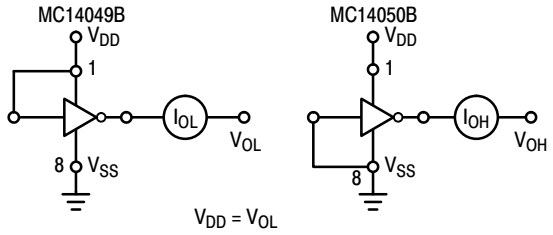
Where: $I_T$ is in μA (per Package), $C_L$ in pF, V = ($V_{DD}$ – $V_{SS}$) in volts, f in kHz is input frequency and k = 0.002.

**AC SWITCHING CHARACTERISTICS** (Note 5) ($C_L$ = 50 pF, $T_A$ = + 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | | | | | ns |
| $t_{TLH}$ = (0.7 ns/pF) $C_L$ + 65 ns | | 5.0 | – | 100 | 160 | |
| $t_{TLH}$ = (0.25 ns/pF) $C_L$ + 37.5 ns | | 10 | – | 50 | 80 | |
| $t_{TLH}$ = (0.2 ns/pF) $C_L$ + 30 ns | | 15 | – | 40 | 60 | |
| Output Fall Time | $t_{THL}$ | | | | | ns |
| $t_{THL}$ = (0.2 ns/pF) $C_L$ + 30 ns | | 5.0 | – | 40 | 60 | |
| $t_{THL}$ = (0.06 ns/pF) $C_L$ + 17 ns | | 10 | – | 20 | 40 | |
| $t_{THL}$ = (0.04 ns/pF) $C_L$ + 13 ns | | 15 | – | 15 | 30 | |
| Propagation Delay Time | $t_{PLH}$ | | | | | ns |
| $t_{PLH}$ = (0.33 ns/pF) $C_L$ + 63.5 ns | | 5.0 | – | 80 | 140 | |
| $t_{PLH}$ = (0.19 ns/pF) $C_L$ + 30.5 ns | | 10 | – | 40 | 80 | |
| $t_{PLH}$ = (0.06 ns/pF) $C_L$ + 27 ns | | 15 | – | 30 | 60 | |
| Propagation Delay Time | $t_{PHL}$ | | | | | ns |
| $t_{PHL}$ = (0.2 ns/pF) $C_L$ + 30 ns | | 5.0 | – | 40 | 80 | |
| $t_{PHL}$ = (0.1 ns/pF) $C_L$ + 15 ns | | 10 | – | 20 | 40 | |
| $t_{PHL}$ = (0.05 ns/pF) $C_L$ + 12.5 ns | | 15 | – | 15 | 30 | |

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



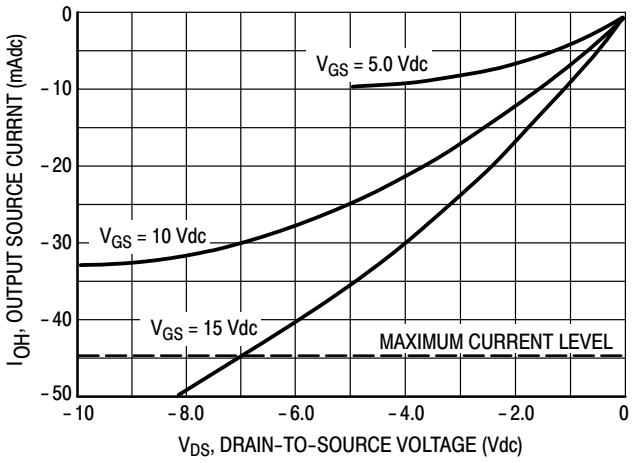




**Figure 1. Typical Output Source Characteristics**

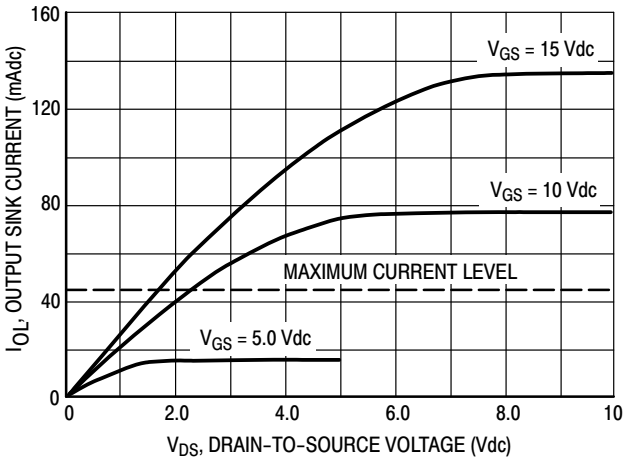



**Figure 2. Typical Output Sink Characteristics**

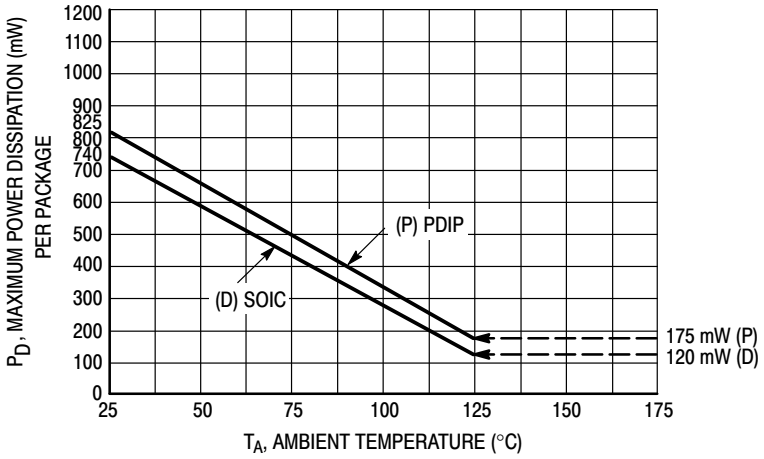



**Figure 3. Ambient Temperature Power Derating**

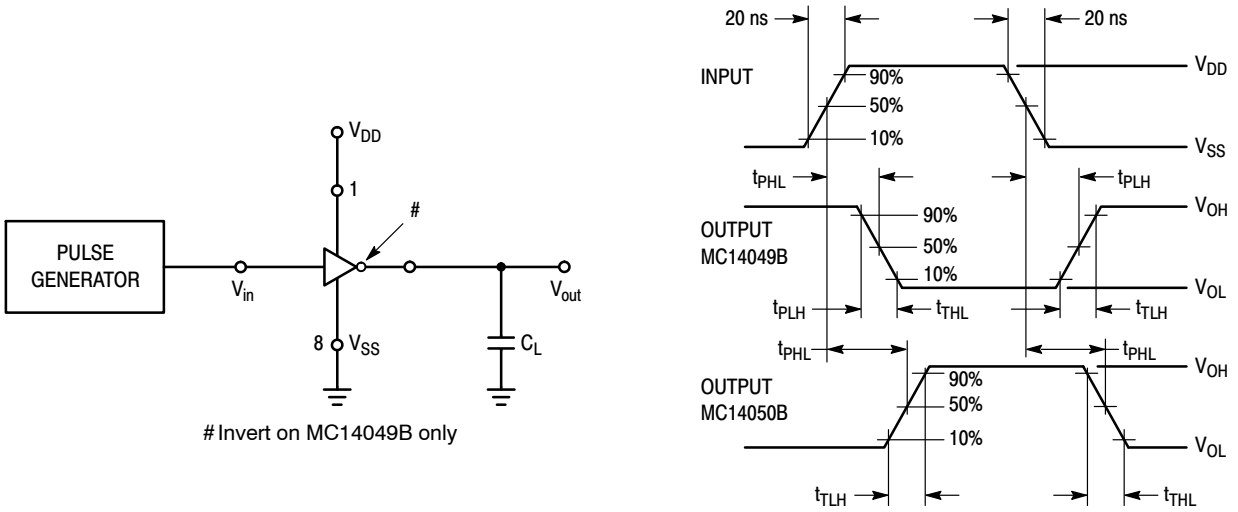
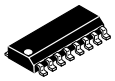


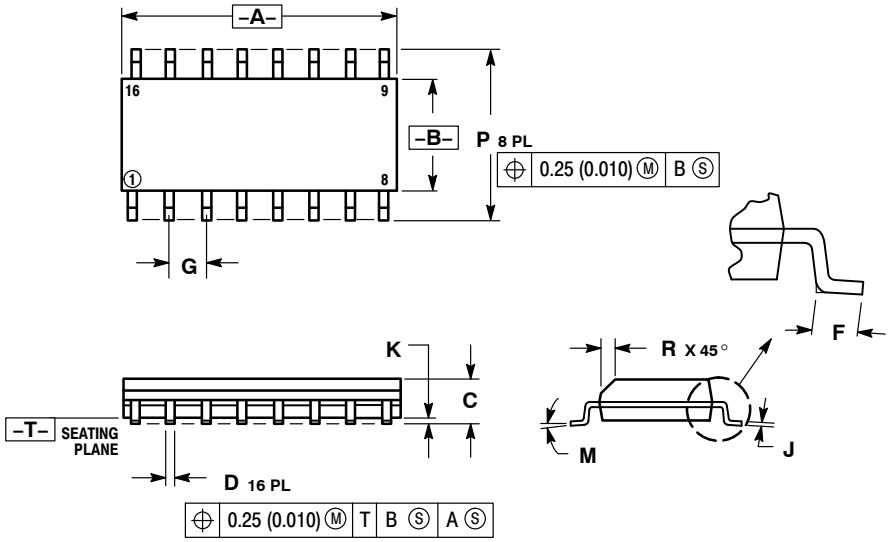

**Figure 4. Switching Time Test Circuit and Waveforms**



SCALE 1:1

**SOIC–16**
CASE 751B–05
ISSUE K

DATE 29 DEC 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

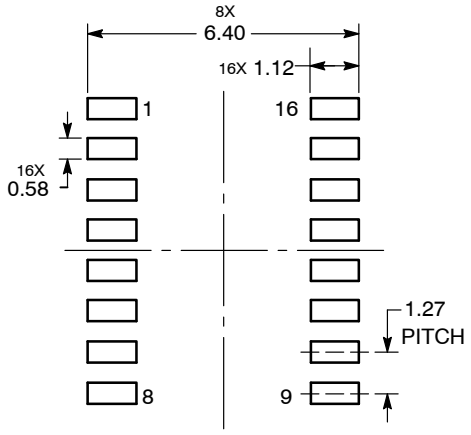
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

**SOLDERING FOOTPRINT**

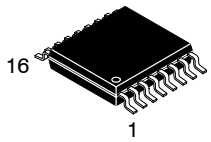



DIMENSIONS: MILLIMETERS

| DOCUMENT NUMBER: | 98ASB42566B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | SOIC–16 | PAGE 1 OF 1 |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

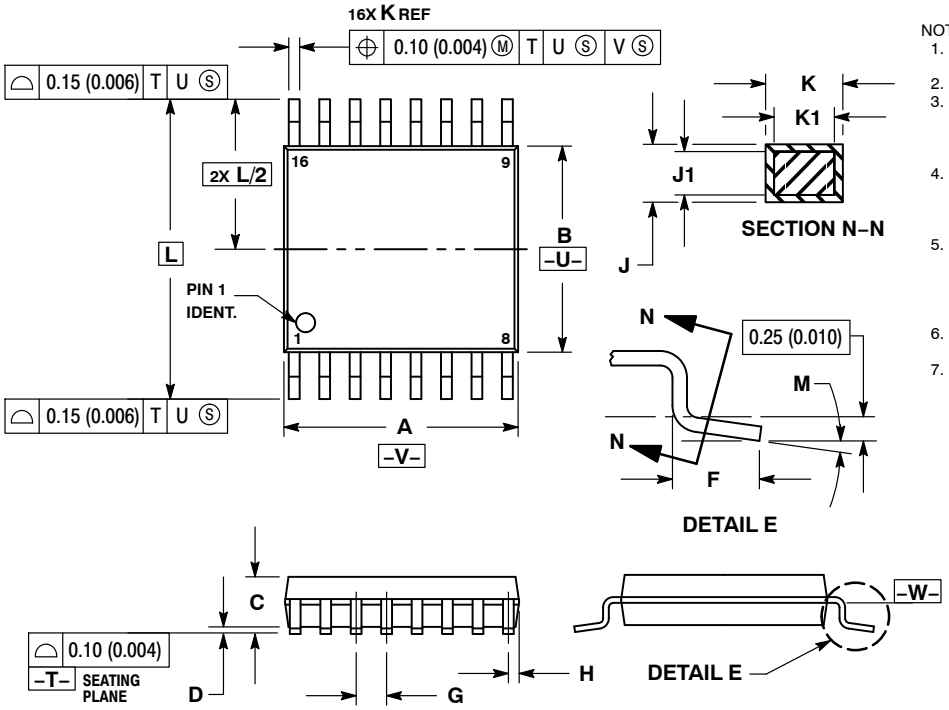
ON Semiconductor®




SCALE 2:1

**TSSOP−16**
CASE 948F−01
ISSUE B

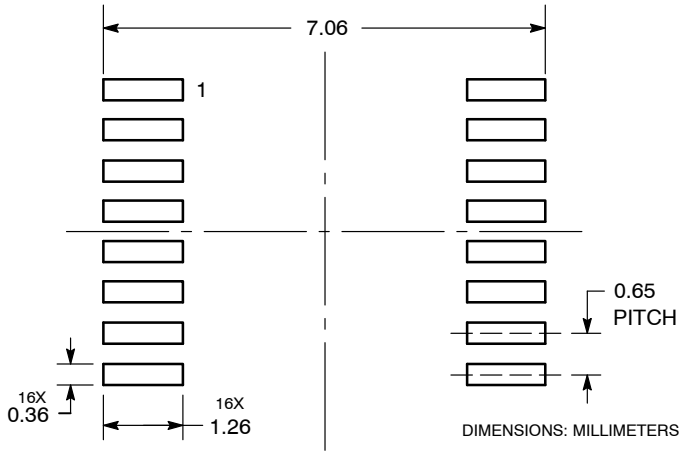
DATE 19 OCT 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

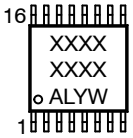
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or ▪ | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
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| DESCRIPTION: | TSSOP−16 | PAGE 1 OF 1 |

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