

# MC74LCX138

## Low-Voltage CMOS 3-to-8 Decoder/Demultiplexer

### With 5 V-Tolerant Inputs

The MC74LCX138 is a high performance, 3-to-8 decoder/demultiplexer operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX138 inputs to be safely driven from 5 V devices. The MC74LCX138 is suitable for memory address decoding and other TTL level bus-oriented applications.

The MC74LCX138 high-speed 3-to-8 decoder/demultiplexer accepts three binary weighted inputs (A0, A1, A2) and, when enabled, provides eight mutually exclusive active-LOW outputs ( $\overline{O0}$ – $\overline{O7}$ ). The LCX138 features three Enable inputs, two active-LOW ( $\overline{E1}$ ,  $\overline{E2}$ ) and one active-HIGH (E3). All outputs will be HIGH unless  $\overline{E1}$  and  $\overline{E2}$  are LOW, and E3 is HIGH. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LCX138 devices and one inverter (see Figure 1). The LCX138 can be used as an 8-output demultiplexer by using one of the active-LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Current drive capability is 24 mA at the outputs.

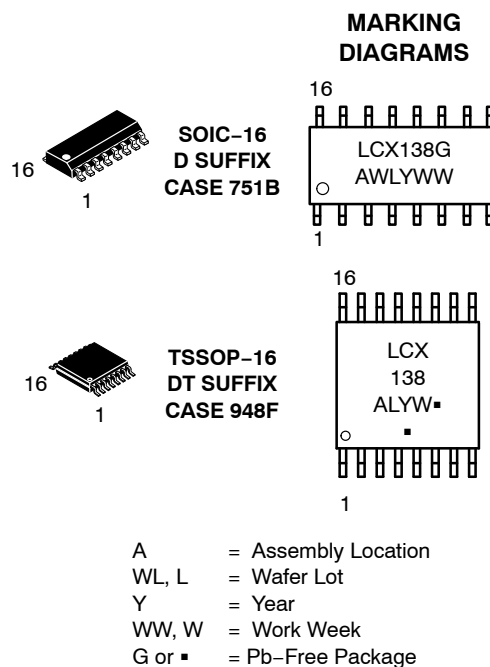
#### Features

- Designed for 2.3 V to 3.6 V  $V_{CC}$  Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V  
Machine Model >200 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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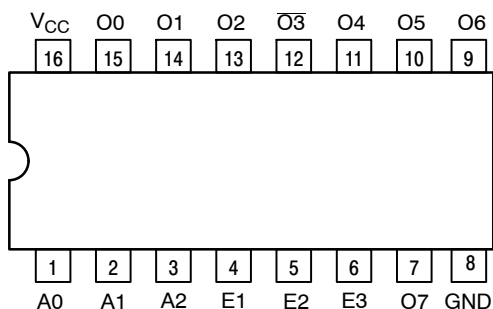


Figure 1. Pinout: 16-Lead (Top View)

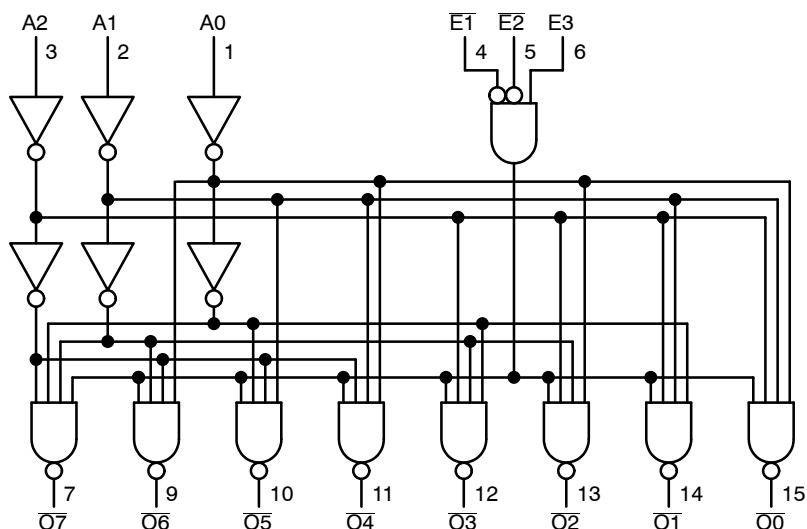


Figure 2. Logic Diagram

## PIN NAMES

Pins	Function
A0-A2	Address Inputs
E1-E2	Enable Inputs
E3	Enable Input
O0-O7	Outputs

## TRUTH TABLE

Inputs						Outputs							
E1	E2	E3	A0	A1	A2	O0	O1	O2	O3	O4	O5	O6	O7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

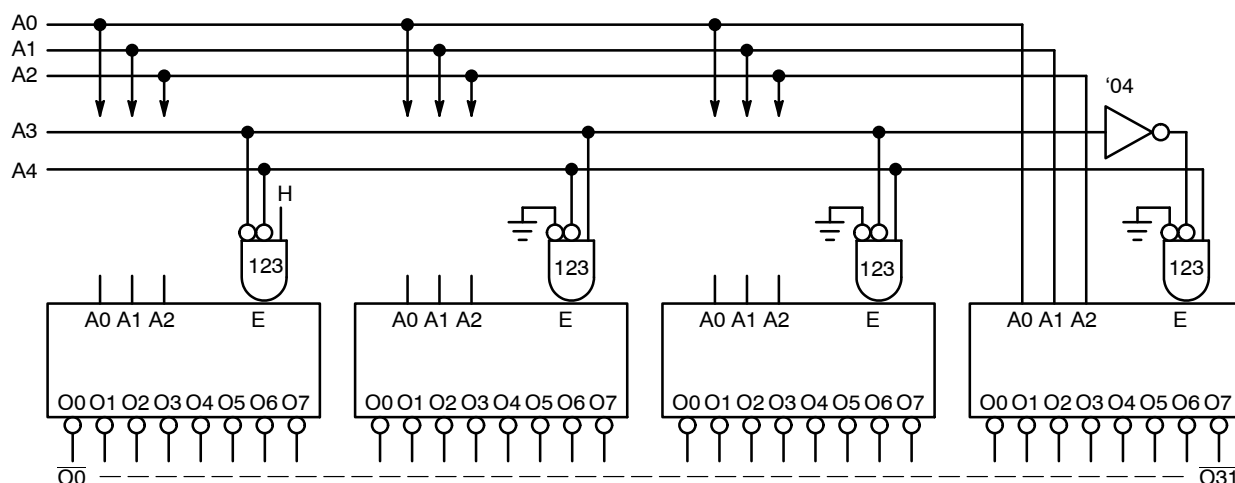
H = High Voltage Level

L = Low Voltage Level

X = High or Low Voltage Level and Transitions are Acceptable

For I<sub>CC</sub> reasons, DO NOT FLOAT Inputs

## MC74LCX138



**Figure 3. Expansion to 1-of-32 Decoding**

### ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX138DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LCX138DTG	TSSOP-16 (Pb-Free)	96 Units / Rail
MC74LCX138DTR2G	TSSOP-16 (Pb-Free)	2500 Tape & Reel
NLV74LCX138DR2G*	SOIC-16 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

### MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $I_O$  absolute maximum rating must be observed.

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V <sub>CC</sub>	Supply Voltage	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
V <sub>I</sub>	Input Voltage	0		5.5	V
V <sub>O</sub>	Output Voltage	0		V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH Level Output Current			-24 -12 -8	mA
I <sub>OL</sub>	LOW Level Output Current			+24 +12 +8	mA
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8 V to 2.0 V, V <sub>CC</sub> = 3.0 V	0		10	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Units
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V	1.7		V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V	2.0		
V <sub>IL</sub>	LOW Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V		0.7	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -8 mA	1.8		
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -12 mA	2.2		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -18 mA	2.4		
V <sub>OL</sub>	LOW Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA		0.2	V
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 8 mA		0.6	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 24 mA		0.55	
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>CC</sub> = 0, V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V		10	μA
I <sub>IN</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND		±5	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND		10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		500	μA

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

## AC CHARACTERISTICS (t<sub>R</sub> = t<sub>F</sub> = 2.5 ns; R<sub>L</sub> = 500 Ω)

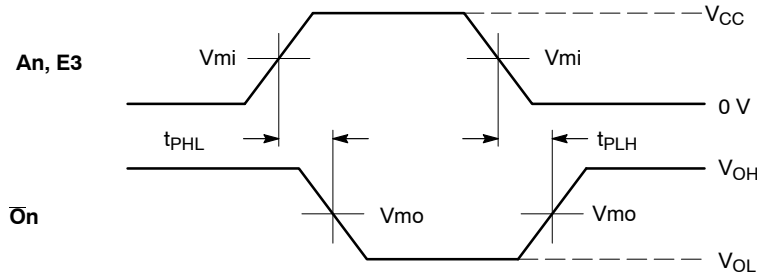
Symbol	Parameter	Waveform	Limits						Units
			T <sub>A</sub> = -40°C to +85°C						
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		
			C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay An to $\bar{O}n$	1, 2	1.5	6.0	1.5	7.0	1.5	7.2	ns
			1.5	6.0	1.5	7.0	1.5	7.2	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E1, E2 to $\bar{O}n$	2	1.5	6.5	1.5	7.5	1.5	8.4	ns
			1.5	6.5	1.5	7.5	1.5	8.4	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E3 to $\bar{O}n$	1	1.5	6.0	1.5	7.0	1.5	7.2	ns
			1.5	6.0	1.5	7.0	1.5	7.2	
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 3)		1.0	1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

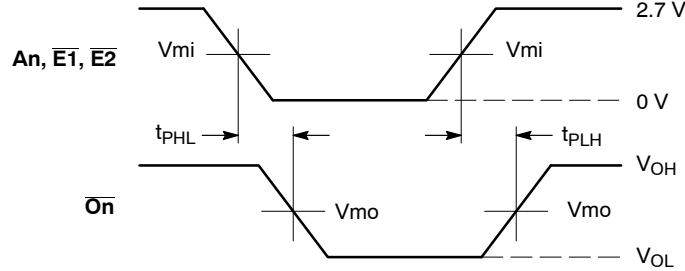
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## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = 3.3\text{ V}$ , $V_I = 0\text{ V}$ or $V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3\text{ V}$ , $V_I = 0\text{ V}$ or $V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	10 MHz, $V_{CC} = 3.3\text{ V}$ , $V_I = 0\text{ V}$ or $V_{CC}$	25	pF



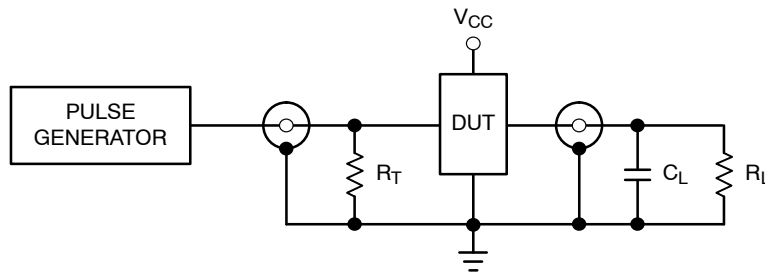
WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING OUTPUTS



WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING OUTPUTS

Symbol	$V_{CC}$		
	$3.3\text{ V} \pm 0.3\text{ V}$	$2.7\text{ V}$	$2.5\text{ V} \pm 0.2\text{ V}$
$V_{mi}$	1.5 V	1.5 V	$V_{CC}/2$
$V_{mo}$	1.5 V	1.5 V	$V_{CC}/2$

Figure 4. AC Waveforms



- $C_L = 50\text{ pF}$  at  $V_{CC} = 3.3 \pm 0.3\text{ V}$  or equivalent (includes jig and probe capacitance)
- $C_L = 30\text{ pF}$  at  $V_{CC} = 2.5 \pm 0.2\text{ V}$  or equivalent (includes jig and probe capacitance)
- $R_L = R_1 = 500\ \Omega$  or equivalent
- $R_T = Z_{OUT}$  of pulse generator (typically  $50\ \Omega$ )

Figure 5. Test Circuit

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> |  |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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