MOSFET – Power, Single **N-Channel** 40 V. 10.3 mΩ. 37 A

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C468NLWF Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	40	V
Gate-to-Source Voltage	Э		V _{GS}	±20	V
Continuous Drain		T _C = 25°C	I _D	37	Α
Current R _{θJC} (Notes 1, 3)	Steady	T _C = 100°C		26	
Power Dissipation	State	T _C = 25°C	P_{D}	28	W
R _{θJC} (Note 1)		T _C = 100°C		14	
Continuous Drain		T _A = 25°C	I _D	13	Α
Current R _{θJA} (Notes 1, 2, 3)	Steady	T _A = 100°C		9.2	
Power Dissipation	State	T _A = 25°C	P_{D}	3.5	W
R _{θJA} (Notes 1 & 2)		T _A = 100°C		1.7	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I _{DM}	190	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	–55 to + 175	°C
Source Current (Body Diode)			Is	31	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 2 A)			E _{AS}	95	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	5.3	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	43	

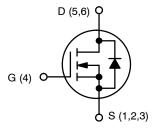
- 1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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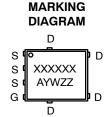
V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX	
40 V	10.3 mΩ @ 10 V	37 A	
40 V	17.6 mΩ @ 4.5 V	37 A	



N-CHANNEL MOSFET



DFN5 (SO-8FL) CASE 488AA STYLE 1



XXXXXX = 5C468L

(NVMFS5C468NL) or

468LWF

(NVMFS5C468NLWF)

= Assembly Location

= Year

W = Work Week

ZΖ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit	
OFF CHARACTERISTICS	<u> </u>				-	-	-	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				24		mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25 °C			10		
		V _{DS} = 40 V	T _J = 125°C			250	μΑ	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _G	_S = 20 V			100	nA	
ON CHARACTERISTICS (Note 4)								
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 20 \mu A$		1.2		2.0	V	
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-4.8		mV/°C	
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A		8.6	10.3	mΩ	
		V _{GS} = 4.5 V	I _D = 20 A		14.5	17.6		
Forward Transconductance	9 _{FS}	V _{DS} =15 V, I _D = 20 A			33		S	
CHARGES, CAPACITANCES & GATE F	RESISTANCE							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V			570			
Output Capacitance	C _{OSS}				230		pF	
Reverse Transfer Capacitance	C _{RSS}				11			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 20 V; I _D = 20 A			7.3		nC	
Total Gate Charge	Q _{G(TOT)}				3.4		nC	
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 20 \text{ V}; I_D = 20 \text{ A}$			0.9			
Gate-to-Source Charge	Q _{GS}				1.6		nC	
Gate-to-Drain Charge	Q_{GD}				1.0			
Plateau Voltage	V_{GP}				3.4		V	
SWITCHING CHARACTERISTICS (Note	e 5)							
Turn-On Delay Time	t _{d(ON)}				7			
Rise Time	t _r	V _{GS} = 4.5 V, V _I	ns = 20 V,		43		1	
Turn-Off Delay Time	t _{d(OFF)}	V_{GS} = 4.5 V, V_{DS} = 20 V, I_{D} = 20 A, R_{G} = 1 Ω			11		- ns	
Fall Time	t _f				2			
DRAIN-SOURCE DIODE CHARACTER	ISTICS				•	•		
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.88	1.2	.,	
		$I_{S} = 20 \text{ A}^{'}$	T _J = 125°C		0.79		V	
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } dI_{S}/dt = 100 \text{ A}/\mu\text{s,}$ $I_{S} = 20 \text{ A}$			18			
Charge Time	t _a				9		ns	
Discharge Time	t _b				9			
Reverse Recovery Charge	Q _{RR}				6.0		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300~\mu s$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

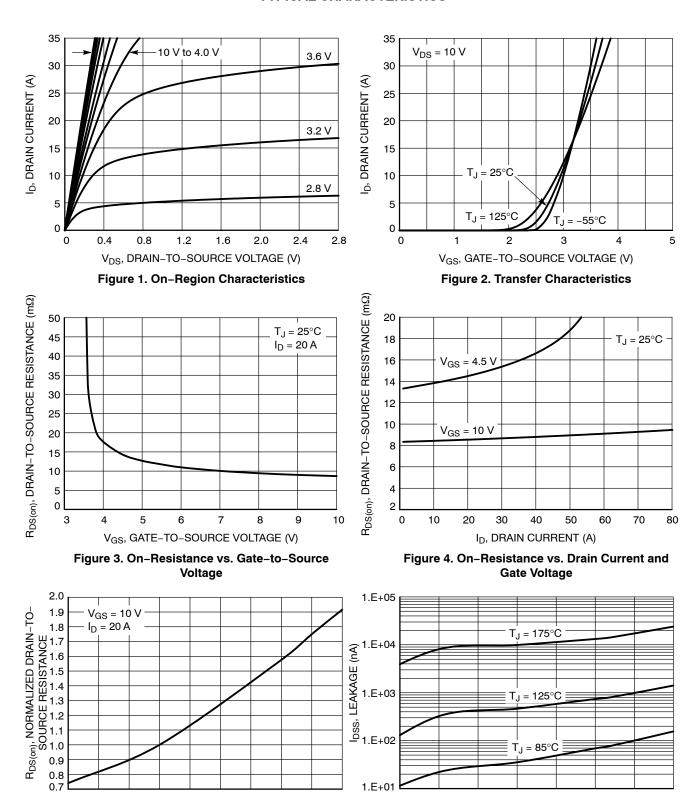


Figure 5. On–Resistance Variation with Temperature

T_J, JUNCTION TEMPERATURE (°C)

75

100

150

175

10

15

50

-50

-25

Figure 6. Drain-to-Source Leakage Current vs. Voltage

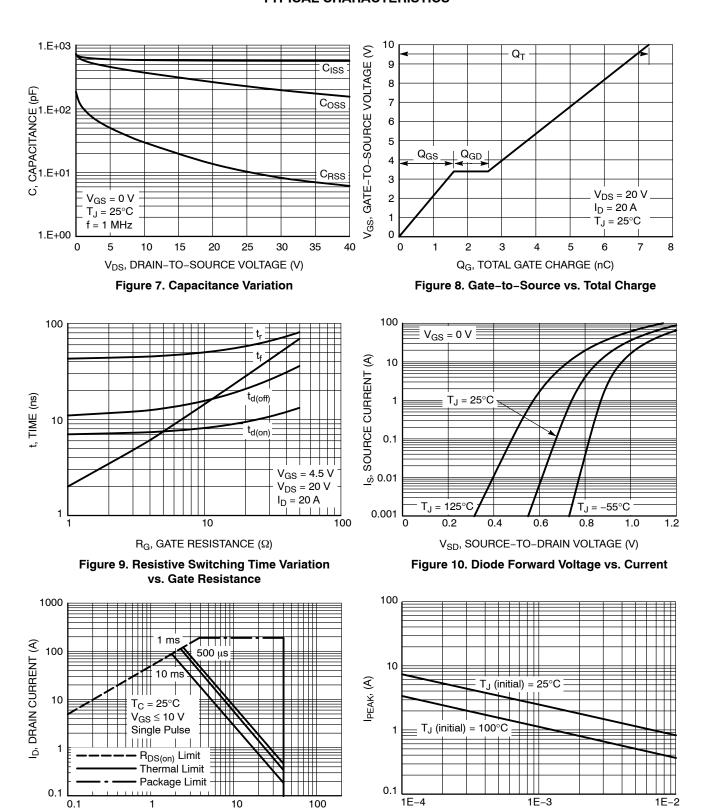
V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

25

40

20

TYPICAL CHARACTERISTICS



 $V_{DS}(V)$ Figure 11. Safe Operating Area

TIME IN AVALANCHE (s) Figure 12. I_{PEAK} vs. Time in Avalanche

100

TYPICAL CHARACTERISTICS

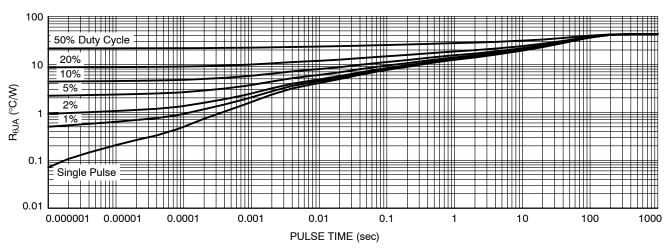


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS5C468NLT1G	5C468L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C468NLWFT1G	468LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C468NLT3G	5C468L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C468NLWFT3G	468LWF	DFN5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C468NLAFT1G	5C468L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C468NLWFAFT1G	468LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



0.10

0.10

SIDE VIEW

DFN5 5x6, 1.27P (SO-8FL) CASE 488AA ISSUE N

DATE 25 JUN 2018

NOTES:

BURRS

- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE

	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.90	1.00	1.10	
A1	0.00		0.05	
b	0.33	0.41	0.51	
С	0.23	0.28	0.33	
D	5.00	5.15	5.30	
D1	4.70	4.90	5.10	
D2	3.80	4.00	4.20	
E	6.00	6.15	6.30	
E1	5.70	5.90	6.10	
E2	3.45	3.65	3.85	
е	1.27 BSC			
G	0.51	0.575	0.71	
K	1.20	1.35	1.50	
L	0.51	0.575	0.71	
L1	0.125 REF			
M	3.00	3.40	3.80	
A	0 0		12 °	

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code

= Assembly Location Α

Υ = Year W = Work Week ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.





DETAIL A

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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