

MOSFET - Power, N-Channel, Shielded Gate

60 V, 5.2 mΩ, 78 A

NTTFS5D1N06HL

General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced MOSFET process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 5.2 mΩ at $V_{GS} = 10$ V, $I_D = 16$ A
- Max $r_{DS(on)}$ = 7.1 mΩ at $V_{GS} = 4.5$ V, $I_D = 13$ A
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

Applications

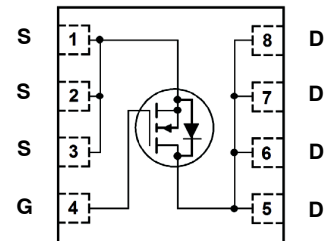
- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive



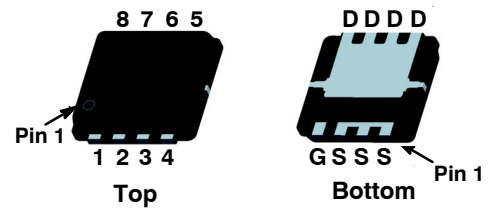
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ELECTRICAL CONNECTION

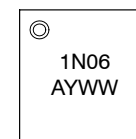


N-Channel MOSFET



WDFN8
(3.3x3.3, 0.65 P)
CASE 511DY

MARKING DIAGRAM



1N06	= Device Code
A	= Assembly Location
Y	= Year Code
WW	= Work Week Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NTTFS5D1N06HL

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
V_{DS}	Drain to Source Voltage	60	V	
V_{GS}	Gate to Source Voltage	± 20	V	
I_D	Drain Current	-Continuous $T_C = 25^\circ\text{C}$ (Note 5)	78	A
		-Continuous $T_C = 100^\circ\text{C}$ (Note 5)	49	
		-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	18	
		-Pulsed (Note 4)	216	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	72	mJ	
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	63	W	
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.2		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	39	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1N06	NTTFS5D1N06HL	WDFN8 (3.3x3.3)	7"	12 mm	1500 Units

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		37		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$			10	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = +20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 80 \mu\text{A}$	1.2	1.6	2.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 80 \mu\text{A}$, referenced to 25°C		-5.2		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}$		4.4	5.2	m Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 13 \text{ A}$		5.6	7.1	

DYNAMIC CHARACTERISTICS

C_{ISS}	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1610		pF
C_{OSS}	Output Capacitance			313		
C_{RSS}	Reverse Transfer Capacitance			12.2		
R_G	Gate Resistance			0.9		

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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SWITCHING CHARACTERISTICS

$t_{d(ON)}$	Turn – On Delay Time	$V_{DD} = 30\text{ V}, I_D = 16\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 2.5\ \Omega$		14		ns
$t_{rd(ON)}$	Rise Time			24		
$t_{d(OFF)}$	Turn – Off Delay Time			41.3		
t_f	Fall Time			12.2		
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$		22.5		nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$		10.3		
Q_{gs}	Gate to Source Charge	$V_{DD} = 30\text{ V}$ $I_D = 16\text{ A}$		5		
Q_{gd}	Gate to Drain “Miller” Charge			3		

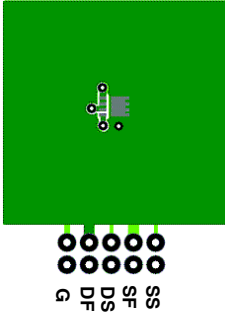
DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 16\text{ A}$ (Note 2)		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 16\text{ A}$ (Note 2)		0.66		
t_{rr}	Reverse Recovery Time	$I_F = 16\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		35.1		ns
Q_{rr}	Reverse Recovery Charge			37		nC

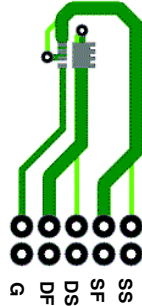
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



- 53°C/W when mounted on a 1 in² pad of 2 oz copper.



- 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- E_{AS} of 72 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 1\text{ mH}$, $I_{AS} = 12\text{ A}$, $V_{DD} = 48\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 1\text{ mH}$, $I_{AS} = 12\text{ A}$.
- Pulsed I_D please refer to SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

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TYPICAL CHARACTERISTICS

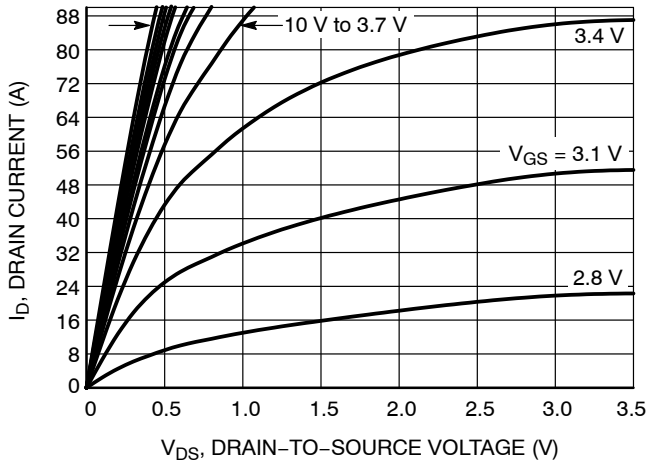


Figure 1. On-Region Characteristics

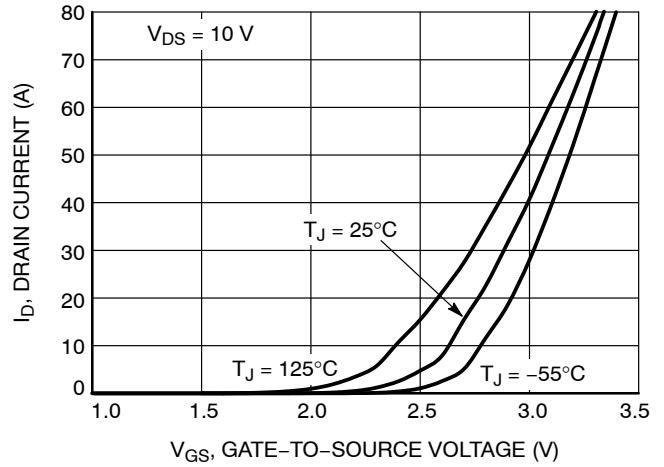


Figure 2. Transfer Characteristics

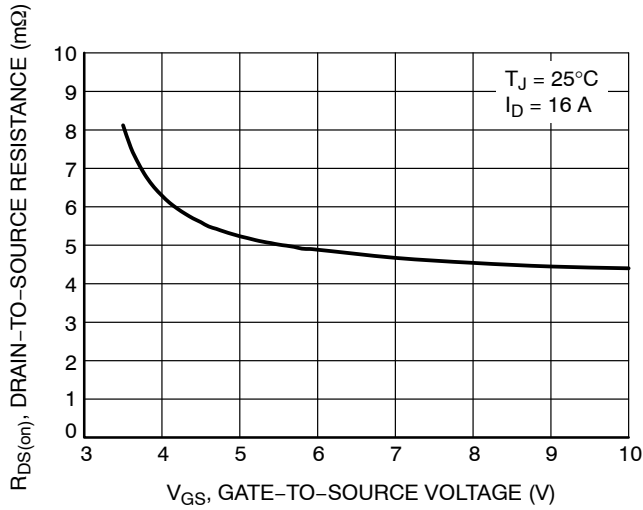


Figure 3. On-Resistance vs. Gate-to-Source Voltage

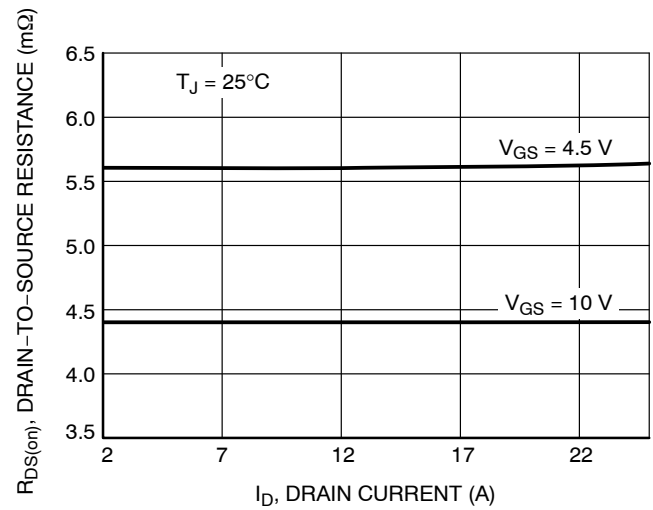


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

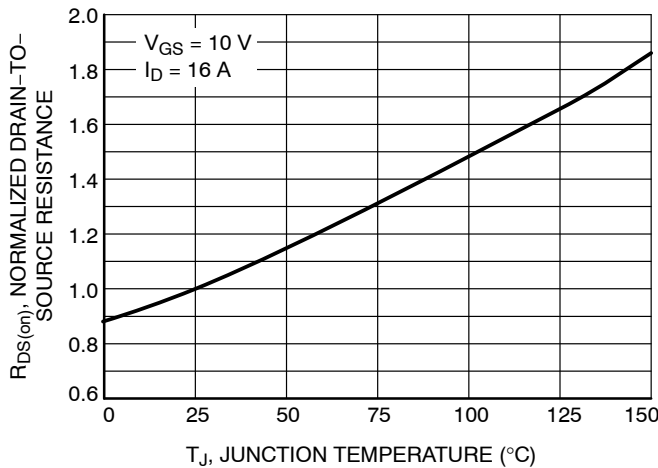


Figure 5. On-Resistance Variation with Temperature

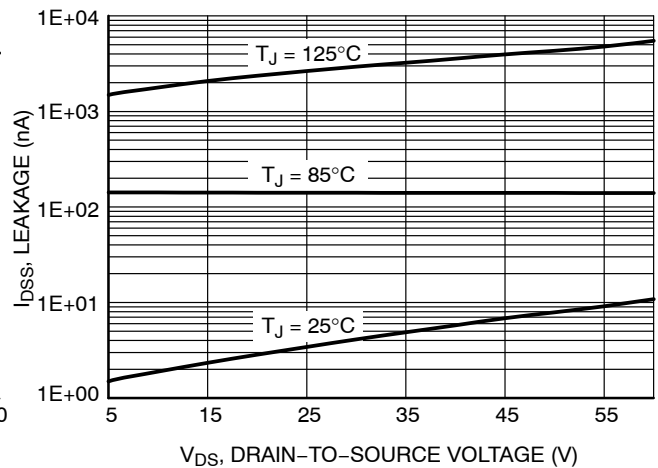


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

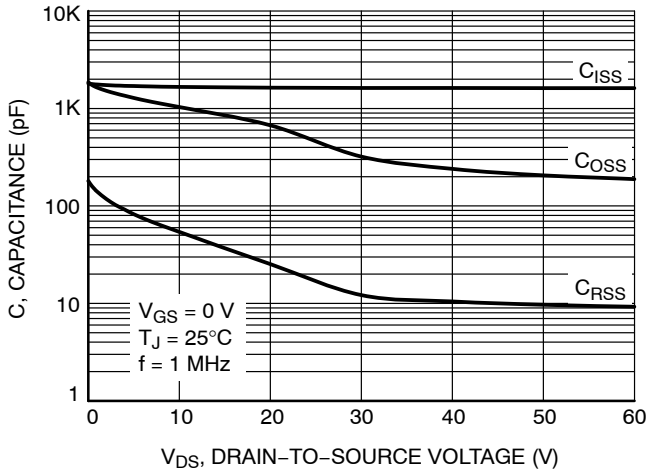


Figure 7. Capacitance Variation

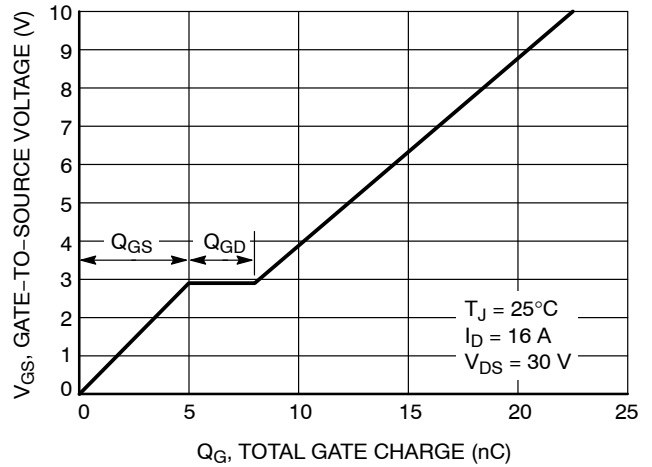


Figure 8. Gate-to-Source Voltage vs. Total Charge

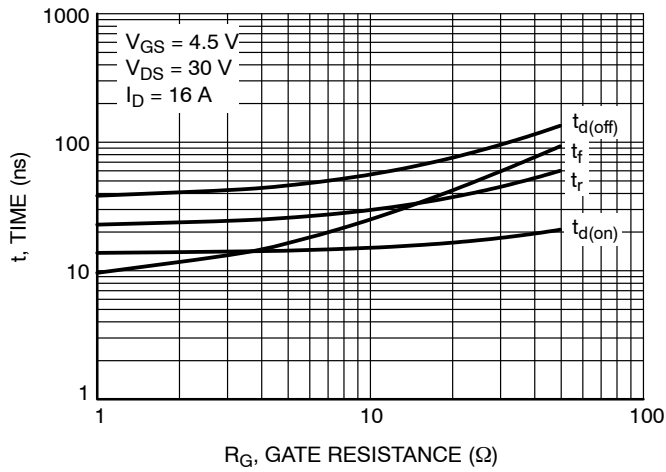


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

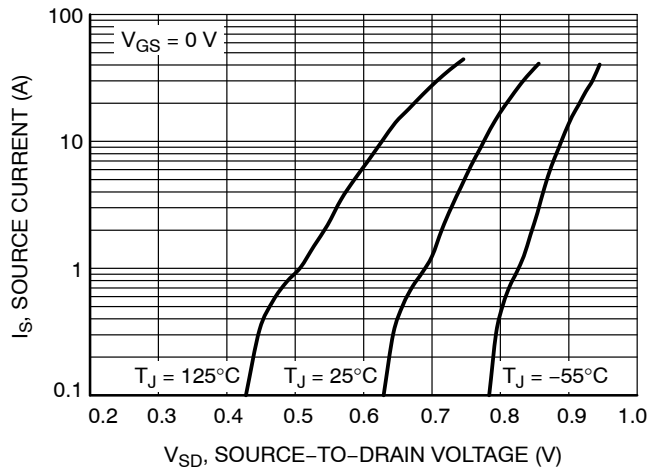


Figure 10. Diode Forward Voltage vs. Current

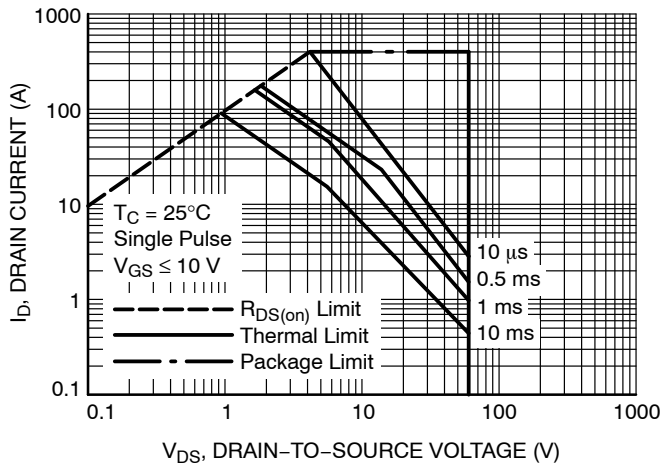


Figure 11. Maximum Rated Forward Biased Safe Operating Area

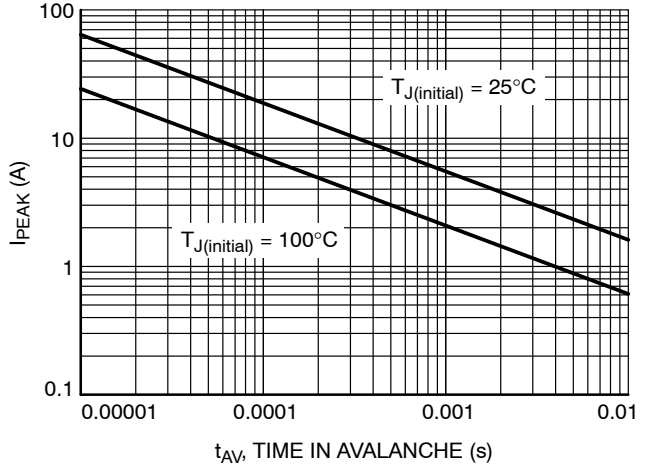


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

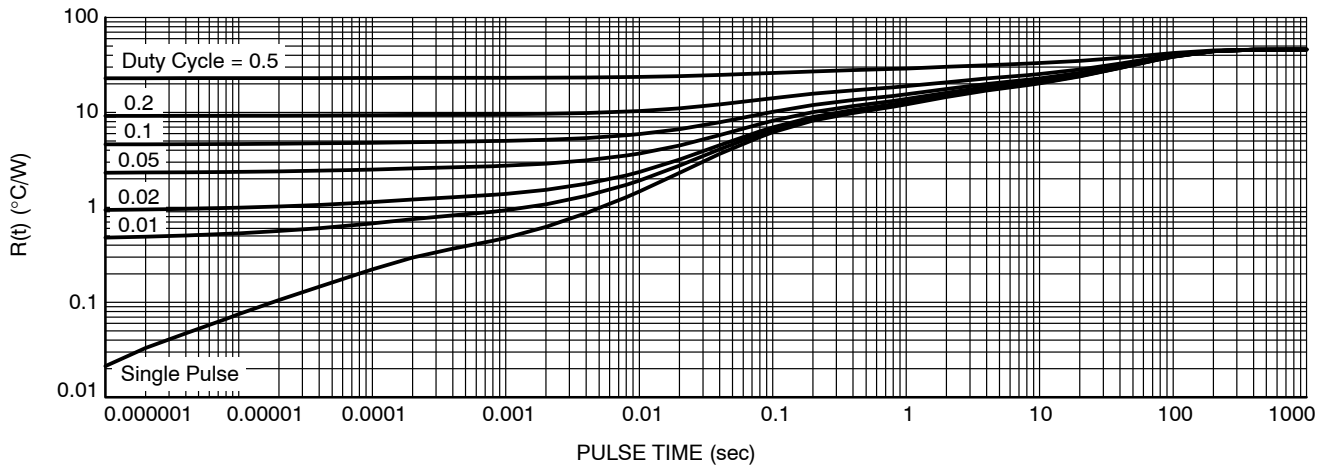


Figure 13. Transient Thermal Impedance

MECHANICAL CASE OUTLINE

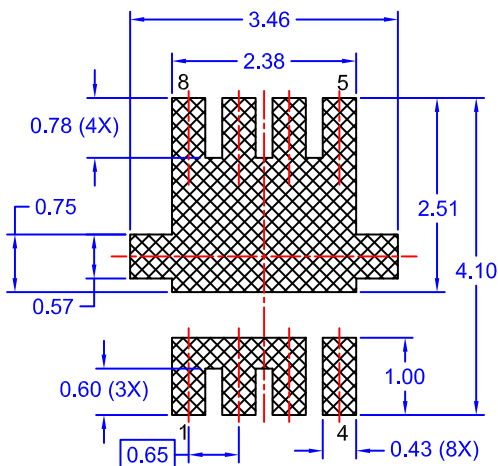
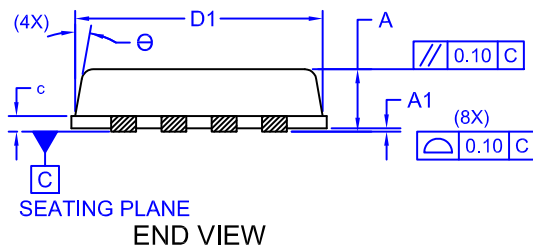
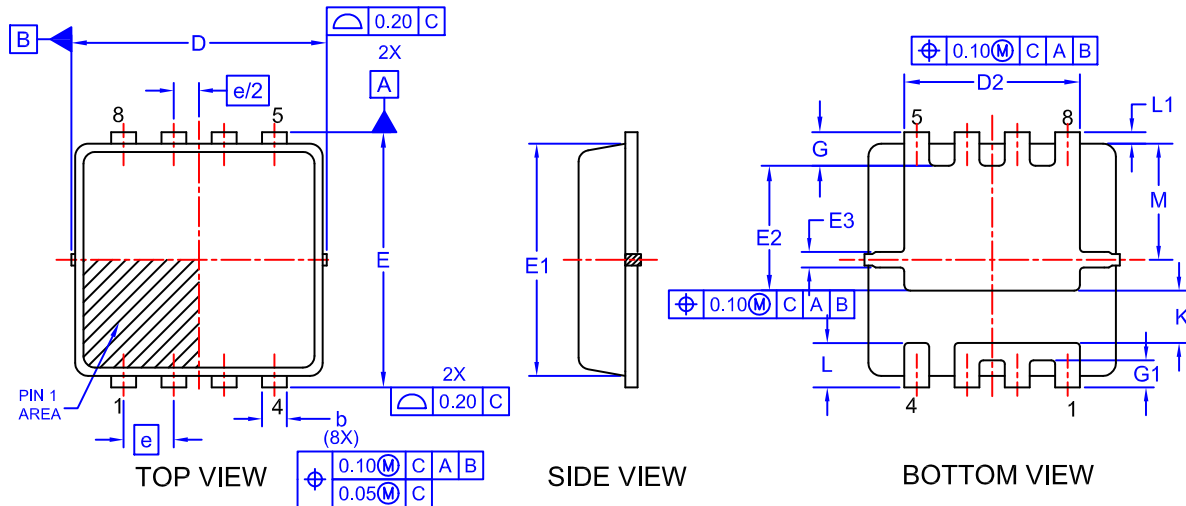
PACKAGE DIMENSIONS

ON Semiconductor®



WDFN8 3.3x3.3, 0.65P
CASE 511DY
ISSUE A

DATE 21 AUG 2018

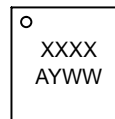


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS D1 & E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60
θ	0	-	12

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN8 3.3x3.3, 0.65P	PAGE 1 OF 1

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