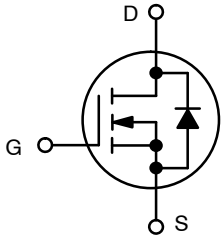
MOSFET - Single N-Channel
150 V, 4.4 mΩ, 187 A
NVBLS4D0N15MC

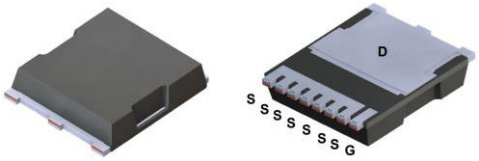
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
150 V	4.4 mΩ @ 10 V	187 A

Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation



N−CHANNEL MOSFET



Top Bottom

H−PSOF8L 11.68x9.80
MO−299A
CASE 100CU

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

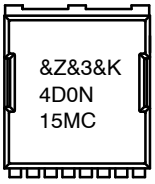
Symbol	Parameter			Value	Unit
V_{DSS}	Drain−to−Source Voltage			150	V
V_{GS}	Gate−to−Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	187	A
			T_C = 100°C	132	
P_D	Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	316	W
			T_C = 100°C	158	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	22	A
			T_A = 100°C	15	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	4	W
			T_A = 100°C	2	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		900	A
T_J, T_{stg}	Operating Junction and Storage Temperature Range			−55 to +175	°C
I_S	Source Current (Body Diode)			263	A
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy (I_{LPEAK} = 15.9 A)			2300	mJ
T_L	Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Surface−mounted on FR4 board using 1 in^2 pad size, 2 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction−to−Case − Steady State (Note 2)	0.5	°C/W
$R_{\theta JA}$	Junction−to−Ambient − Steady State (Note 2)	35.8	

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
4D0N15MC	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NVBLS4D0N15MC	MO−299A (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		150	–	–	V
$V_{(BR)DSS}$ / T_J	Drain−to−Source Breakdown Voltage Temperature Coefficient	I_D = 250 μA, ref to 25°C		–	30.23	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 120 V	T_J = 25°C	–	–	1	μA
			T_J = 125°C	–	–	10	μA
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 584 μA		2.5	3.7	4.5	V
$V_{GS(TH)}$ / T_J	Negative Threshold Temperature Coefficient	I_D = 250 μA, ref to 25°C		–	−10.12	–	mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 80 A		–	3.1	4.4	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 80 A		–	174	–	S
R_G	Gate−Resistance	T_A = 25°C		–	1.3	–	Ω
CHARGES & CAPACITANCES							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 75 V		–	7490	–	pF
C_{OSS}	Output Capacitance			–	2055	–	
C_{RSS}	Reverse Transfer Capacitance			–	27.2	–	
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 75 V, I_D = 80 A		–	90.4	–	nC
$Q_{G(TH)}$	Threshold Gate Charge			–	24.7	–	
Q_{GS}	Gate−to−Source Charge			–	40.2	–	
Q_{GD}	Gate−to−Drain Charge			–	12.6	–	
V_{GP}	Plateau Voltage			–	5.7	–	V
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
$t_{d(ON)}$	Turn−On Delay Time	V_{GS} = 10 V, V_{DS}=75 V, I_D = 80 A, R_G = 6 Ω		–	47	–	ns
t_r	Rise Time			–	115	–	
$t_{d(OFF)}$	Turn−Off Delay Time			–	58	–	
t_f	Fall Time			–	11	–	
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 80 A	T_J = 25°C	–	0.86	1.2	V
			T_J = 125°C	–	0.75	–	
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 80 A		–	84	–	ns
t_a	Charge Time			–	55	–	
t_b	Discharge Time			–	29	–	
Q_{RR}	Reverse Recovery Charge			–	180	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

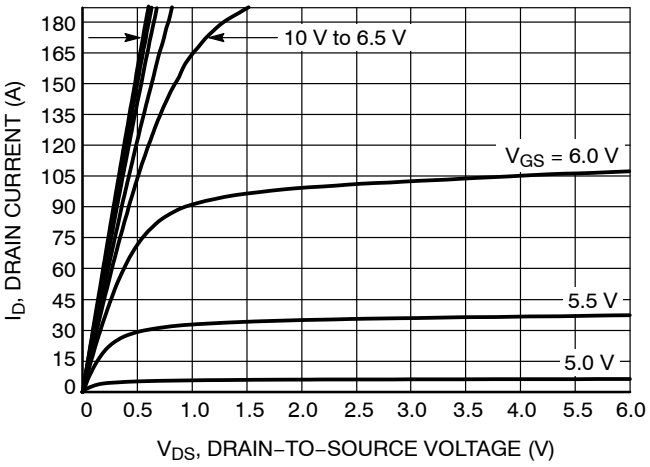


Figure 1. On−Region Characteristics

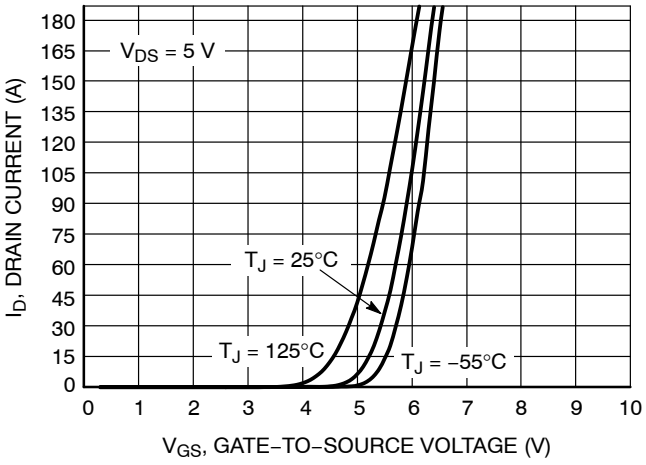


Figure 2. Transfer Characteristics

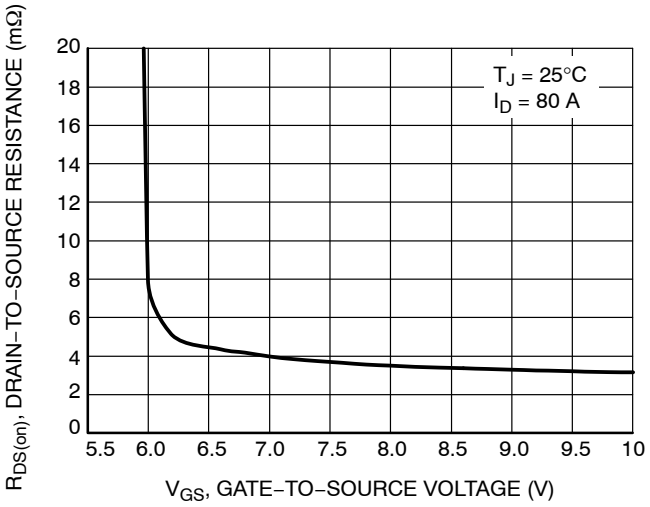


Figure 3. On−Resistance vs. V_{GS}

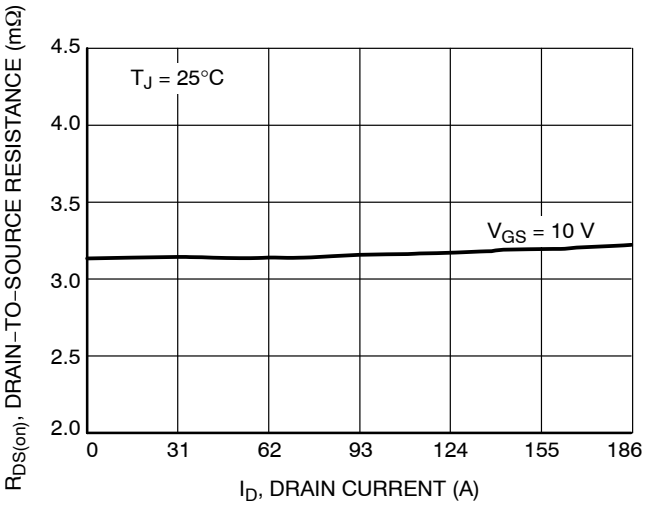


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

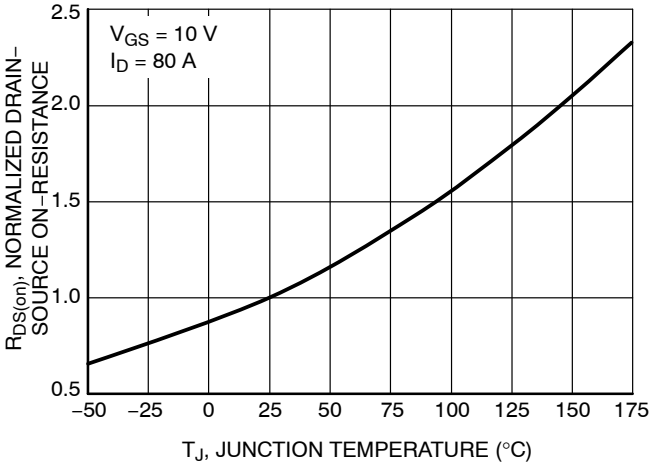


Figure 5. On−Resistance Variation with Temperature

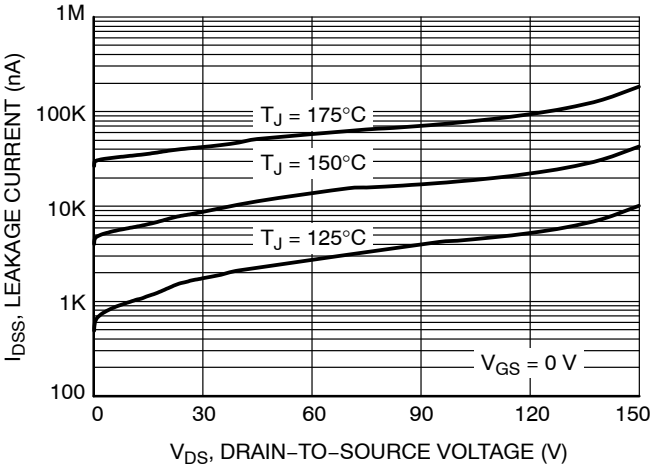


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

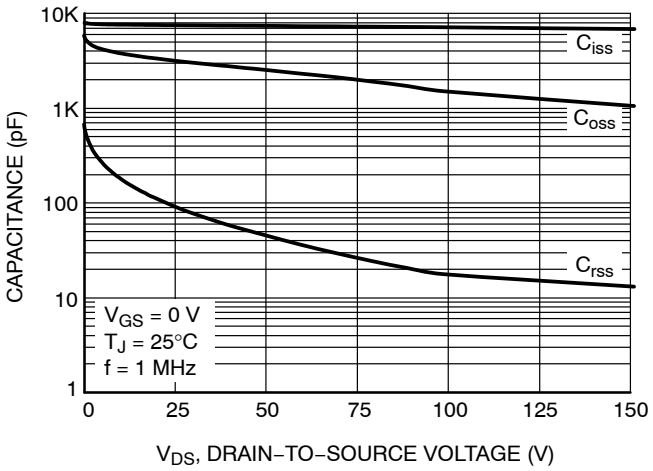


Figure 7. Capacitance Variation

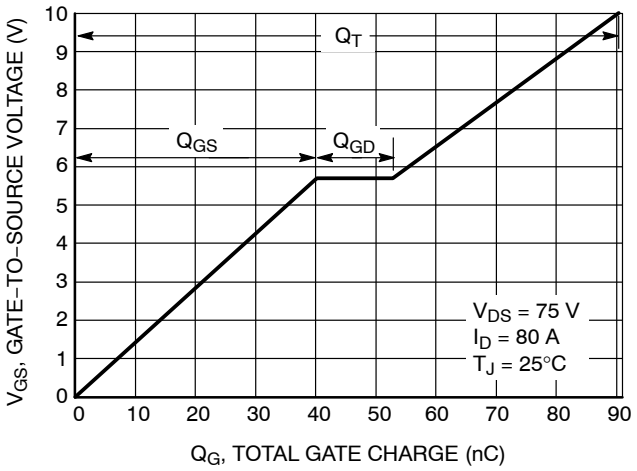


Figure 8. Gate−to−Source Voltage vs. Total Gate Charge

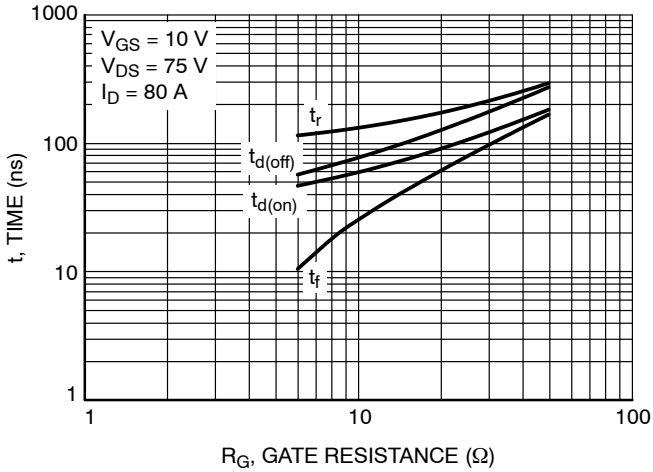


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

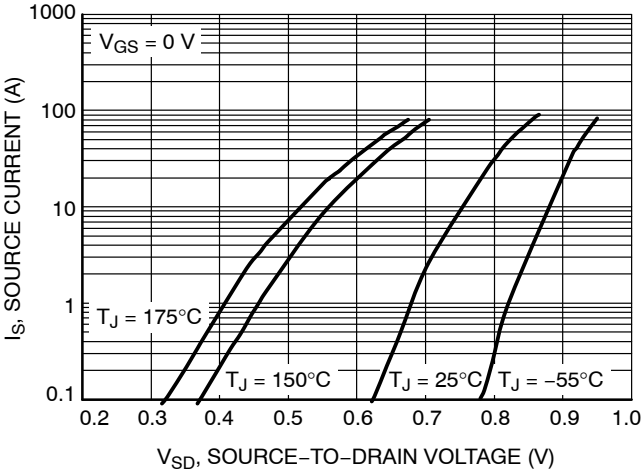


Figure 10. Diode Forward Voltage vs. Current

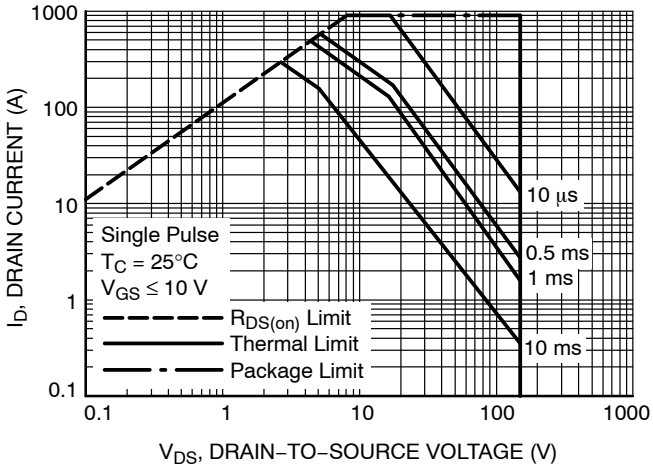


Figure 11. Maximum Rated Forward Biased Safe Operating Area

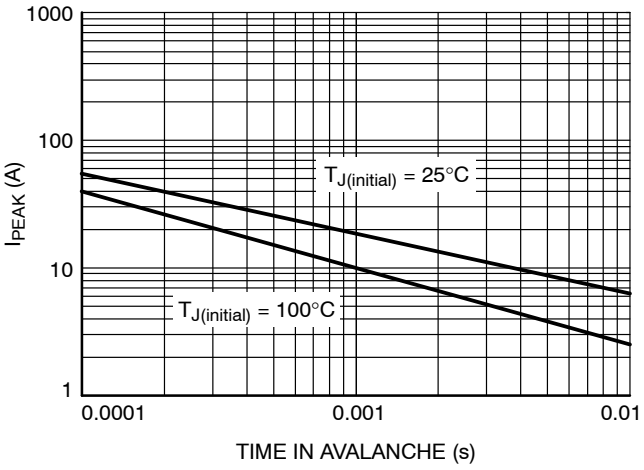


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

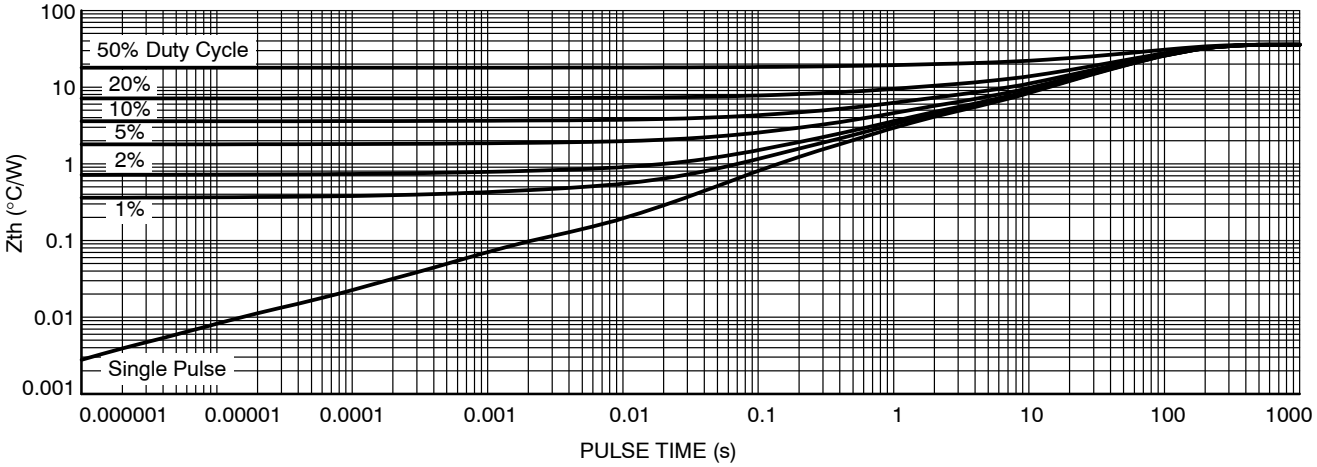
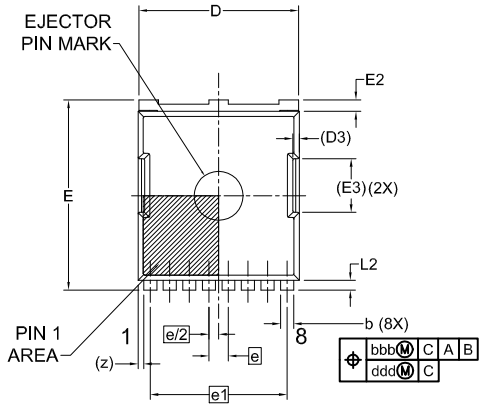


Figure 13. Thermal Characteristics (Junction−to−Ambient)

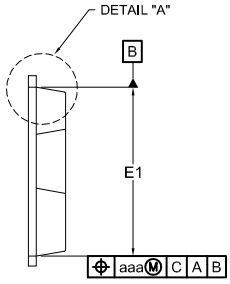
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

H−PSOF8L 11.68x9.80
CASE 100CU
ISSUE B

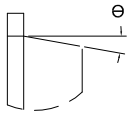
DATE 20 MAY 2022



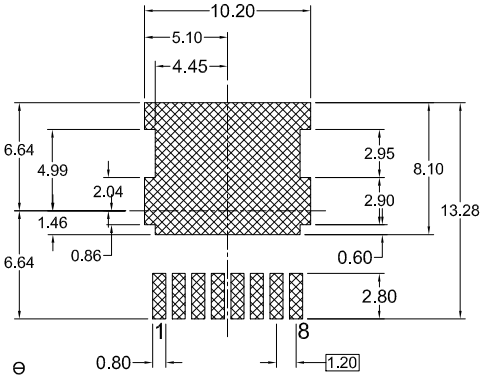
TOP VIEW



SIDE VIEW

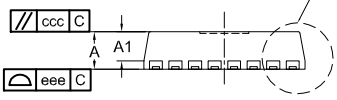


DETAIL "A"
SCALE: 2X

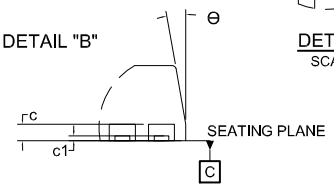


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

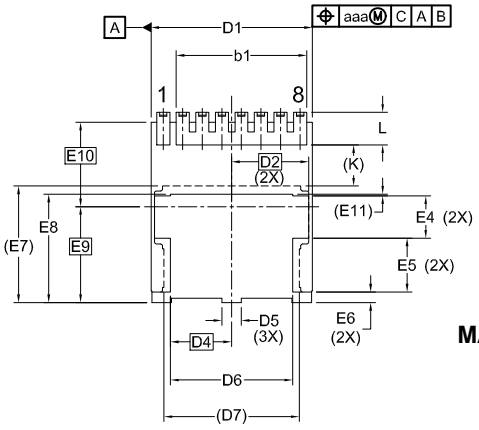


FRONT VIEW



DETAIL "B"
SCALE: 2X

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

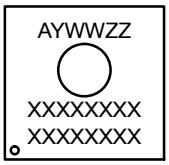


BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1		8.00 REF	
c	0.40	0.50	0.60
c1	0.10	---	---
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2		4.73 BSC	
D3		0.40 REF	
D4		3.75 BSC	
D5	---	1.20	---
D6	7.40	7.50	7.60
D7		8.30 REF	
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3		3.30 REF	
E4	---	2.60	---
E5	---	3.30	---

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E6	—	0.65	---
E7		7.15 REF	
E8	6.55	6.65	6.75
E9		5.89 BSC	
E10		5.19 BSC	
E11		0.10 REF	
e		1.20 BSC	
e/2		0.60 BSC	
e1		8.40 BSC	
K	2.43	2.53	2.63
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z		0.35 REF	
Θ	0°	---	12°
aaa		0.20	
bbb		0.25	
ccc		0.20	
ddd		0.20	
eee		0.10	

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**H−PSOF8L 11.68x9.80**	**PAGE 1 OF 1**

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For additional information, please contact your local Sales Representative

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