

# MC74VHC4066

## Quad Analog Switch/ Multiplexer/Demultiplexer

### High-Performance Silicon-Gate CMOS

The MC74VHC4066 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from  $V_{CC}$  to GND).

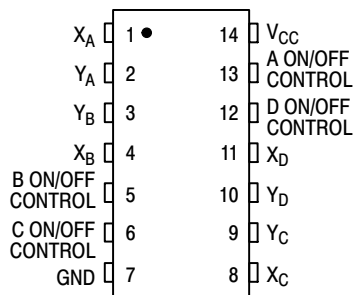
The VHC4066 is identical in pinout to the metal-gate CMOS MC14066 and the high-speed CMOS HC4066A. Each device has four independent switches. The device has been designed so that the ON resistances ( $R_{ON}$ ) are much more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the VHC4316.

#### Features

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Analog Input Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

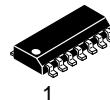
#### PIN ASSIGNMENT



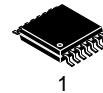
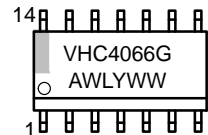
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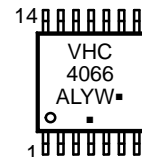
#### MARKING DIAGRAMS



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package  
(Note: Microdot may be in either location)

#### FUNCTION TABLE

| On/Off Control Input | State of Analog Switch |
|----------------------|------------------------|
| L                    | Off                    |
| H                    | On                     |

#### ORDERING INFORMATION

| Device           | Package               | Shipping†             |
|------------------|-----------------------|-----------------------|
| MC74VHC4066DR2G  | SOIC-14<br>(Pb-Free)  | 2500 / Tape<br>& Reel |
| MC74VHC4066DTR2G | TSSOP-14<br>(Pb-Free) | 2500 / Tape<br>& Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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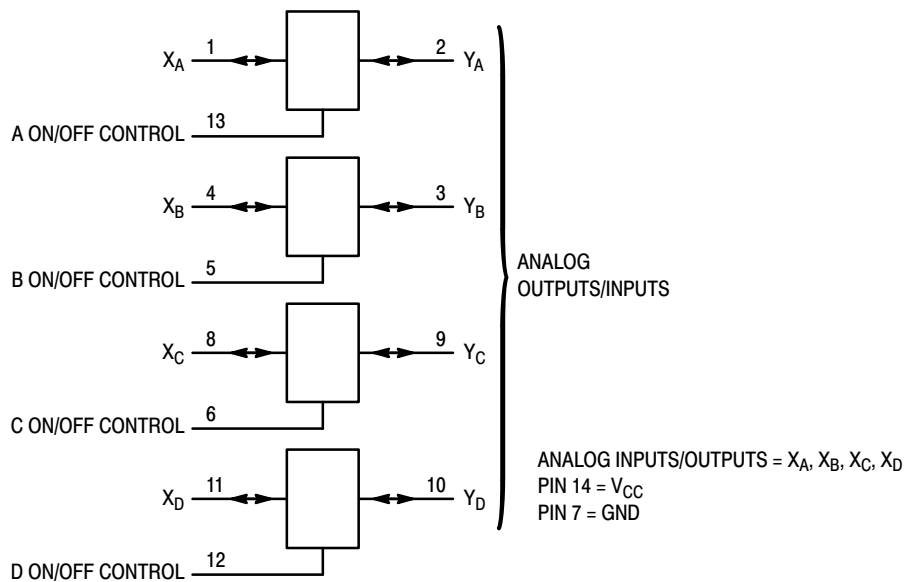


Figure 1. Logic Diagram

## MAXIMUM RATINGS

| Symbol    | Parameter   | Value                   | Unit |
|-----------|---|-------------------------|------|
| $V_{CC}$  | Positive DC Supply Voltage (Referenced to GND)                  | - 0.5 to + 14.0         | V    |
| $V_{IS}$  | Analog Input Voltage (Referenced to GND)                        | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{in}$  | Digital Input Voltage (Referenced to GND)                       | - 0.5 to $V_{CC} + 0.5$ | V    |
| I         | DC Current Into or Out of Any Pin                               | $\pm 25$                | mA   |
| $P_D$     | Power Dissipation in Still Air, SOIC Package†<br>TSSOP Package† | 500<br>450              | mW   |
| $T_{stg}$ | Storage Temperature   | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds                 | 260                     | °C   |

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C  
 TSSOP Package: - 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

## RECOMMENDED OPERATING CONDITIONS

| Symbol     | Parameter   | Min  | Max      | Unit |
|------------|---|------|----------|------|
| $V_{CC}$   | Positive DC Supply Voltage (Referenced to GND)              | 2.0  | 12.0     | V    |
| $V_{IS}$   | Analog Input Voltage (Referenced to GND)                    | GND  | $V_{CC}$ | V    |
| $V_{in}$   | Digital Input Voltage (Referenced to GND)                   | GND  | $V_{CC}$ | V    |
| $V_{IO}^*$ | Static or Dynamic Voltage Across Switch                     | —    | 1.2      | V    |
| $T_A$      | Operating Temperature, All Package Types                    | - 55 | + 125    | °C   |
| $t_r, t_f$ | Input Rise and Fall Time, ON/OFF Control Inputs (Figure 14) |      |          | ns   |
|            | $V_{CC} = 2.0 \text{ V}$                                    | 0    | 1000     |      |
|            | $V_{CC} = 3.0 \text{ V}$                                    | 0    | 600      |      |
|            | $V_{CC} = 4.5 \text{ V}$                                    | 0    | 500      |      |
|            | $V_{CC} = 9.0 \text{ V}$                                    | 0    | 400      |      |
|            | $V_{CC} = 12.0 \text{ V}$                                   | 0    | 250      |      |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

\*For voltage drops across the switch greater than 1.2 V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

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## DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

| Symbol          | Parameter   | Test Conditions   | V <sub>CC</sub><br>V | Guaranteed Limit |        |            | Unit |
|-----------------|---|---|----------------------|------------------|--------|------------|------|
|                 |   |   |                      | - 55 to<br>25°C  | ≤ 85°C | ≤<br>125°C |      |
| V <sub>IH</sub> | Minimum High-Level Voltage<br>ON/OFF Control Inputs       | R <sub>on</sub> = Per Spec  | 2.0                  | 1.5              | 1.5    | 1.5        | V    |
|                 |   |   | 3.0                  | 2.1              | 2.1    | 2.1        |      |
|                 |   |   | 4.5                  | 3.15             | 3.15   | 3.15       |      |
|                 |   |   | 9.0                  | 6.3              | 6.3    | 6.3        |      |
|                 |   |   | 12.0                 | 8.4              | 8.4    | 8.4        |      |
| V <sub>IL</sub> | Maximum Low-Level Voltage<br>ON/OFF Control Inputs        | R <sub>on</sub> = Per Spec  | 2.0                  | 0.5              | 0.5    | 0.5        | V    |
|                 |   |   | 3.0                  | 0.9              | 0.9    | 0.9        |      |
|                 |   |   | 4.5                  | 1.35             | 1.35   | 1.35       |      |
|                 |   |   | 9.0                  | 2.7              | 2.7    | 2.7        |      |
|                 |   |   | 12.0                 | 3.6              | 3.6    | 3.6        |      |
| I <sub>in</sub> | Maximum Input Leakage<br>Current<br>ON/OFF Control Inputs | V <sub>in</sub> = V <sub>CC</sub> or GND                          | 12.0                 | ± 0.1            | ± 1.0  | ± 1.0      | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply<br>Current (per Package)         | V <sub>in</sub> = V <sub>CC</sub> or GND<br>V <sub>IO</sub> = 0 V | 6.0                  | 2                | 20     | 40         | μA   |
|                 |   |   | 12.0                 | 4                | 40     | 160        |      |

## DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

| Symbol           | Parameter  | Test Conditions   | V <sub>CC</sub><br>V | Guaranteed Limit |        |            | Unit |
|------------------|--|---|----------------------|------------------|--------|------------|------|
|                  |  |   |                      | - 55 to<br>25°C  | ≤ 85°C | ≤<br>125°C |      |
| R <sub>on</sub>  | Maximum "ON" Resistance  | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = V <sub>CC</sub> to GND<br>I <sub>S</sub> ≤ 2.0 mA<br>(Figures 2 through 7)             | 2.0†                 | —                | —      | —          | Ω    |
|                  |  |   | 3.0†                 | —                | —      | —          |      |
|                  |  |   | 4.5                  | 120              | 160    | 200        |      |
|                  |  |   | 9.0                  | 70               | 85     | 100        |      |
|                  |  |   | 12.0                 | 70               | 85     | 100        |      |
|                  |  | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = V <sub>CC</sub> or GND (Endpoints)<br>I <sub>S</sub> ≤ 2.0 mA<br>(Figures 2 through 7) | 2.0                  | —                | —      | —          |      |
|                  |  |   | 3.0                  | —                | —      | —          |      |
|                  |  |   | 4.5                  | 70               | 85     | 100        |      |
|                  |  |   | 9.0                  | 50               | 60     | 80         |      |
|                  |  |   | 12.0                 | 30               | 60     | 80         |      |
| ΔR <sub>on</sub> | Maximum Difference in "ON"<br>Resistance Between Any Two<br>Channels in the Same Package | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - GND)<br>I <sub>S</sub> ≤ 2.0 mA                                 | 2.0                  | —                | —      | —          | Ω    |
|                  |  |   | 4.5                  | 20               | 25     | 30         |      |
|                  |  |   | 9.0                  | 15               | 20     | 25         |      |
|                  |  |   | 12.0                 | 15               | 20     | 25         |      |
| I <sub>off</sub> | Maximum Off-Channel<br>Leakage<br>Current, Any One Channel                               | V <sub>in</sub> = V <sub>IL</sub><br>V <sub>IO</sub> = V <sub>CC</sub> or GND<br>Switch Off   | 12.0                 | 0.1              | 0.5    | 1.0        | μA   |
| I <sub>on</sub>  | Maximum On-Channel<br>Leakage<br>Current, Any One Channel                                | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = V <sub>CC</sub> or GND   | 12.0                 | 0.1              | 0.5    | 1.0        | μA   |

†At supply voltage (V<sub>CC</sub>) approaching 3 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

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## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, ON/OFF Control Inputs: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter   | V <sub>CC</sub><br>V                    | Guaranteed Limit |        |            | Unit |
|--|---|---|------------------|--------|------------|------|
|  |   |   | - 55 to<br>25°C  | ≤ 85°C | ≤<br>125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Analog Input to Analog Output<br>(Figures 18 and 13)   | 2.0                                     | 40               | 50     | 60         | ns   |
|  |   | 3.0                                     | 30               | 40     | 50         |      |
|  |   | 4.5                                     | 5                | 7      | 8          |      |
|  |   | 9.0                                     | 5                | 7      | 8          |      |
|  |   | 12.0                                    | 5                | 7      | 8          |      |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, ON/OFF Control to Analog Output<br>(Figures 14 and 15) | 2.0                                     | 80               | 90     | 110        | ns   |
|  |   | 3.0                                     | 60               | 70     | 80         |      |
|  |   | 4.5                                     | 20               | 25     | 35         |      |
|  |   | 9.0                                     | 20               | 25     | 35         |      |
|  |   | 12.0                                    | 20               | 25     | 35         |      |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, ON/OFF Control to Analog Output<br>(Figures 14 and 15) | 2.0                                     | 80               | 90     | 100        | ns   |
|  |   | 3.0                                     | 45               | 50     | 60         |      |
|  |   | 4.5                                     | 20               | 25     | 30         |      |
|  |   | 9.0                                     | 20               | 25     | 30         |      |
|  |   | 12.0                                    | 20               | 25     | 30         |      |
| C                                      | Maximum Capacitance   | ON/OFF Control Input                    | —                | 10     | 10         | pF   |
|  |   | Control Input = GND                     | —                | 35     | 35         |      |
|  |   | Analog I/O<br>Feedthrough               | —                | 1.0    | 1.0        |      |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Per Switch) (Figure 17)*                           | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |                  |        | pF         |      |
|  |   | 15                                      |                  |        |            |      |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

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## ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter  | Test Conditions  | V <sub>CC</sub><br>V                         | Limit*<br>25°C<br>74HC                           | Unit             |
|--------|--|--|--|--|------------------|
| BW     | Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure NO TAG) | f <sub>in</sub> = 1 MHz Sine Wave<br>Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub><br>Increase f <sub>in</sub> Frequency Until dB Meter Reads - 3 dB<br><br>R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF  | 4.5<br>9.0<br>12.0                           | 150<br>160<br>160                                | MHz              |
| —      | Off-Channel Feedthrough Isolation (Figure NO TAG)                          | f <sub>in</sub> ≡ Sine Wave<br>Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub><br>f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF<br><br>f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF                               | 4.5<br>9.0<br>12.0<br><br>4.5<br>9.0<br>12.0 | - 50<br>- 50<br>- 50<br><br>- 40<br>- 40<br>- 40 | dB               |
| —      | Feedthrough Noise, Control to Switch (Figure NO TAG)                       | V <sub>in</sub> ≤ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns)<br>Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A<br>R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF<br><br>R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF  | 4.5<br>9.0<br>12.0<br><br>4.5<br>9.0<br>12.0 | 60<br>130<br>200<br><br>30<br>65<br>100          | mV <sub>PP</sub> |
| —      | Crosstalk Between Any Two Switches (Figure 16)                             | f <sub>in</sub> ≡ Sine Wave<br>Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub><br>f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF<br><br>f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF                               | 4.5<br>9.0<br>12.0<br><br>4.5<br>9.0<br>12.0 | - 70<br>- 70<br>- 70<br><br>- 80<br>- 80<br>- 80 | dB               |
| THD    | Total Harmonic Distortion (Figure 20)                                      | f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF<br>THD = THD <sub>Measured</sub> - THD <sub>Source</sub><br>V <sub>IS</sub> = 4.0 V <sub>PP</sub> sine wave<br>V <sub>IS</sub> = 8.0 V <sub>PP</sub> sine wave<br>V <sub>IS</sub> = 11.0 V <sub>PP</sub> sine wave | 4.5<br>9.0<br>12.0                           | 0.10<br>0.06<br>0.04                             | %                |

\*Guaranteed limits not tested. Determined by design and verified by qualification.

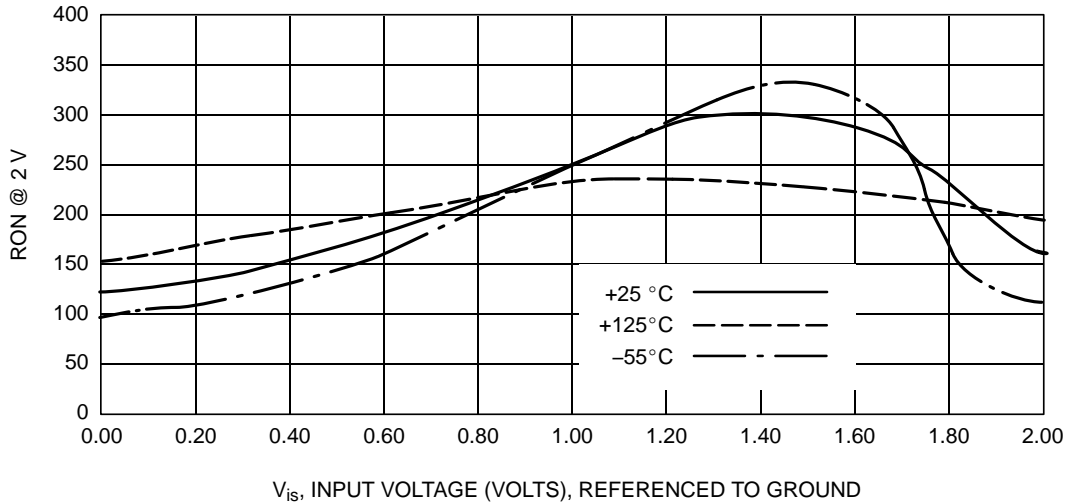


Figure 2. Typical On Resistance, V<sub>CC</sub> = 2.0 V

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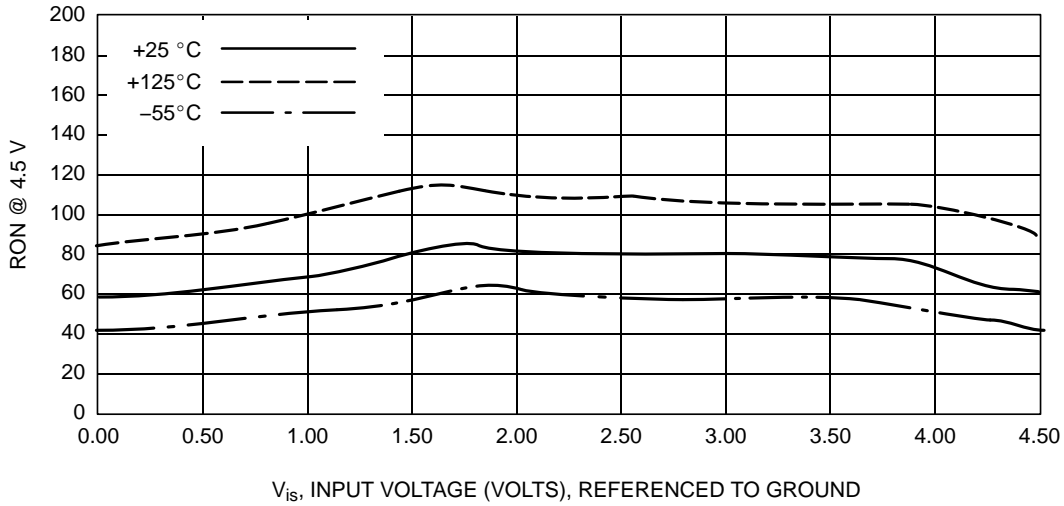


Figure 3. Typical On Resistance, V<sub>CC</sub> = 4.5 V

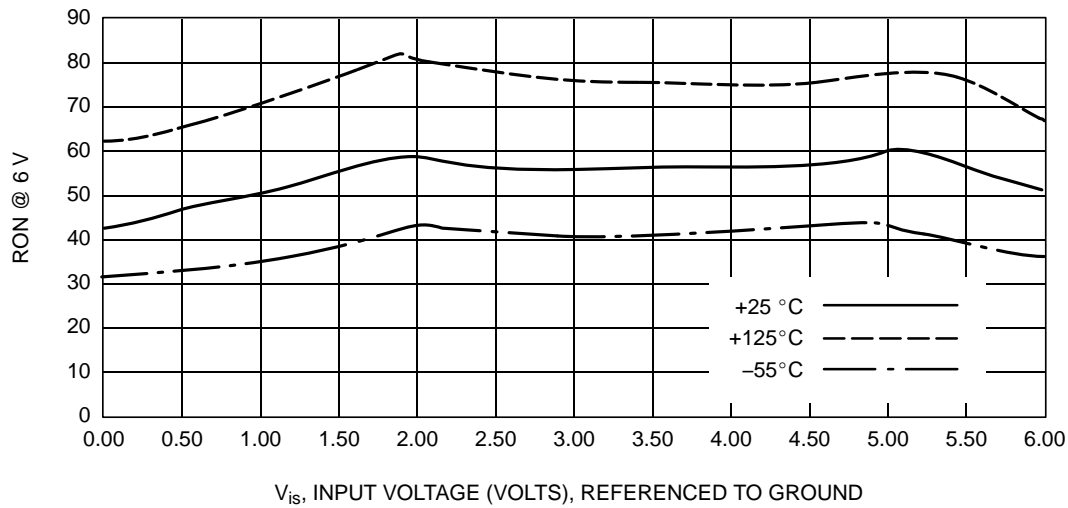


Figure 4. Typical On Resistance, V<sub>CC</sub> = 6.0 V

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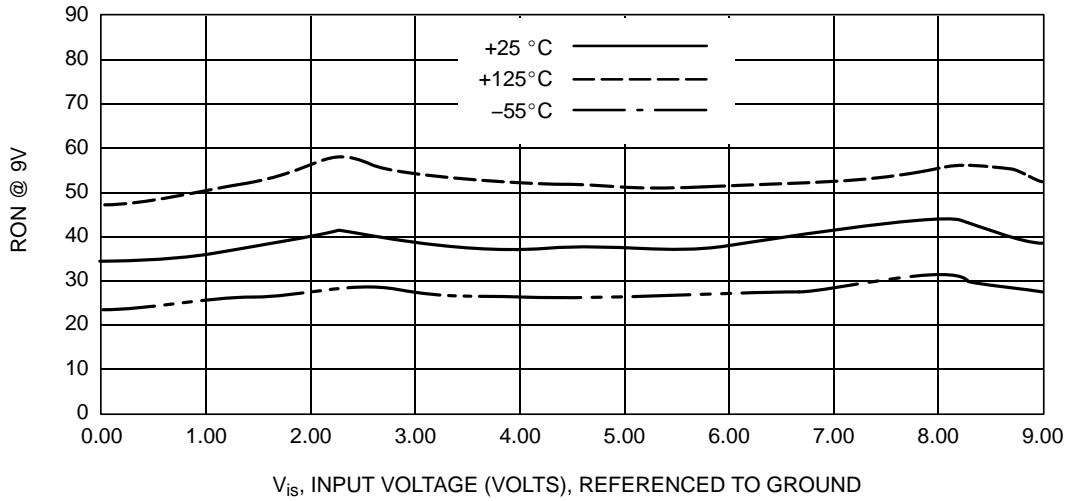


Figure 5. Typical On Resistance, V<sub>CC</sub> = 9.0 V

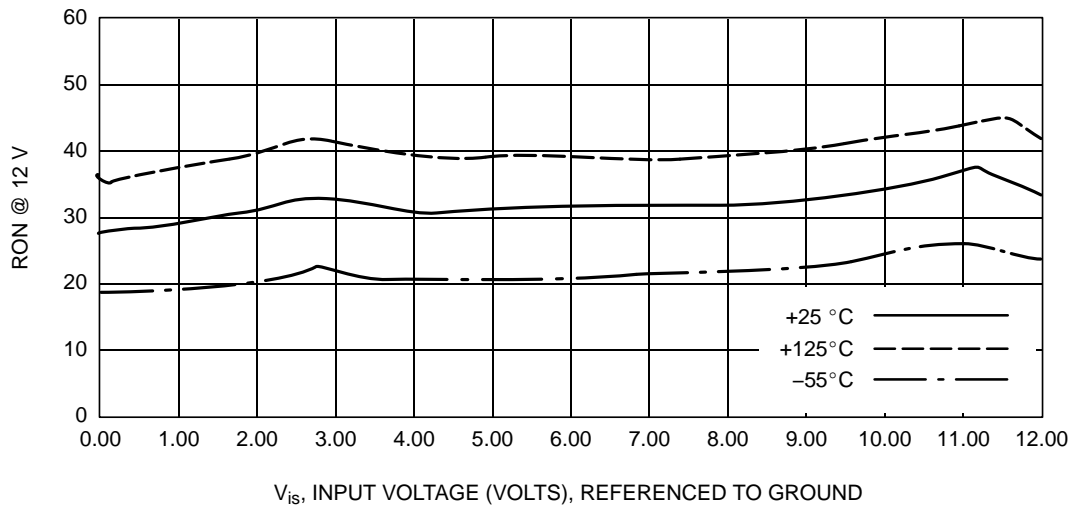


Figure 6. Typical On Resistance, V<sub>CC</sub> = 12 V

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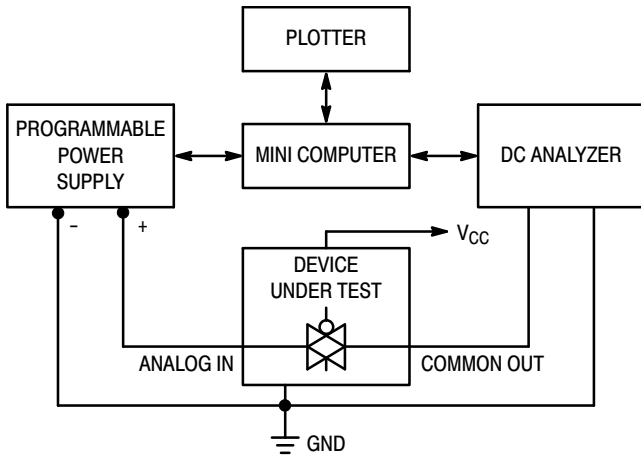


Figure 7. On Resistance Test Set-Up

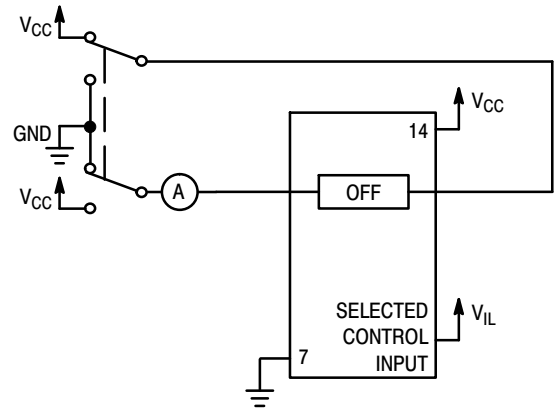


Figure 8. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

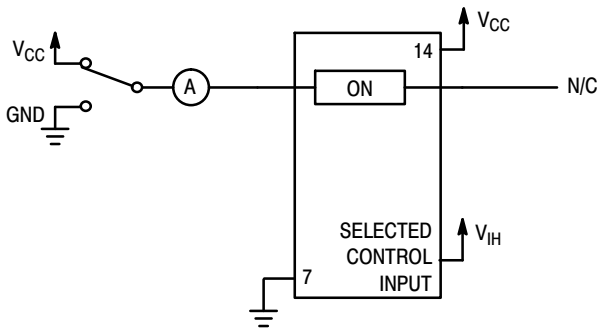
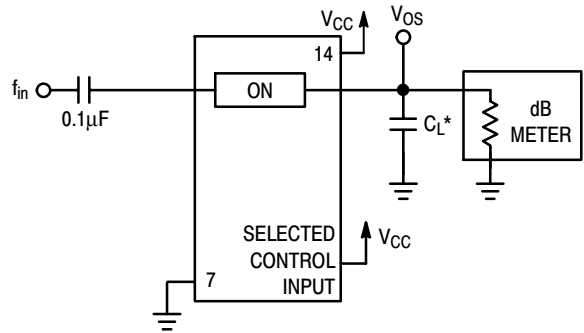
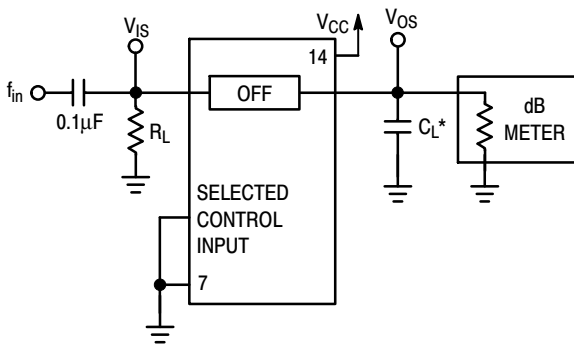


Figure 9. Maximum On Channel Leakage Current, Test Set-Up



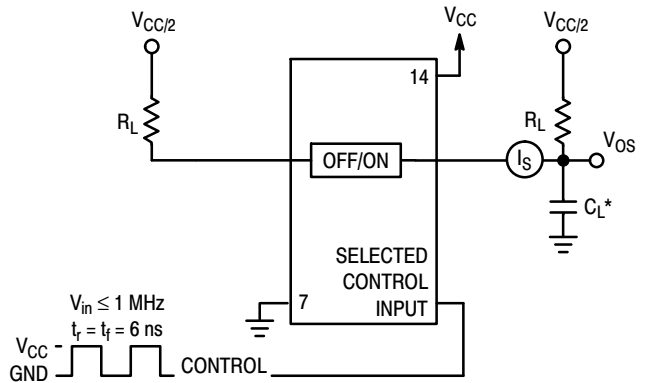
\*Includes all probe and jig capacitance.

Figure 10. Maximum On-Channel Bandwidth Test Set-Up



\*Includes all probe and jig capacitance.

Figure 11. Off-Channel Feedthrough Isolation, Test Set-Up

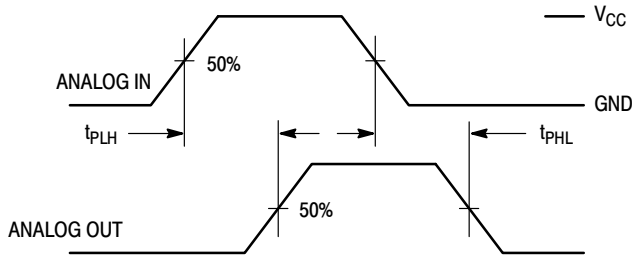


\*Includes all probe and jig capacitance.

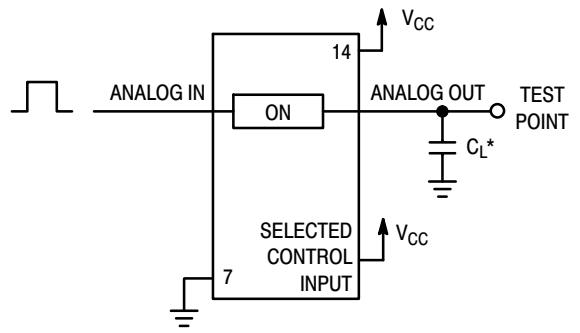
Figure 12. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up



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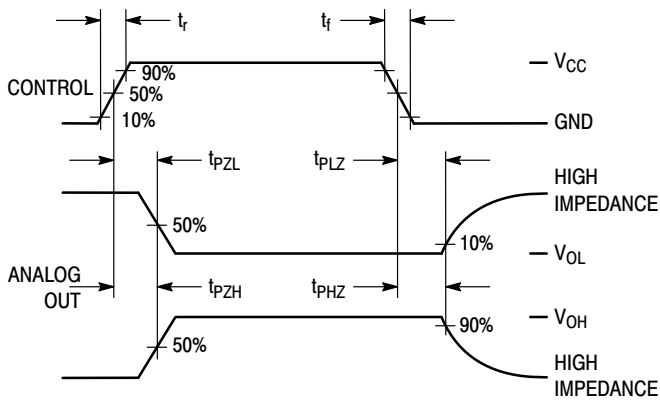


**Figure 18. Propagation Delays, Analog In to Analog Out**

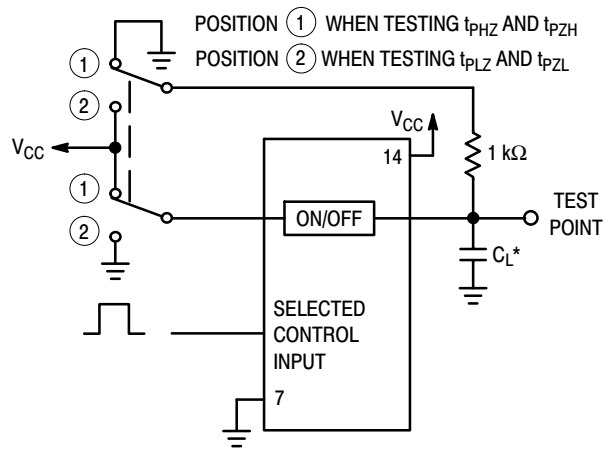


\*Includes all probe and jig capacitance.

**Figure 13. Propagation Delay Test Set-Up**

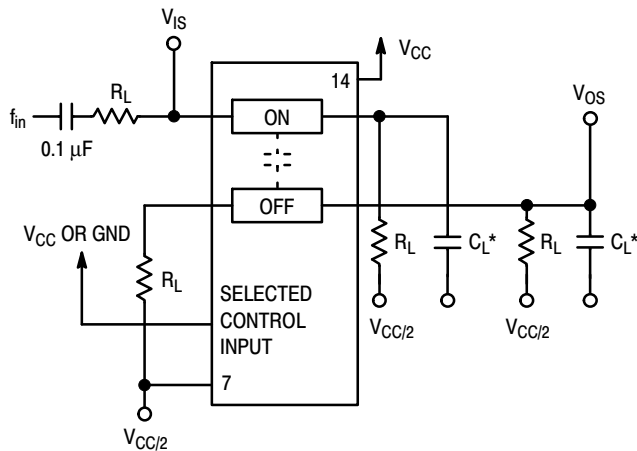


**Figure 14. Propagation Delay, ON/OFF Control to Analog Out**



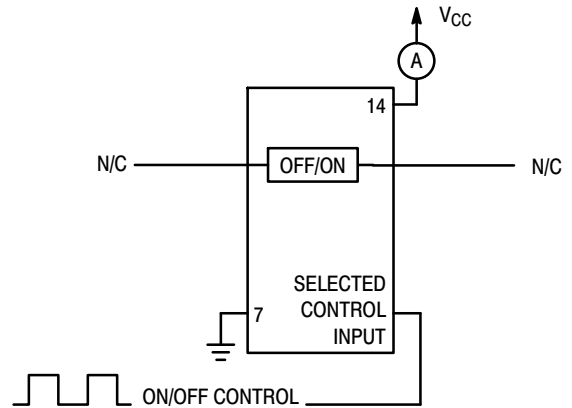
\*Includes all probe and jig capacitance.

**Figure 15. Propagation Delay Test Set-Up**

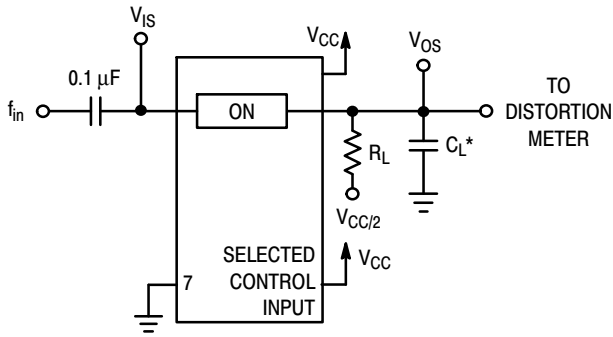


\*Includes all probe and jig capacitance.

**Figure 16. Crosstalk Between Any Two Switches, Test Set-Up**



**Figure 17. Power Dissipation Capacitance Test Set-Up**



\*Includes all probe and jig capacitance.

Figure 20. Total Harmonic Distortion, Test Set-Up

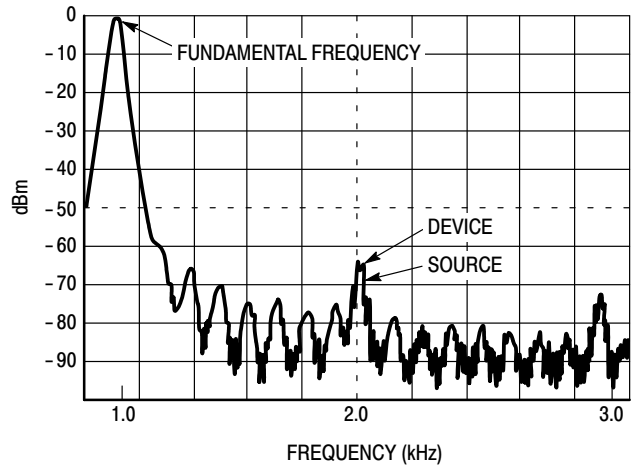


Figure 19. Plot, Harmonic Distortion

**APPLICATION INFORMATION**

The ON/OFF Control pins should be at  $V_{CC}$  or GND logic levels,  $V_{CC}$  being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked-up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and GND. The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below GND. In

the example below, the difference between  $V_{CC}$  and GND is twelve volts. Therefore, using the configuration in Figure 21, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above  $V_{CC}$  and/or below GND are anticipated on the analog channels, external diodes ( $D_x$ ) are recommended as shown in Figure 22. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the  $D_x$  diodes with Mosorbs (high current surge protectors). Mosorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear out mechanism.

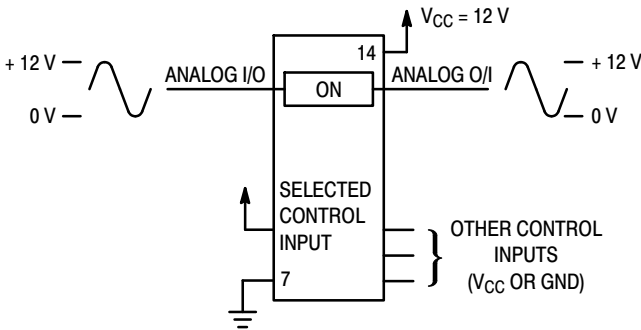


Figure 21. 12 V Application

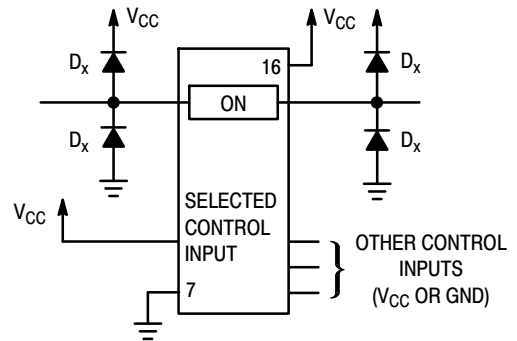


Figure 22. Transient Suppressor Application

# MC74VHC4066

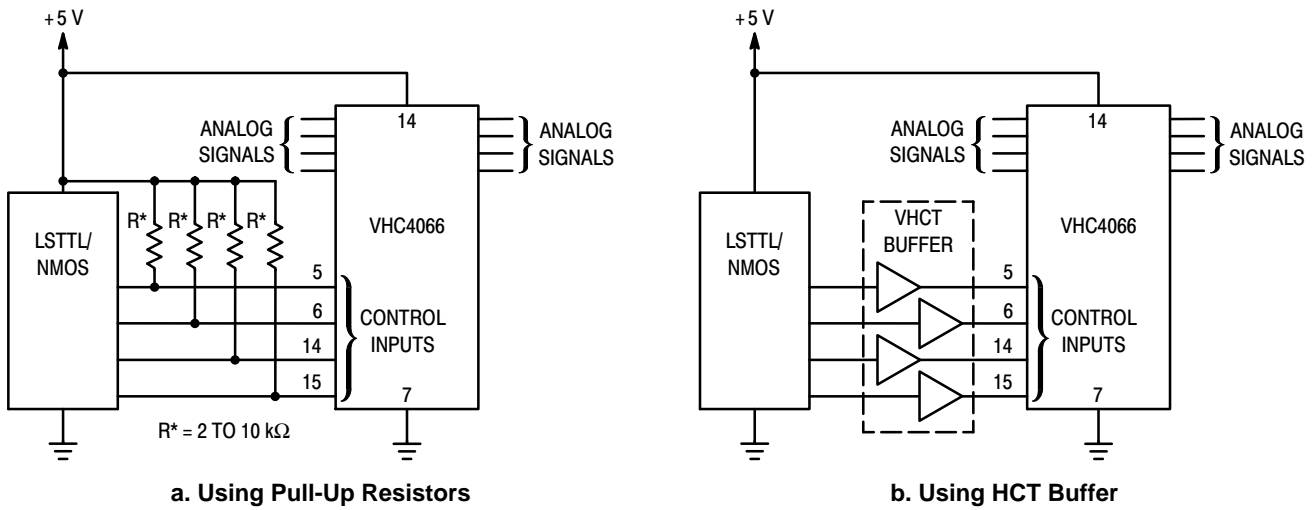


Figure 23. LSTTL/NMOS to HCMOS Interface

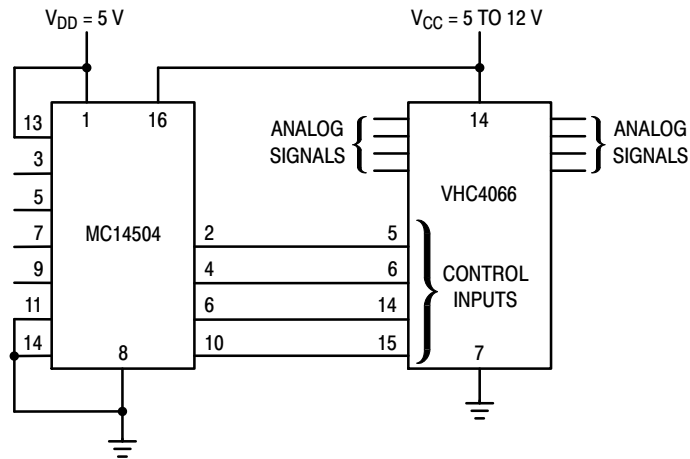


Figure 24. TTL/NMOS-to-CMOS Level Converter Analog Signal Peak-to-Peak Greater than 5 V (Also see VHC4316)

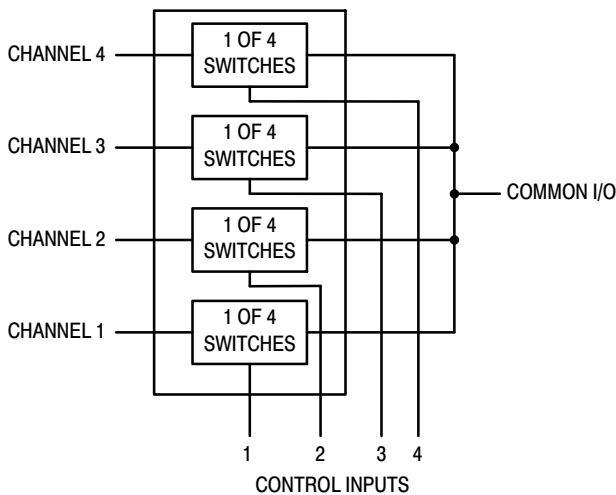


Figure 25. 4-Input Multiplexer

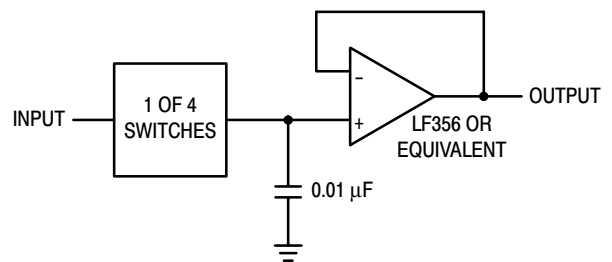


Figure 26. Sample/Hold Amplifier

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

|                  |             |  |
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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

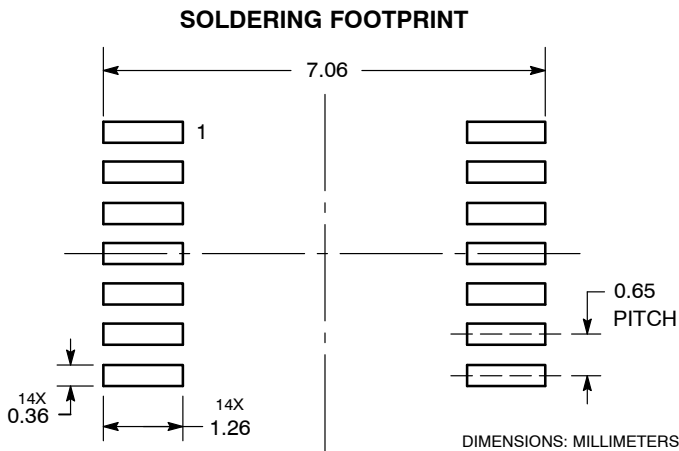
**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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