

Silicon Carbide (SiC) MOSFET – 40 mohm, 1200 V, M1, D2PAK-7

NTBG040N120SC1

Features

- Typ. $R_{DS(on)} = 40\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_{G(tot)} = 106\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss} = 139\text{ pF}$)
- 100% Avalanche Tested
- $T_J = 175^\circ\text{C}$
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb-Free 2LI (on second level interconnection)

Typical Applications

- UPS
- DC-DC Converter
- Boost Inverter

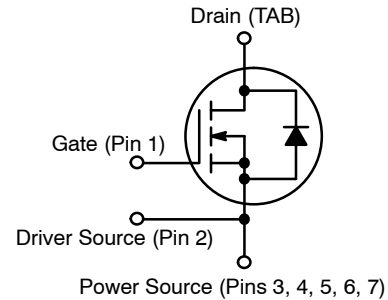
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	1200	V	
Gate-to-Source Voltage		V_{GS}	+25/-15	V	
Recommended Operation Values of Gate-Source Voltage		$T_C < 175^\circ\text{C}$ V_{GSop}	+20/-5	V	
Continuous Drain Current (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	I_D	60	A
			P_D	357	W
Continuous Drain Current (Note 1)	Steady State	$T_C = 100^\circ\text{C}$	I_D	43	A
			P_D	178	W
Pulsed Drain Current (Note 2)		$T_A = 25^\circ\text{C}$	I_{DM}	240	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	36	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 34\text{ A}_{pk}$, $L = 1\text{ mH}$) (Note 3)		E_{AS}	578	mJ	
Maximum Lead Temperature for Soldering, 1/8" from Case for 10 Seconds		T_L	300	$^\circ\text{C}$	

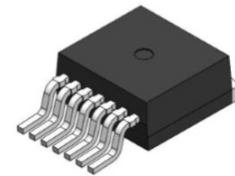
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Repetitive rating, limited by max junction temperature.
3. E_{AS} of 578 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 1\text{ mH}$, $I_{AS} = 34\text{ A}$, $V_{DD} = 120\text{ V}$, $V_{GS} = 18\text{ V}$.

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
1200 V	56 m Ω @ 20 V	60 A

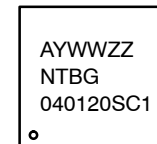


N-CHANNEL MOSFET



D2PAK-7L
CASE 418BJ

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Lot Traceability
- NTBG040120SC1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTBG040N120SC1	D2PAK-7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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Table 1. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-to-Case (Note 1)	$R_{\theta JC}$	0.42	$^{\circ}C/W$
Thermal Resistance Junction-to-Ambient (Note 1)	$R_{\theta JA}$	40	$^{\circ}C/W$

Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 V, I_D = 1 mA$	1200			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 1 mA$, refer to $25^{\circ}C$		0.45		$V/^{\circ}C$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0 V,$ $V_{DS} = 1200 V$	$T_J = 25^{\circ}C$		100	μA
			$T_J = 175^{\circ}C$		1	mA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = +25/-15 V, V_{DS} = 0 V$			± 1	μA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 10 mA$	1.8	3	4.3	V
Recommended Gate Voltage	V_{GOP}		-5		+20	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 20 V, I_D = 35 A, T_J = 25^{\circ}C$ $V_{GS} = 20 V, I_D = 35 A, T_J = 175^{\circ}C$		40	56	$m\Omega$
				71	100	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS} = 20 V, I_D = 35 A$		20		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0 V, f = 1 MHz,$ $V_{DS} = 800 V$		1789		μF
Output Capacitance	C_{OSS}			139		
Reverse Transfer Capacitance	C_{RSS}			12.5		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/20 V, V_{DS} = 600 V,$ $I_D = 47 A$		106		nC
Threshold Gate Charge	$Q_{G(TH)}$			18		
Gate-to-Source Charge	Q_{GS}			34		
Gate-to-Drain Charge	Q_{GD}			26		
Gate-Resistance	R_G	$f = 1 MHz$		2		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/20 V, V_{DS} = 800 V,$ $I_D = 47 A, R_G = 4.7 \Omega,$ Inductive Load		17	30	ns
Rise Time	t_r			20	36	
Turn-Off Delay Time	$t_{d(OFF)}$			30	48	
Fall Time	t_f			9	18	
Turn-On Switching Loss	E_{ON}			366		μJ
Turn-Off Switching Loss	E_{OFF}			200		
Total Switching Loss	E_{TOT}			566		

DRAIN-SOURCE DIODE CHARACTERISTICS

Continuous Drain-Source Diode Forward Current	I_{SD}	$V_{GS} = -5 V, T_J = 25^{\circ}C$			36	A
Pulsed Drain-Source Diode Forward Current (Note 2)	I_{SDM}	$V_{GS} = -5 V, T_J = 25^{\circ}C$			240	A
Forward Diode Voltage	V_{SD}	$V_{GS} = -5 V, I_{SD} = 17.5 A, T_J = 25^{\circ}C$		3.7		V

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Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise stated) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	$V_{GS} = -5/20\text{ V}$, $I_{SD} = 47\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$		24		ns
Reverse Recovery Charge	Q_{RR}			124.8		nC
Reverse Recovery Energy	E_{REC}			8.4		μJ
Peak Reverse Recovery Current	I_{RRM}			10.4		A
Charge Time	T_a			12.4		ns
Discharge Time	T_b			11.6		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

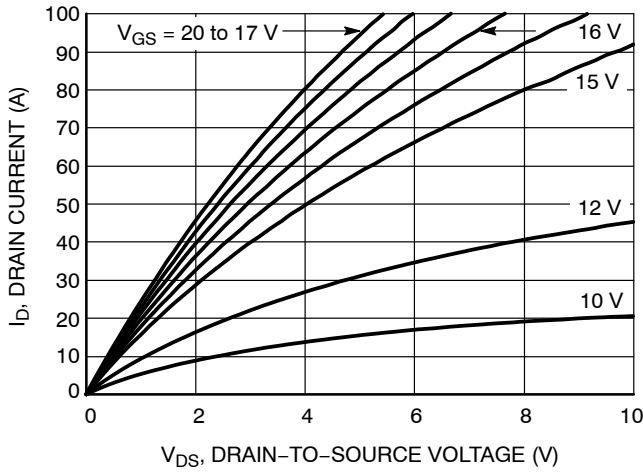


Figure 1. On-Region Characteristics

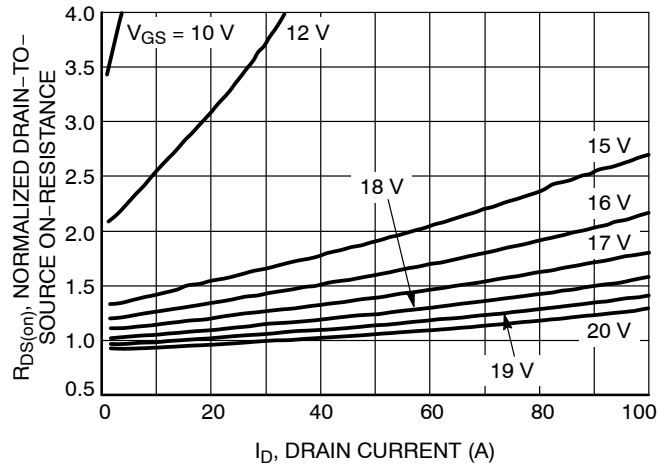


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

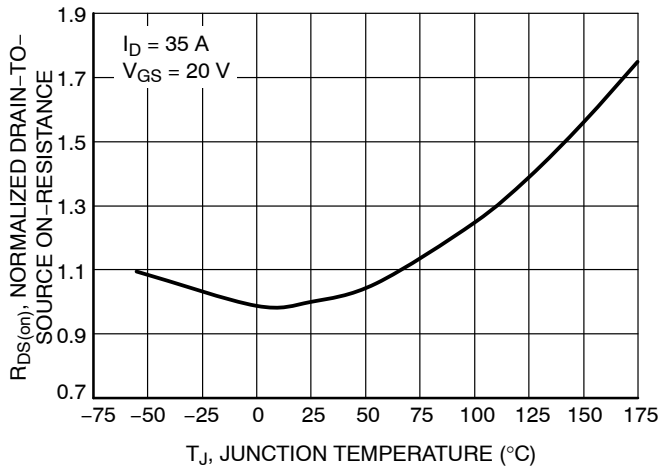


Figure 3. On-Resistance Variation with Temperature

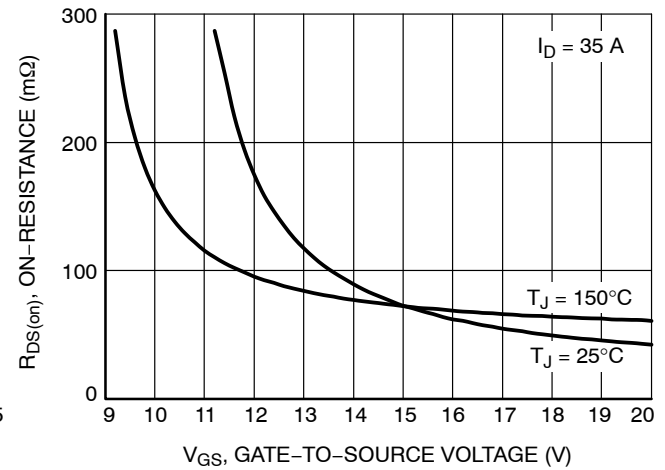


Figure 4. On-Resistance vs. Gate-to-Source Voltage

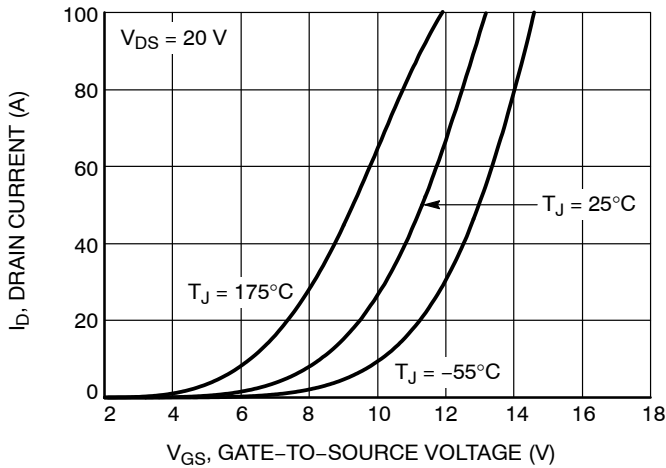


Figure 5. Transfer Characteristics

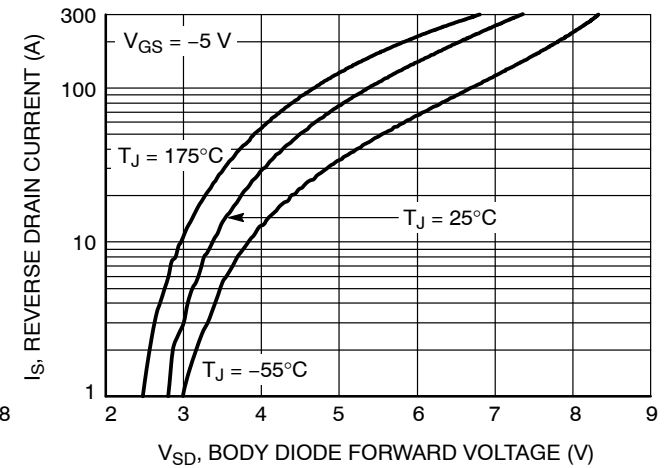


Figure 6. Diode Forward Voltage vs. Current

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TYPICAL CHARACTERISTICS (continued)

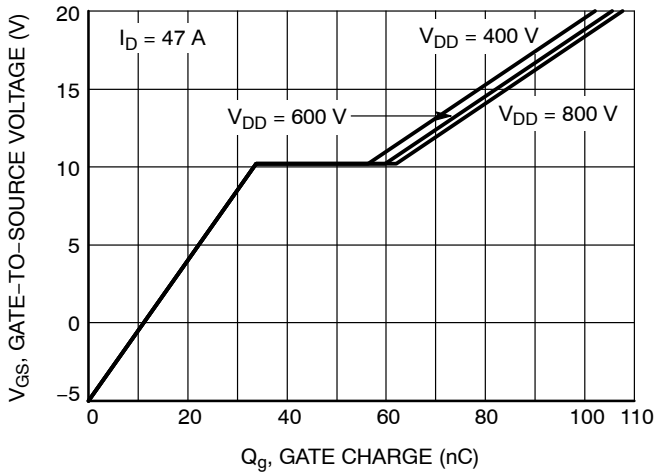


Figure 7. Gate-to-Source Voltage vs. Total Charge

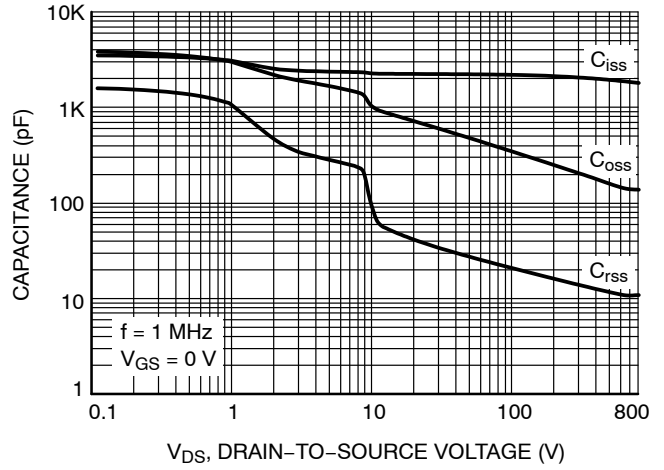


Figure 8. Capacitance vs. Drain-to-Source Voltage

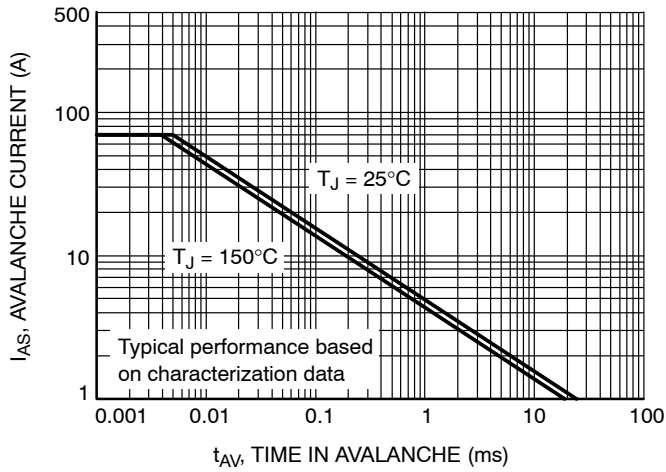


Figure 9. Unclamped Inductive Switching Capability

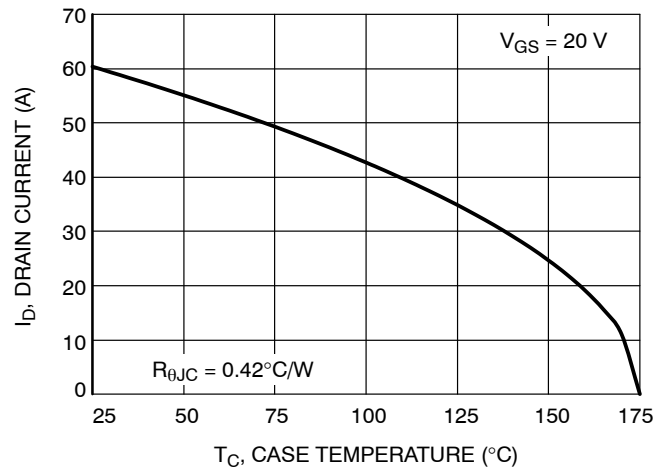


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

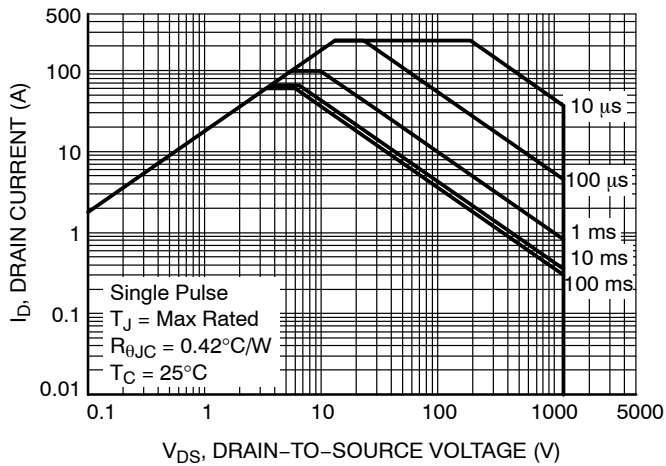


Figure 11. Safe Operating Area

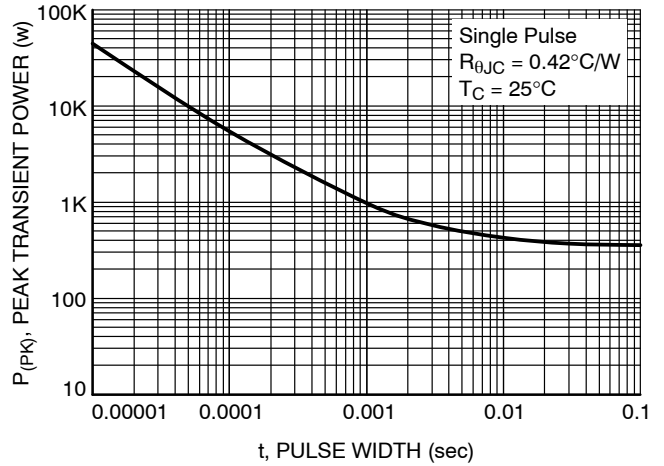


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (continued)

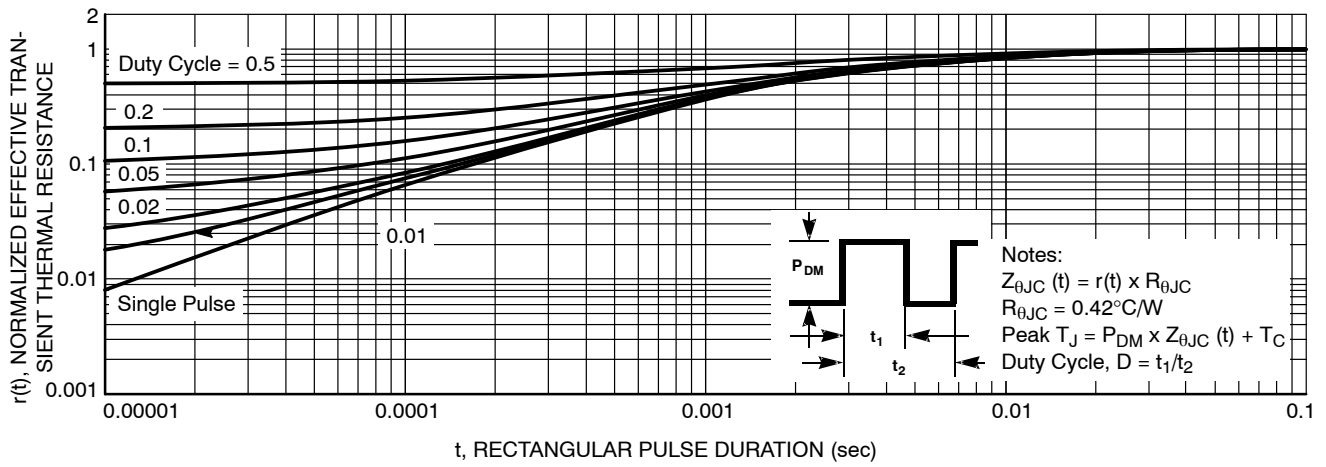


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

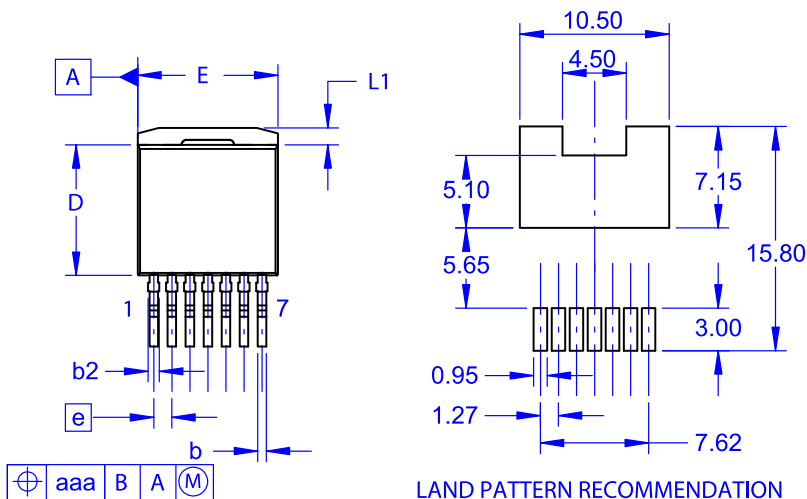
PACKAGE DIMENSIONS

ON Semiconductor®



D²PAK7 (TO-263-7L HV) CASE 418BJ ISSUE B

DATE 16 AUG 2019



LAND PATTERN RECOMMENDATION

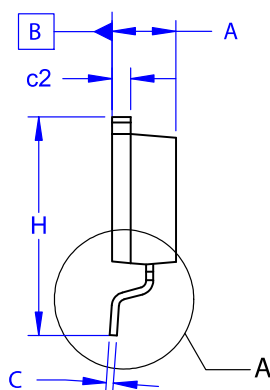
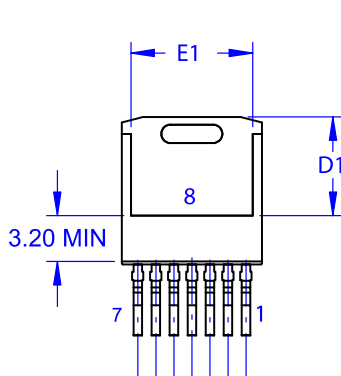
NOTES:

A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.

\triangle OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.

E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

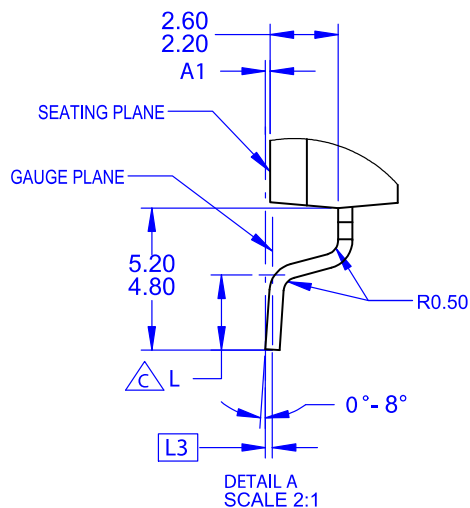


GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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