3 A Output Current, High Speed MOSFET Gate Driver Optocoupler

FOD3182

Description

The FOD3182 is a 3 A Output Current, High Speed MOSFET Gate Drive Optocoupler. It consists of a aluminium gallium arsenide (AlGaAs) light emitting diode optically coupled to a CMOS detector with PMOS and NMOS output power transistors integrated circuit power stage. It is ideally suited for high frequency driving of power MOSFETS used in Plasma Display Panels (PDPs), motor control inverter applications and high performance DC/DC converters.

The device is packaged in an 8−pin dual in−line housing compatible with 260°C reflow processes for lead free solder compliance.

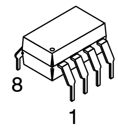
Features

- High Noise Immunity Characterized by 50 kV/μs (Typ.) Common Mode Rejection @ V_{CM} = 2,000 V
- Guaranteed Operating Temperature Range of −40°C to +100°C
- 3 A Peak Output Current
- Fast Switching Speed
  - 210 ns Max. Propagation Delay
  - 65 ns Max. Pulse Width Distortion
- Fast Output Rise/Fall Time
- Offers Lower Dynamic Power Dissipation
- 250 kHz Maximum Switching Speed
- Wide V_{DD} operating Range: 10 V to 30 V
- Use of P−Channel MOSFETs at Output Stage Enables Output Voltage Swing Close to the Supply Rail (Rail−to−Rail Output)
- 5000 Vrms, 1 Minute Isolation
- Under Voltage Lockout Protection (UVLO) with Hysteresis – Optimized for Driving MOSFETs
- Minimum Creepage Distance of 8.0 mm
- Minimum Clearance Distance of 10 mm to 16 mm (Option TV or TSV)
- Minimum Insulation Thickness of 0.5 mm
- UL and VDE*
- 1,414 Peak Working Insulation Voltage (V_{IORM})

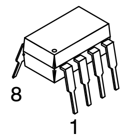
*Requires “V” Ordering Option

Applications

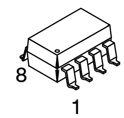
- Plasma Display Panel
- High Performance DC/DC Convertor
- High Performance Switch Mode Power Supply
- High Performance Uninterruptible Power Supply
- Isolated Power MOSFET Gate Drive



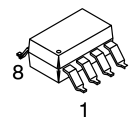
PDIP8 6.6x3.81, 2.54P
CASE 646BW



PDIP8 9.655x6.61, 2.54P
CASE 646CQ

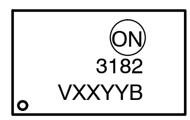


PDIP8 GW
CASE 709AC



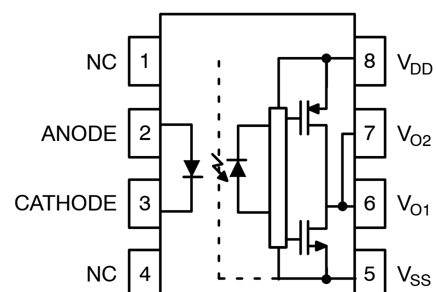
PDIP8 GW
CASE 709AD

MARKING DIAGRAM



3182 = Device Number
V = VDE Mark (Note: Only appears on parts ordered with DIN EN/IEC 60747−5−2 option − See ordering table)
XX = Two Digit Year Code, e.g., “11”
YY = Digit Work Week Ranging from “01” to “53”
B = Assembly Package Code

FUNCTIONAL BLOCK DIAGRAM



NOTE: A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

TRUTH TABLE

LED	$V_{DD} – V_{SS}$ "Positive Going" (Turn−on)	$V_{DD} – V_{SS}$ "Negative Going" (Turn−off)	V_O
Off	0 V to 30 V	0 V to 30 V	Low
On	0 V to 7.4 V	0 V to 7 V	Low
On	7.4 V to 9 V	7 V to 8.5 V	Transition
On	9 V to 30 V	8.5 V to 30 V	High

PIN DEFINITIONS

Pin No.	Name	Description
1	NC	Not Connected
2	Anode	LED Anode
3	Cathode	LED Cathode
4	NC	Not Connected
5	V_{SS}	Negative Supply Voltage
6	V_{O2}	Output Voltage 2 (internally connected to V_{O1})
7	V_{O1}	Output Voltage 1
8	V_{DD}	Positive Supply Voltage

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC 60747−5−2. This optocoupler is suitable for "safe electrical insulation" only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 For Rated Mains Voltage < 150 Vrms	–	I–IV	–	
	For Rated Mains Voltage < 300 Vrms	–	I–IV	–	
	For Rated Mains Voltage < 450 Vrms	–	I–III	–	
	For Rated Mains Voltage < 600 Vrms	–	I–III	–	
	For Rated Mains Voltage < 1000 Vrms (Option T, TS)	–	I–III	–	
	Climatic Classification	–	40/100/21	–	
	Pollution Degree (DIN VDE 0110/1.89)	–	2	–	
CTI	Comparative Tracking Index	175	–	–	
V_{PR}	Input to Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with tm = 1 second, Partial Discharge < 5 pC	2651	–	–	
	Input to Output Test Voltage, Method a, V_{IORM} x 1.5 = V_{PR}, Type and Sample Test with tm = 60 seconds, Partial Discharge < 5 pC	2121	–	–	
V_{IORM}	Max Working Insulation Voltage	1,414	–	–	V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	6000	–	–	V_{peak}
	External Creepage	8	–	–	mm
	External Clearance	7.4	–	–	mm
	External Clearance (for Option T or TS – 0.4" Lead Spacing)	10.16	–	–	mm
	Insulation Thickness	0.5	–	–	mm
T_{Case}	Safety Limit Values – Maximum Values Allowed in the Event of a Failure Case Temperature	150	–	–	°C
$I_{S,INPUT}$	Input Current	25	–	–	mA
$P_{S,OUTPUT}$	Output Power (Duty Factor ≤ 2.7%)	250	–	–	mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9	–	–	Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +100	°C
T_J	Junction Temperature	−40 to +125	°C
T_{SOL}	Lead Solder Temperature – Wave Solder (Refer to Reflow Temperature Profile, page 15)	260 for 10 seconds	°C
$I_{F(AVG)}$	Average Input Current (Note 1)	25	mA
$I_{F(tr, tf)}$	LED Current Minimum Rate of Rise/Fall	250	ns
V_R	Reverse Input Voltage	5	V
$I_{OH(PEAK)}$	“High” Peak Output Current (Note 2)	3	A
$I_{OL(PEAK)}$	“Low” Peak Output Current (Note 2)	3	A
$V_{DD} - V_{SS}$	Supply Voltage	−0.5 to 35	V
$V_{O(PEAK)}$	Output Voltage	0 to V_{DD}	V
P_O	Output Power Dissipation (Note 3)	250	mW
P_D	Total Power Dissipation (Note 4)	295	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Derate linearly above +79°C free air temperature at a rate of 0.37mA/°C.
2. Maximum pulse width = 10 μs, maximum duty cycle = 11%.
3. Derate linearly above +79°C, free air temperature at the rate of 5.73 mW/°C.
4. No derating required across operating temperature range.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD} - V_{SS}$	Power Supply	10 to 30	V
$I_{F(ON)}$	Input Current (ON)	10 to 16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	−3.0 to 0.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL−OPTICAL CHARACTERISTICS (DC) (Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = 0 V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OH}	High Level Output Current	V_{OH} = (V_{DD} − V_{SS} − 1 V)	0.5	0.9	–	A
		V_{OH} = (V_{DD} − V_{SS} − 6 V)	2.5	–	–	
I_{OL}	Low Level Output Current	V_{OL} = (V_{DD} − V_{SS} + 1 V)	0.5	1	–	A
		V_{OL} = (V_{DD} − V_{SS} + 6 V)	2.5	–	–	
V_{OH}	High Level Output Voltage (Note 5, 6)	I_O = −100 mA	V_{DD} − 0.5	–	–	V
V_{OL}	Low Level Output Voltage (Note 5, 6)	I_O = 100 mA	–	–	V_{SS} + 0.5	V
I_{DDH}	High Level Supply Current	Output Open, I_F = 10 to 16 mA	–	2.6	4.0	mA
I_{DDL}	Low Level Supply Current	Output Open, V_F = −3.0 to 0.8 V	–	2.5	4.0	mA
I_{FLH}	Threshold Input Current Low to High	I_O = 0 mA, V_O > 5 V	–	3.0	7.5	mA
V_{FHL}	Threshold Input Voltage High to Low	I_O = 0 mA, V_O < 5 V	0.8	–	–	V
V_F	Input Forward Voltage	I_F = 10 mA	1.1	1.43	1.8	V
$\Delta V_F / T_A$	Temperature Coefficient of Forward Voltage	I_F = 10 mA	–	−1.5	–	mV/°C
V_{UVLO+}	UVLO Threshold	V_O > 5V, I_F = 10 mA	7	8.3	9	V
V_{UVLO-}		V_O < 5V, I_F = 10 mA	6.5	7.7	8.5	V
$UVLO_{HYST}$	UVLO Hysteresis		–	0.6	–	V
BV_R	Input Reverse Breakdown Voltage	I_R = 10 μA	5	–	–	V
C_{IN}	Input Capacitance	f = 1 MHz, V_F = 0 V	–	25	–	pF

5. In this test, V_{OH} is measured with a dc load current of 100 mA. When driving capacitive load V_{OH} will approach V_{DD} as I_{OH} approaches zero amps.
6. Maximum pulse width = 1 ms, maximum duty cycle = 20%.

SWITCHING CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = 0 V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time to High Output Level (Note 7)	I_F = 10 mA, R_g = 10 Ω, f = 250 kHz, Duty Cycle = 50%, C_g = 10 nF	50	120	210	ns
t_{PHL}	Propagation Delay Time to Low Output Level (Note 7)		50	145	210	ns
P_{WD}	Pulse Width Distortion (Note 8)		–	35	65	ns
P_{DD} ($t_{PHL} - t_{PLH}$)	Propagation Delay Difference Between Any Two Parts (Note 9)		–90	–	90	ns
t_r	Rise Time	C_L = 10 nF, R_g = 10 Ω	–	38	–	ns
t_f	Fall Time		–	24	–	ns
$t_{UVLO\ ON}$	UVLO Turn On Delay		–	2.0	–	μs
$t_{UVLO\ OFF}$	UVLO Turn Off Delay		–	0.3	–	μs
$\lvert CM_H \rvert$	Output High Level Common Mode Transient Immunity (Note 10, 11)	T_A = +25°C, I_f = 7 mA to 16 mA, V_{CM} = 2 kV, V_{DD} = 30 V	35	50	–	kV/μs
$\lvert CM_L \rvert$	Output Low Level Common Mode Transient Immunity (Note 10, 12)	T_A = +25°C, V_f = 0 V, V_{CM} = 2 kV, V_{DD} = 30 V	35	50	–	kV/μs

7. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
8. PWD is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.
9. The difference between t_{PHL} and t_{PLH} between any two FOD3182 parts under same operating conditions, with equal loads.
10. Pin 1 and 4 need to be connected to LED common.
11. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse V_{CM} to assure that the output will remain in the high state (i.e. V_O > 15 V).
12. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e. V_O < 1.0 V).

INSULATION CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ*	Max	Unit
V_{ISO}	Withstand Isolation Voltage (Note 13, 14)	T_A = 25°C, R.H. < 50%, t = 1 minute, $I_{I-O} \leq$ 10 μA	5000	–	–	V_{rms}
R_{I-O}	Resistance (Input to Output) (Note 14)	V_{I-O} = 500 V	–	10^{11}	–	Ω
C_{I-O}	Capacitance (Input to Output)	Freq. = 1 MHz	–	1	–	pF

*Typical values at T_A = 25°C

13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 Vrms, 60 Hz for 1 second (leakage detection current limit I_{I-O} < 10 μA).
14. Device considered a two−terminal device: pins on input side shorted together and pins on output side shorted together.

TYPICAL PERFORMANCE CURVES

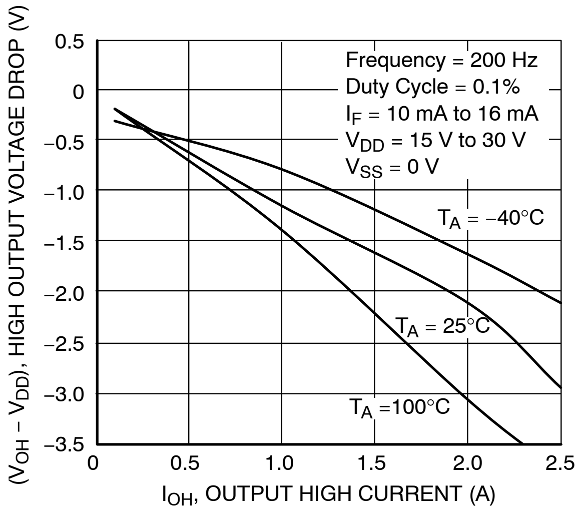


Figure 1. Output High Voltage Drop vs. Output High Current

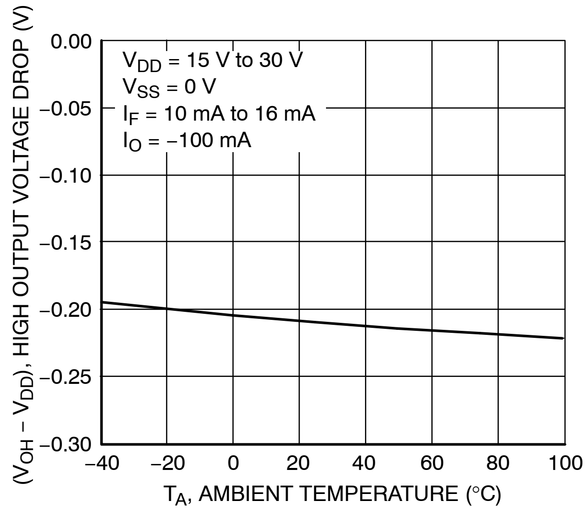


Figure 2. Output High Voltage Drop vs. Ambient Temperature

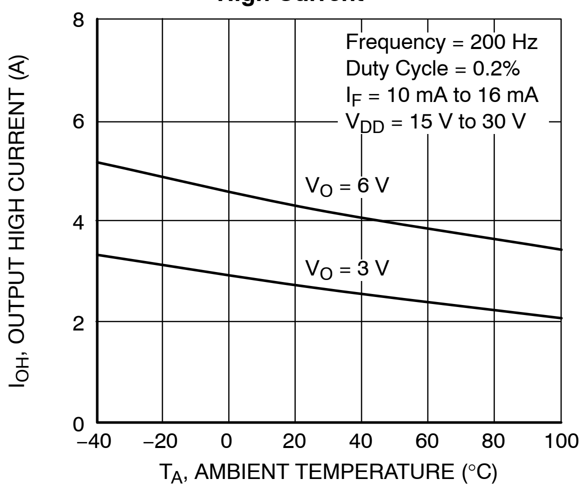


Figure 3. Output High Current vs. Ambient Temperature

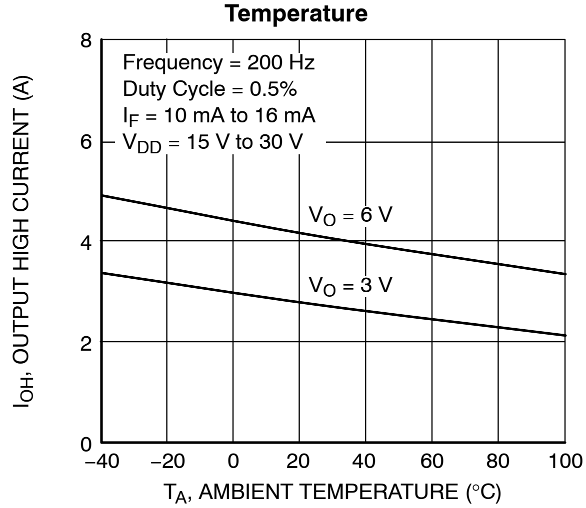


Figure 4. Output High Current vs. Ambient Temperature

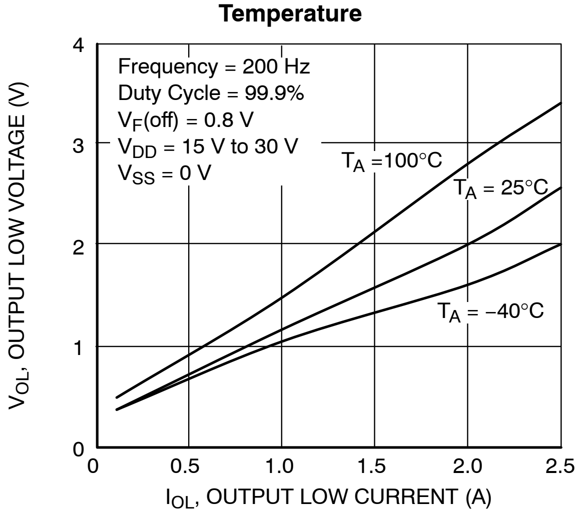


Figure 5. Output Low Voltage vs. Output Low Current

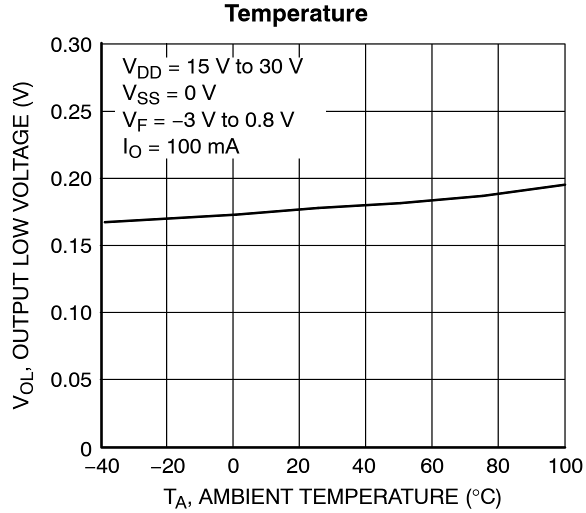


Figure 6. Output Low Voltage vs. Ambient Temperature

TYPICAL PERFORMANCE CURVES (Continued)

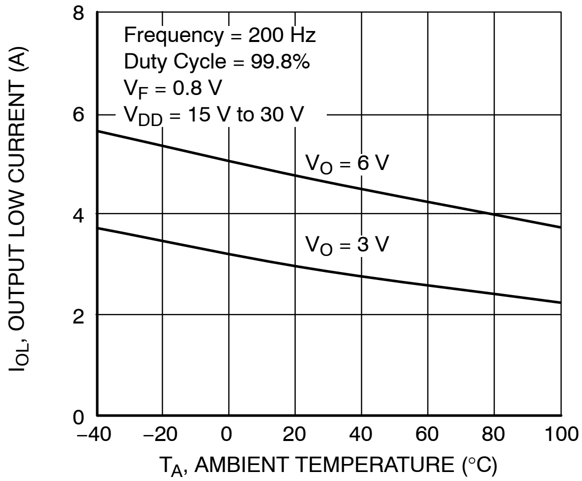


Figure 7. Output Low Current vs. Ambient Temperature

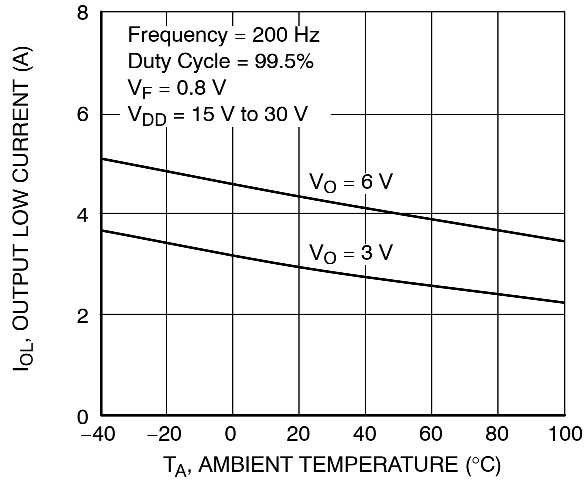


Figure 8. Output Low Current vs. Ambient Temperature

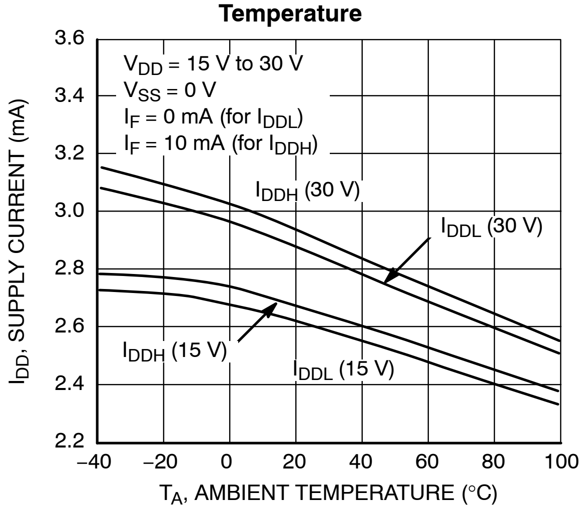


Figure 9. Supply Current vs. Ambient Temperature

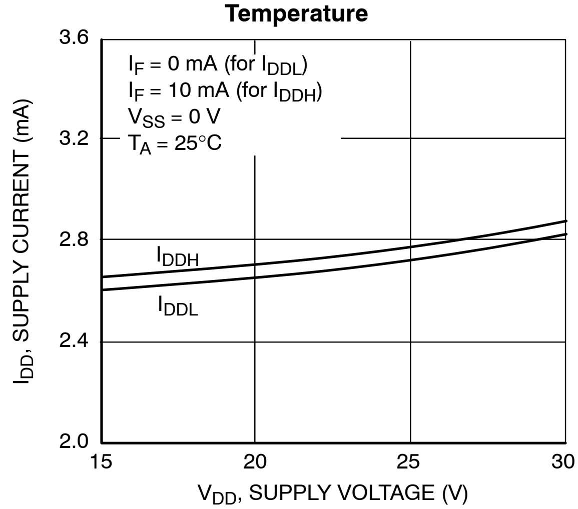


Figure 10. Supply Current vs. Supply Voltage

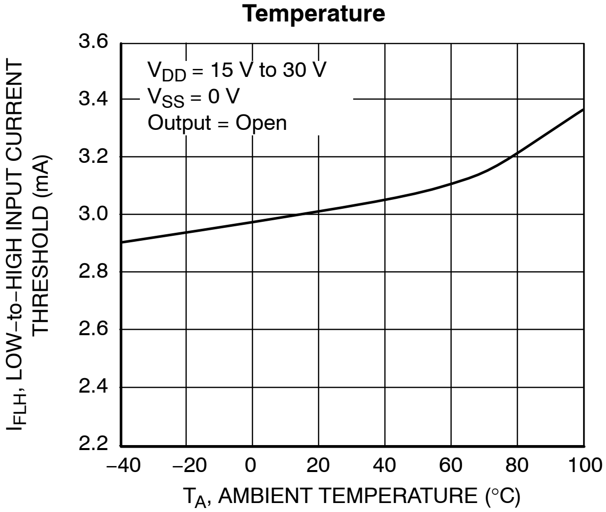


Figure 11. Low-to High Input Current Threshold vs. Ambient Temperature

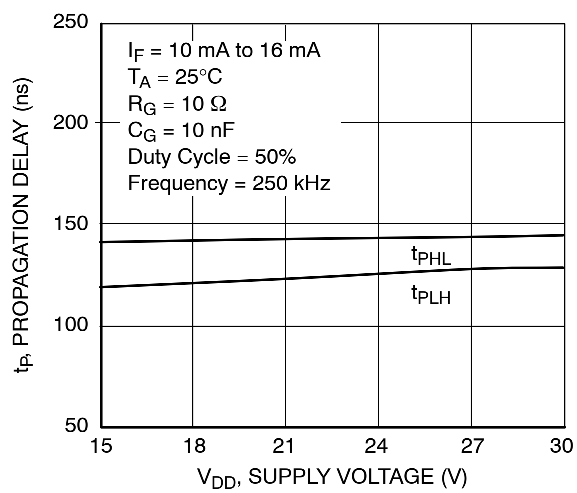


Figure 12. Propagation Delay vs. Supply Voltage

TYPICAL PERFORMANCE CURVES (Continued)

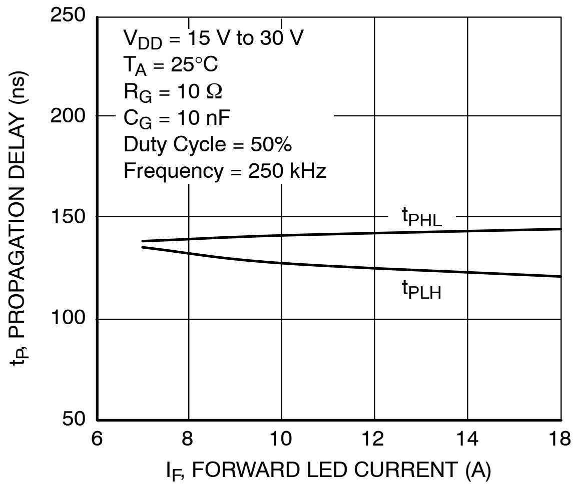


Figure 13. Propagation Delay vs. LED Forward Current

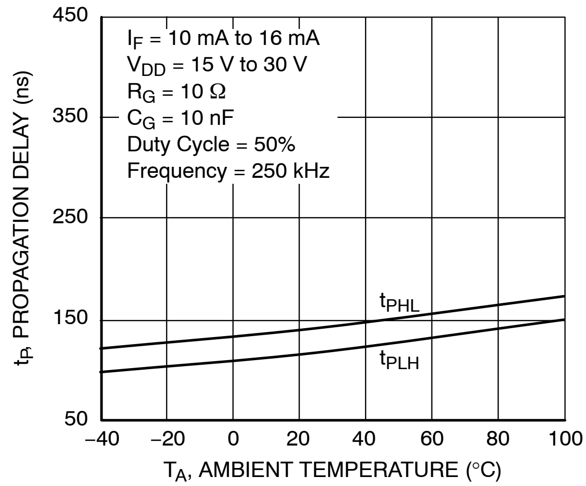


Figure 14. Propagation Delay vs. Ambient Temperature

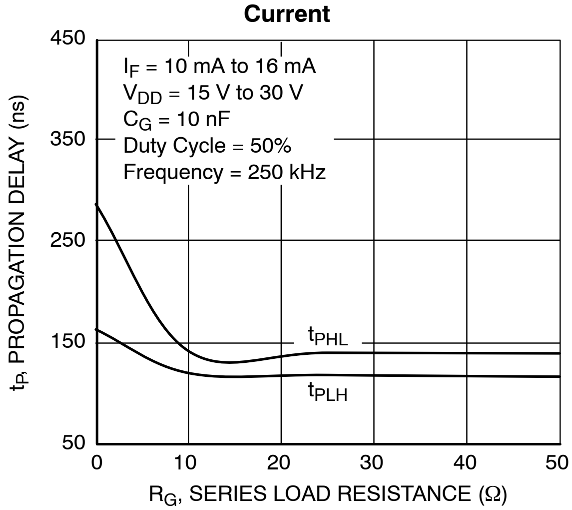


Figure 15. Propagation Delay vs. Series Load Resistance

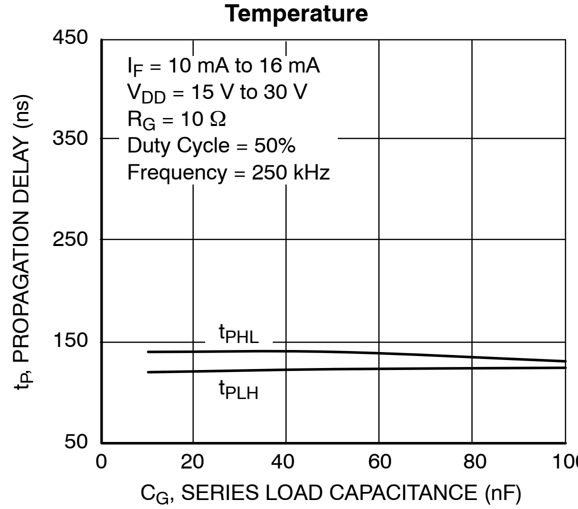


Figure 16. Propagation Delay vs. Series Load Capacitance

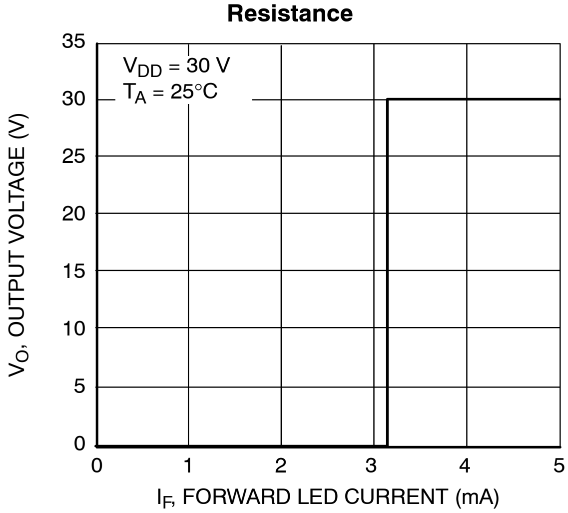


Figure 17. Transfer Characteristics

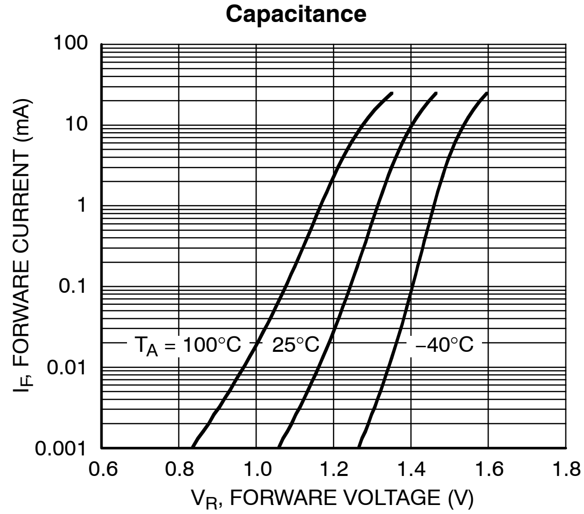


Figure 18. Input Forward Current vs. Forward Voltage

TYPICAL PERFORMANCE CURVES (Continued)

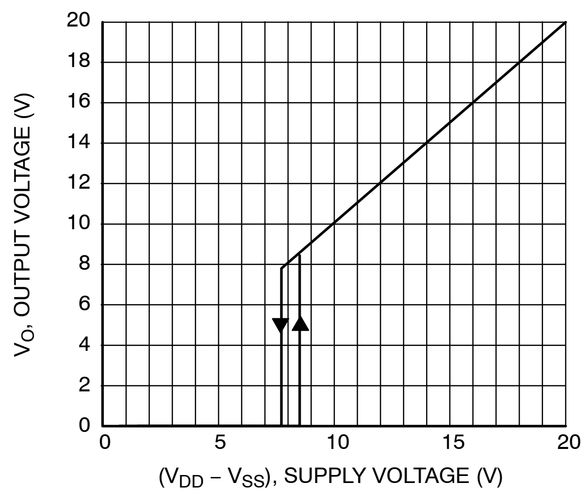


Figure 19. Under Voltage Lockout

TEST CIRCUIT

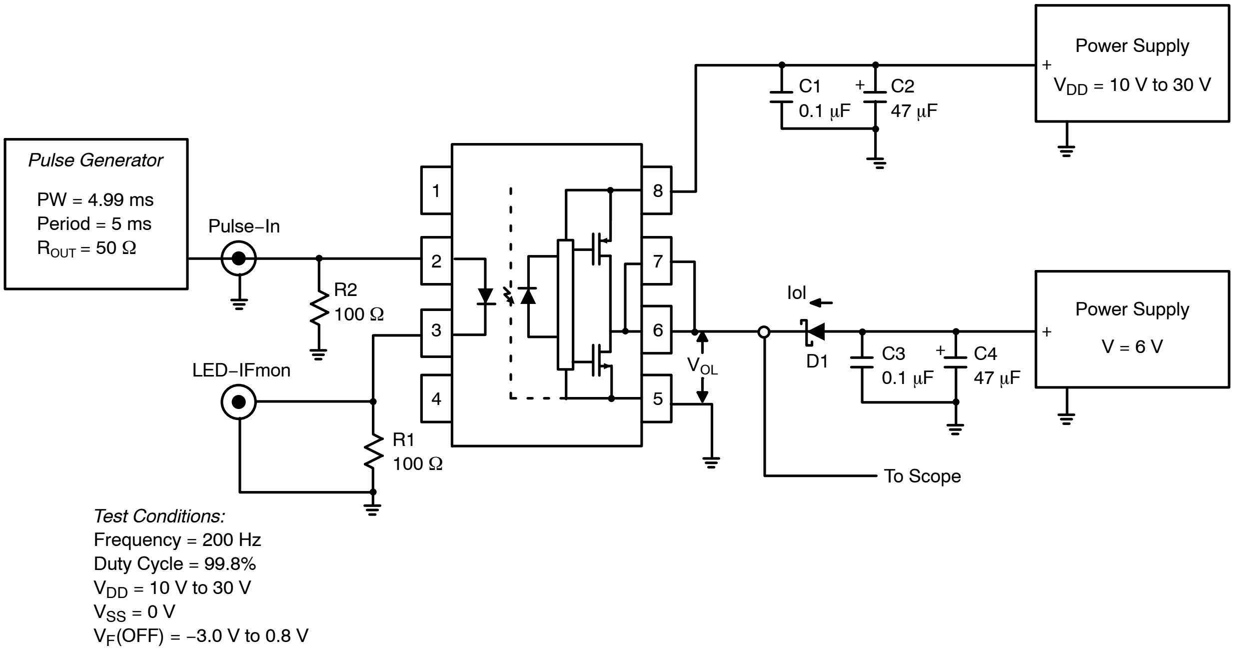


Figure 20. I_{OL} Test Circuit

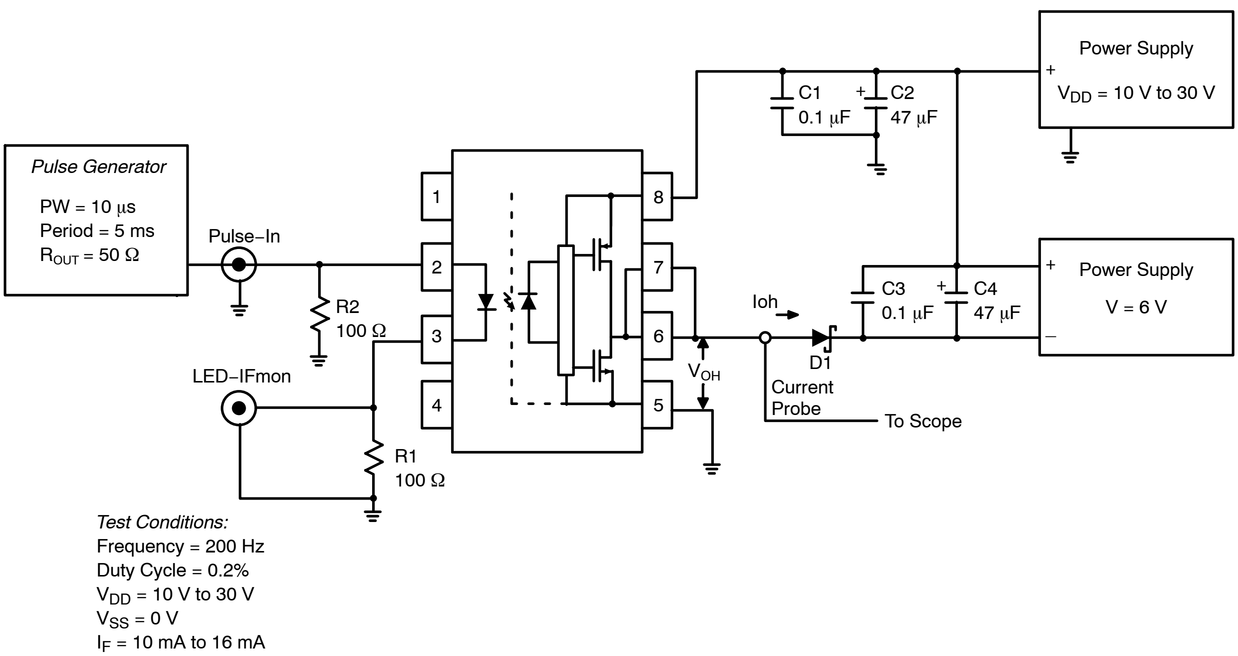


Figure 21. I_{OH} Test Circuit

TEST CIRCUIT (Continued)

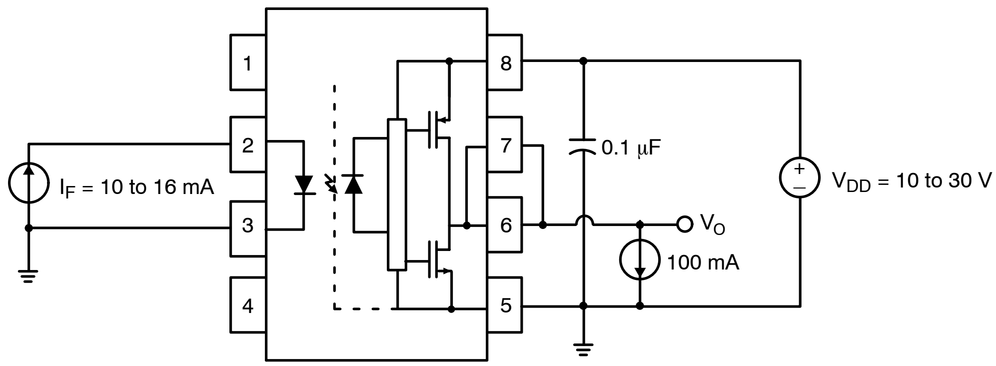


Figure 22. V_{OH} Test Circuit

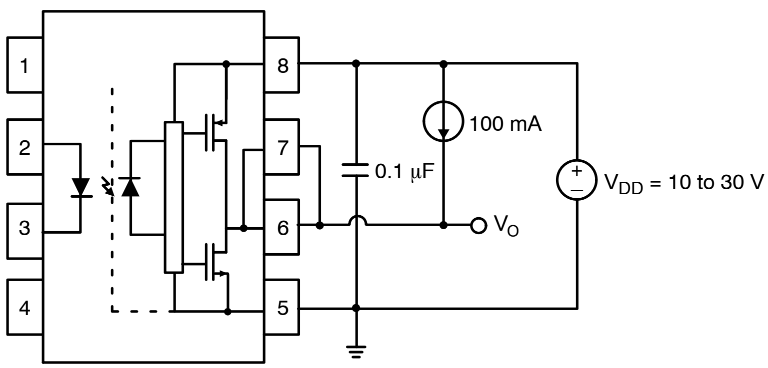


Figure 23. V_{OL} Test Circuit

TEST CIRCUIT (Continued)

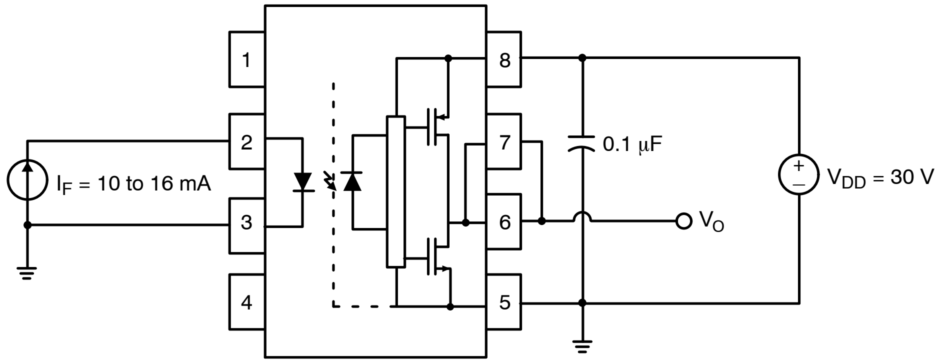


Figure 24. I_{DDH} Test Circuit

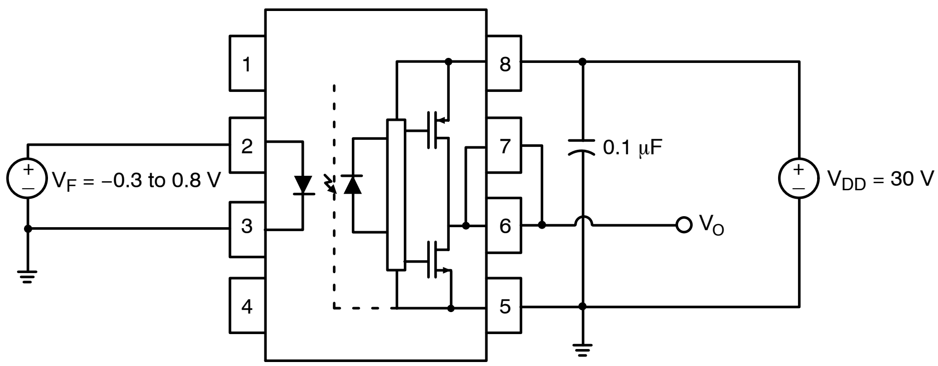


Figure 25. I_{DDL} Test Circuit

TEST CIRCUIT (Continued)

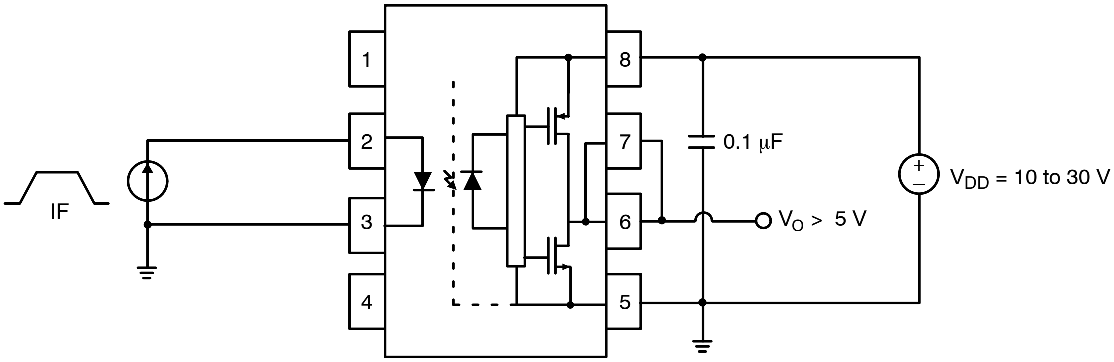


Figure 26. I_{FLH} Test Circuit

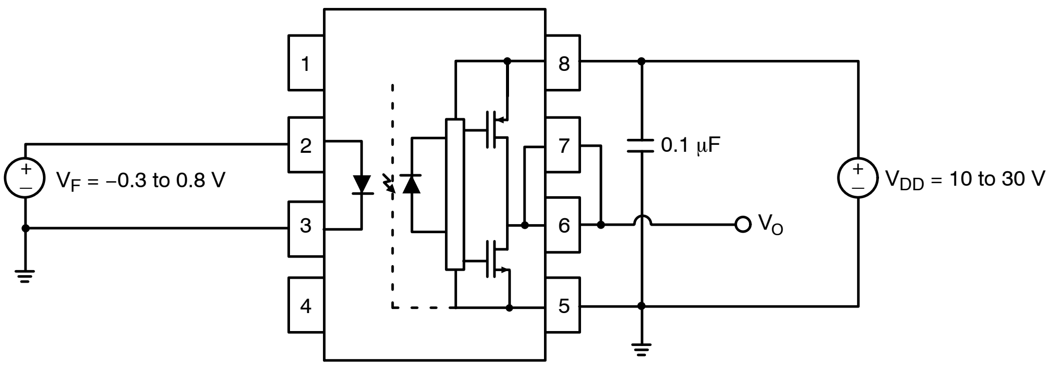


Figure 27. I_{FHL} Test Circuit

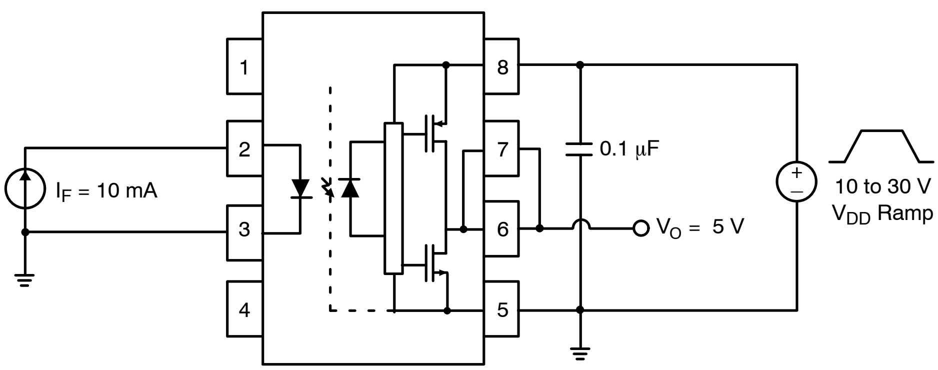


Figure 28. UVLO Test Circuit

TEST CIRCUIT (Continued)

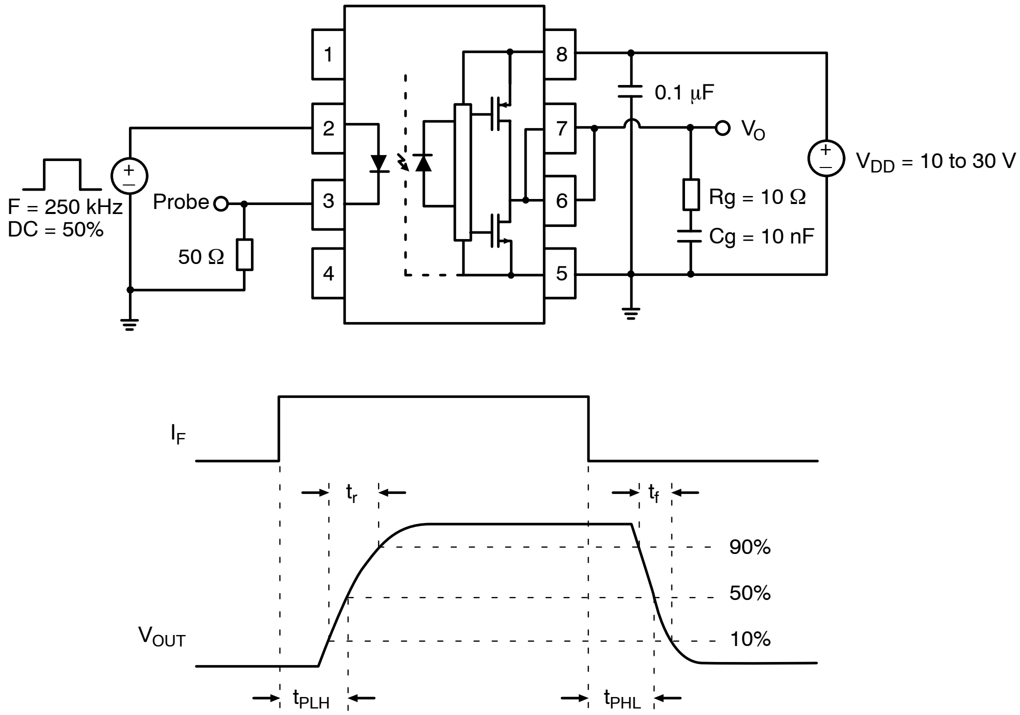


Figure 29. t_{PHL}, t_{PLH}, t_r and t_f Test Circuit and Waveforms

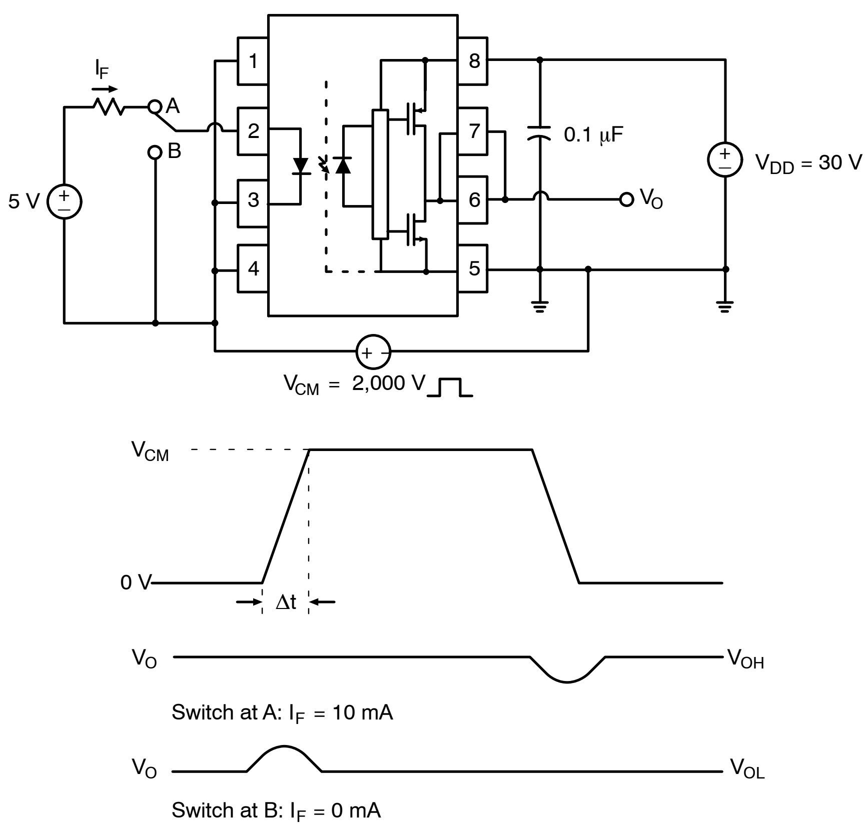


Figure 30. CMR Test Circuit and Waveforms

REFLOW PROFILE

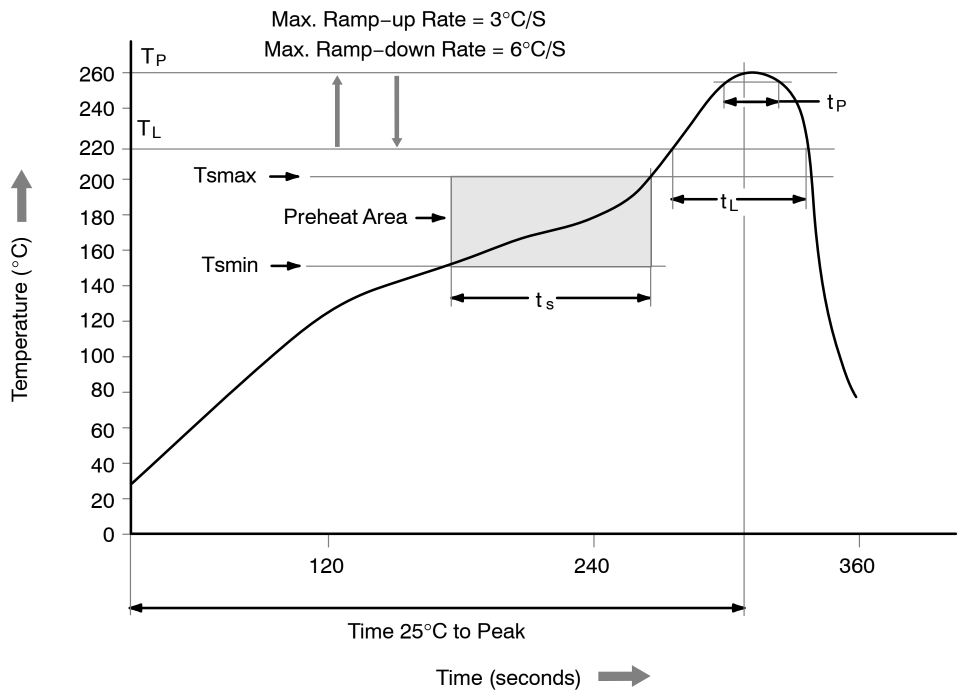


Figure 31. Reflow Profile

Table 1.

Profile Freature	Pb−Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60–120 seconds
Ramp−up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp−down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

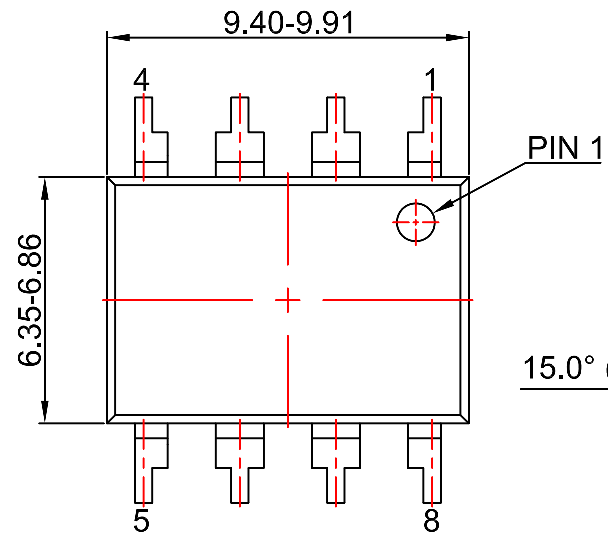
ORDERING INFORMATION

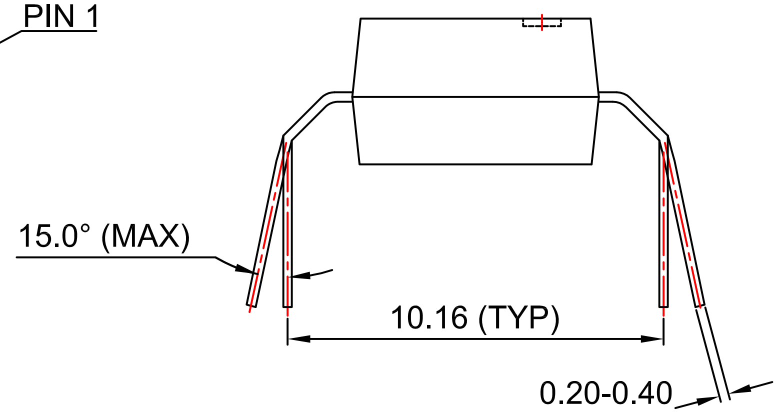
Part Number	Package	Shipping†
FOD3182	PDIP8 9.655x6.61, 2.54P DIP 8−Pin	50 Units / Tube
FOD3182S	PDIP8 GW SMT 8−Pin (Lead Bend)	50 Units / Tube
FOD3182SD	PDIP8 GW SMT 8−Pin (Lead Bend)	1,000 / Tape and Reel
FOD3182V	PDIP8 9.655x6.61, 2.54P DIP 8−Pin, IEC60747−5−2 option	50 Units / Tube
FOD3182SV	PDIP8 GW SMT 8−Pin (Lead Bend), DIN EN/IEC 60747−5−2 option	50 Units / Tube
FOD3182SDV	PDIP8 GW SMT 8−Pin (Lead Bend), DIN EN/IEC 60747−5−2 option	1,000 / Tape and Reel
FOD3182TV	PDIP8 6.6x3.81, 2.54P DIP 8−Pin, 0.4” Lead Spacing, DIN EN/IEC 60747−5−2 option	50 Units / Tube
FOD3182TSV	PDIP8 GW SMT 8−Pin, 0.4” Lead Spacing, DIN EN/IEC 60747−5−2 option	50 Units / Tube
FOD3182TSR2	PDIP8 GW SMT 8−Pin, 0.4” Lead Spacing	700 / Tape and Reel
FOD3182TSR2V	PDIP8 GW SMT 8−Pin, 0.4” Lead Spacing, DIN EN/IEC 60747−5−2 option	700 / Tape and Reel

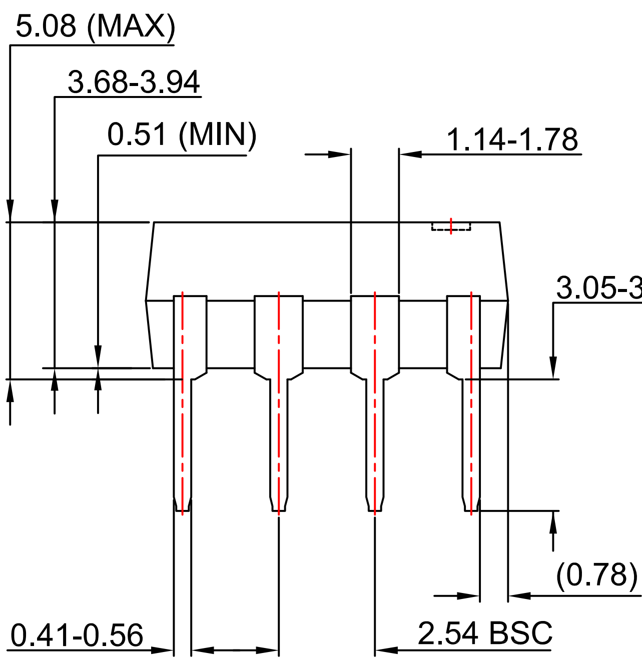
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

DATE 31 JUL 2016







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PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

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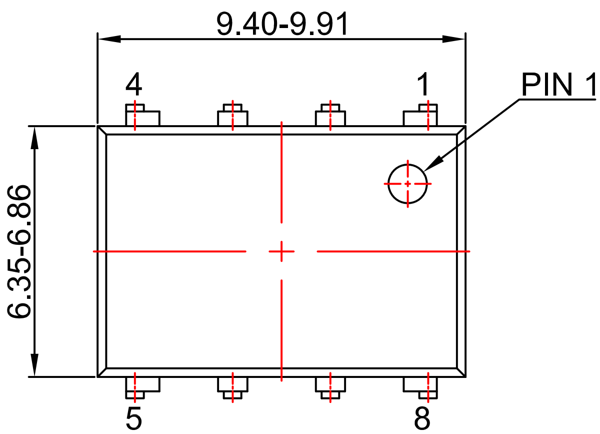

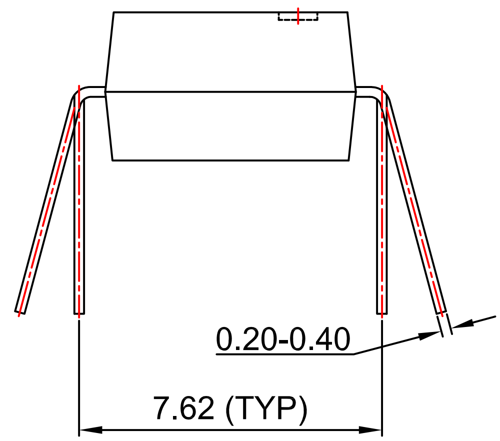

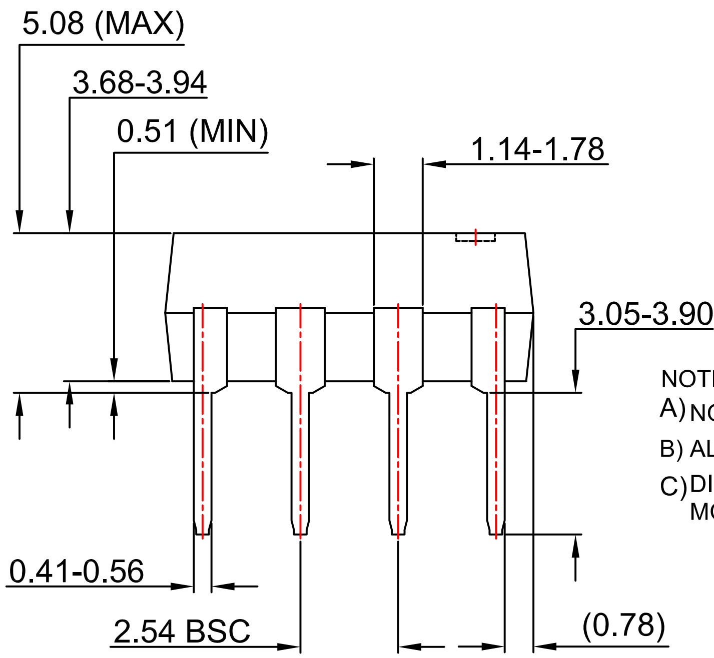

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PDIP8 GW
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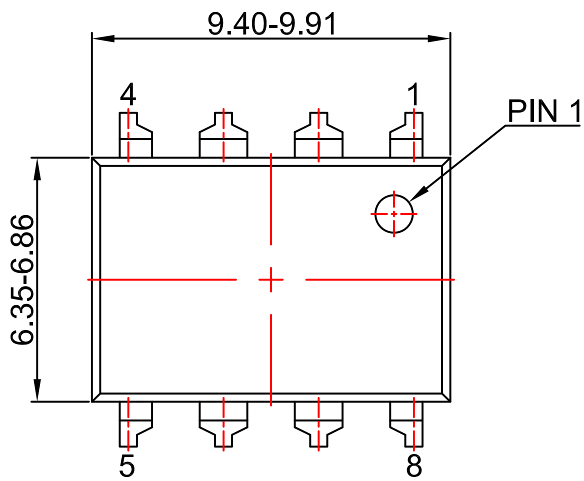
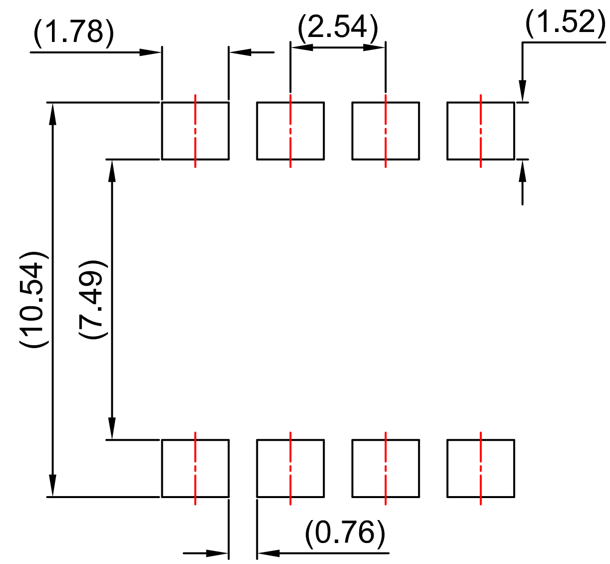
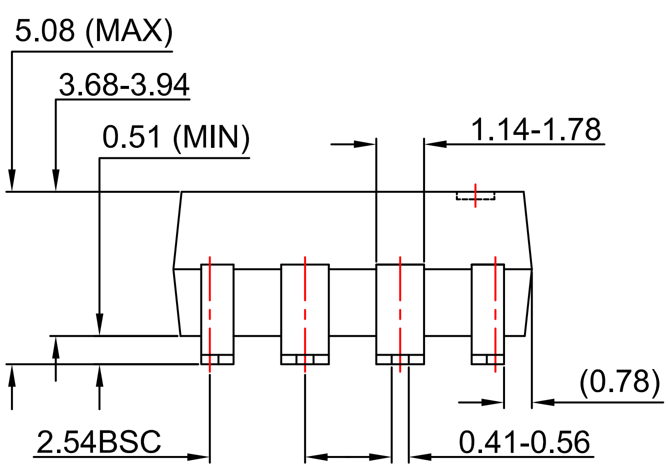
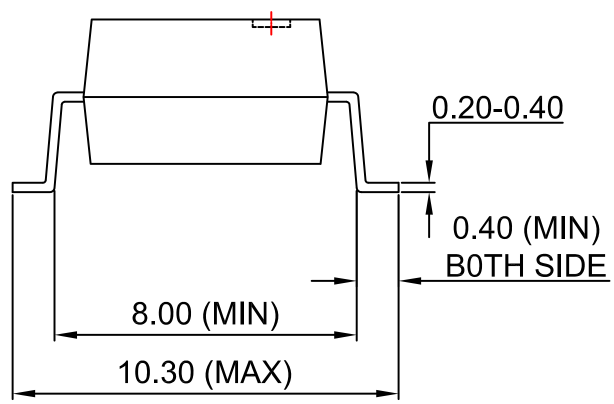




LAND PATTERN RECOMMENDATION





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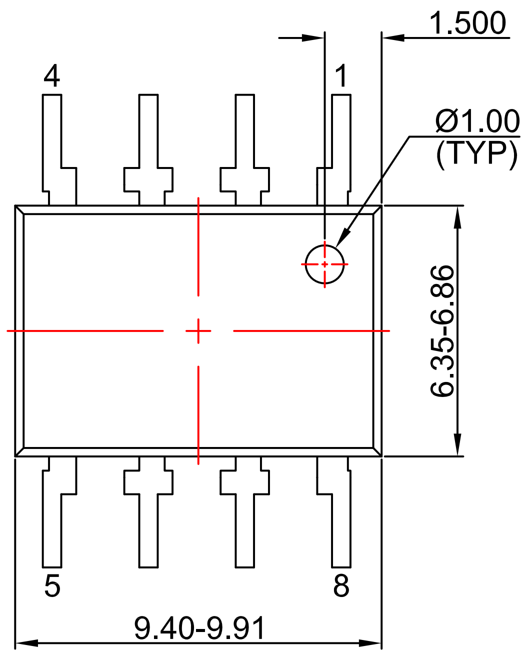

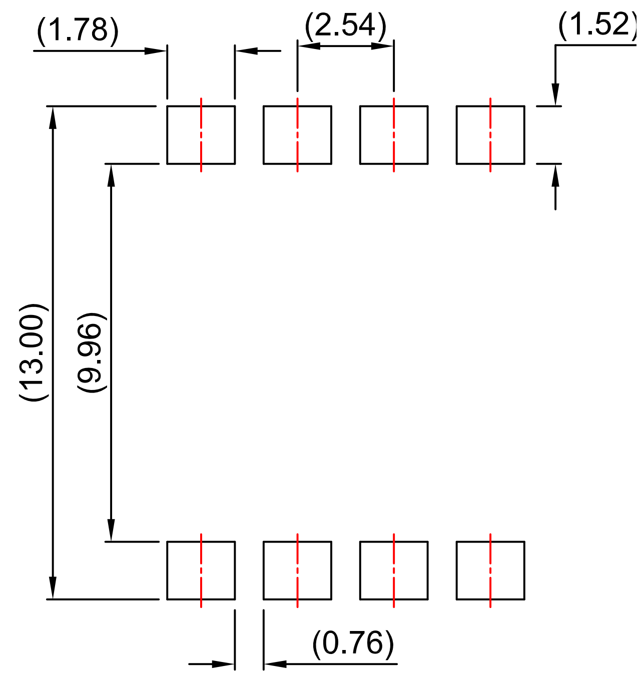

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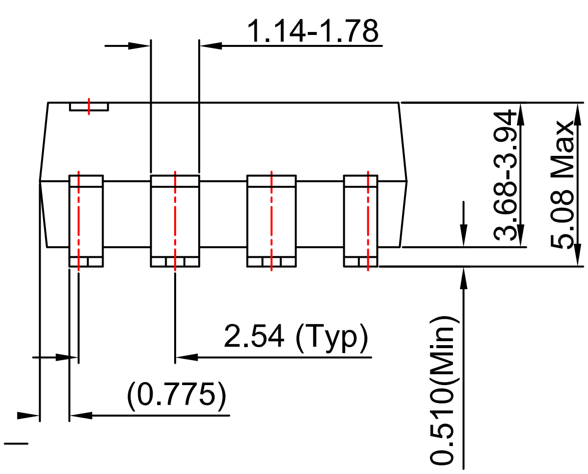

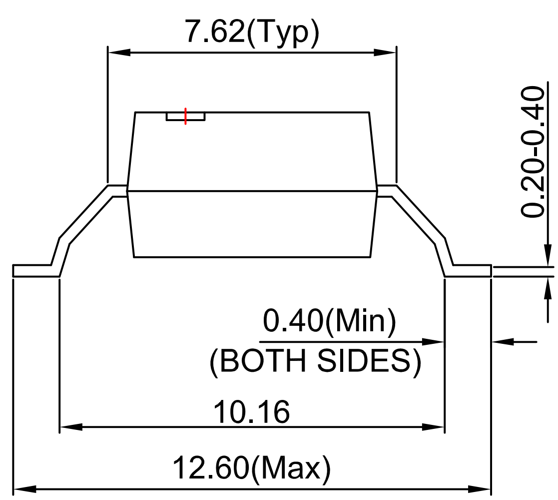

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