LDO Regulator - Watchdog, Wake Up and Reset
5.0 V, 250 mA

NCV8508C

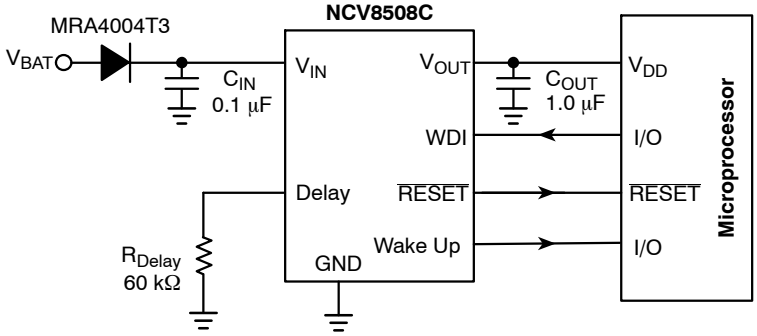
The NCV8508C is a precision micropower Low Dropout (LDO) voltage regulator. The part contains many of the required features for powering microprocessors. Its robustness makes it suitable for severe automotive environments. In addition, the NCV8508C is ideal for use in battery operated, microprocessor controlled equipment because of its low quiescent current.

Features

- Output Voltage Option: 5.0 V
- Output Voltage Accuracy: ±2%
- Output Current up to 250 mA
- Low Dropout Voltage
- Low Quiescent Current of 76 μA
- Micropower Compatible Control Functions:
  - Watchdog
  - RESET
  - Wake Up
- Protection Features:
  - Thermal Shutdown
  - Current Limitation
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications (for safety applications refer to Figure 26)

- Body and Chassis
- Instrument and Clusters
- Engine Control Unit



*C_{IN} required if regulator is located far from power supply filter. If extremely fast input voltage transients are expected then appropriate input filter must be used. The filter can be composed of several capacitors in parallel

Figure 1. Application Circuit

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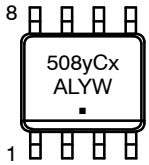
SOIC−8 EP
PD SUFFIX
CASE 751AC

MARKING DIAGRAMS

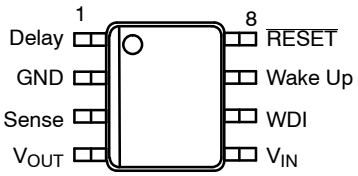


x	=	Voltage Option 5 – 5.0 V
y	=	Timing Option 1
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

PIN CONNECTIONS



SOIC−8 EP

PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	Delay	Delay Timing. Buffered reference voltage used to create timing current for $\overline{RESET}$ and Watchdog threshold frequency from R_{Delay}.
2	GND	Power Supply Ground.
3	Sense	Kelvin connection which allows remote sensing of the output voltage for improved regulation. Connect to V_{OUT} if remote sensing is not required.
4	V_{OUT}	Regulated Output Voltage.
5	V_{IN}	Positive Power Supply. Connect capacitor to ground.
6	WDI	CMOS compatible Watchdog Input. The watchdog function monitors the falling edge of the incoming signal.
7	Wake Up	Continuously generated signal that interrupts the microprocessor from sleep mode.
8	$\overline{RESET}$	CMOS compatible output lead $\overline{RESET}$ goes low whenever V_{OUT} drops by more than 7.0% from nominal, or during the absence of a correct Watchdog signal.
EPAD	EPAD	Connect to Ground potential or leave unconnected.

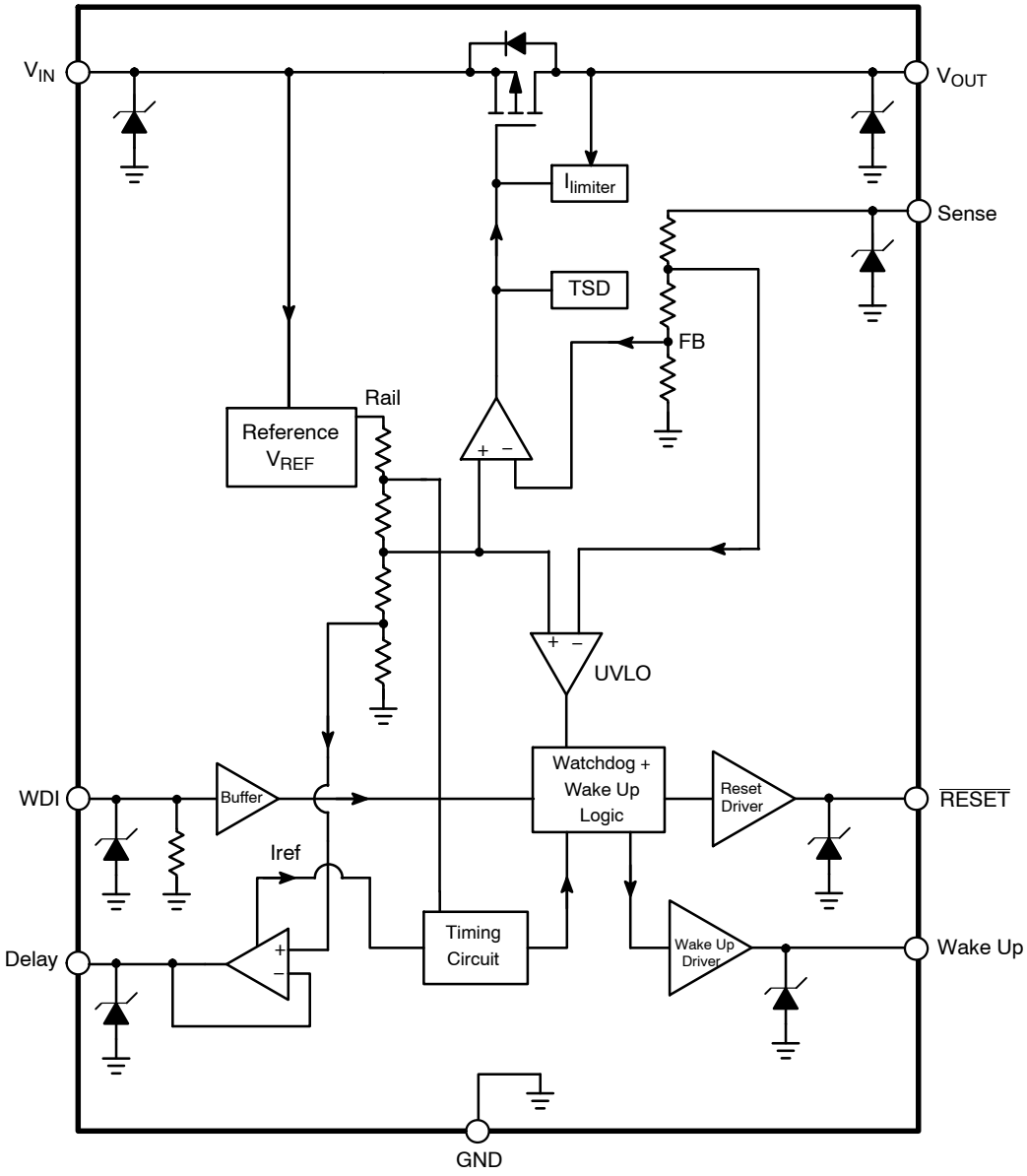


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
DC Voltage (Note 1) − Input Voltage	V_{IN}	−0.3	40	V
Peak Transient Voltage (Load Dump) (Note 2) − Input Voltage	U_S*	−	45	V
Output Voltage	V_{OUT}	−0.3	7	V
Sense Voltage	Sense	−0.3	7	V
$\overline{\text{RESET}}$ Output Voltage Powered chip or connected external components to chip Pin to Ground only, all other pins left disconnected	V_{RESET}	 −0.3 −0.3	 V_{OUT} +7.0	V
$\overline{\text{RESET}}$ Output Current ($\overline{\text{RESET}}$ may be incidentally shorted either to V_{OUT} or to GND without damage)	I_{RESET}	−	Internally Limited	mA
Wake Up Voltage Powered chip or connected external components to chip Pin to Ground only, all other pins left disconnected	V_{WU}	 −0.3 −0.3	 V_{OUT} +7.0	V
Watchdog Input Voltage	V_{WDI}	−0.3	7	V
Delay Timing Voltage	V_{Delay}	−0.3	3.6	V
Operating Junction Temperature	T_J	−40	150	°C
Storage Temperature Range	T_S	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750−1.

ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−1	1	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (JS−001−2017).
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes 2 × 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018.

LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating	Symbol	Value	Unit
Moisture Sensitivity Level SOIC−8 EP	MSL	 2	−

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

See Package Thermal Data Section (Page 15)

ELECTRICAL CHARACTERISTICS

V_{IN} = 13.5 V, C_{IN} = 0.1 μF, C_{OUT} = 1 μF, R_{Delay} = 60 kΩ, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise and are guaranteed by test, design or statical correlation. Typical values are referenced to T_J = 25°C (Note 5).

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
OUTPUT						
Output Voltage	V_{IN} = 6 V to 28 V, I_{OUT} = 0.1 mA to 150 mA	V_{OUT}	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 6 V to 28 V, I_{OUT} = 5.0 mA	Reg_{line}	−20	–	20	mV
Load Regulation	I_{OUT} = 0.1 mA to 150 mA	Reg_{load}	−30	–	30	mV
Current Limit	V_{OUT} = 96% of V_{OUT_nom}	I_{LIM}	255	505	800	mA
Dropout Voltage (Note 6)	I_{OUT} = 150 mA	V_{DO}	–	355	700	mV
QUIESCENT CURRENT						
Quiescent Current, $I_q = I_{IN} - I_{OUT}$	I_{OUT} = 0 mA I_{OUT} = 0.1 mA	I_q	– –	74 76	83 85	μA
$\overline{\text{RESET}}$ OUTPUT						
Output Voltage Reset Threshold		$V_{th(RO)}$	90	93	95	% V_{OUT_nom}
Reset Output Low Voltage	R_{load} = 10 kΩ to V_{OUT}, V_{OUT} = 1.0 V	V_{ROL}	–	0.025	0.4	V
Reset Output High Voltage	R_{load} = 10 kΩ to GND	V_{ROH}	4.50	4.86	–	V
Power On Reset Delay Time	R_{Delay} = 60 kΩ, I_{OUT} = 5 mA R_{Delay} = 120 kΩ, I_{OUT} = 5 mA R_{Delay} = 500 kΩ, I_{OUT} = 5 mA	t_{RD}	2 – –	3.1 6.2 26	4 – –	ms
Reset Reaction Time (Note 7)		t_{RR}	–	20	–	μs
WATCHDOG INPUT						
Threshold Voltage		WDI_{high}	30	50	70	% V_{OUT}
Hysteresis (Note 7)		WDI_{hys}	25	100	–	mV
Input Current	WDI = 6 V		–	1.1	2	μA
WAKE UP OUTPUT						
Wake Up Period	R_{Delay} = 60 kΩ R_{Delay} = 120 kΩ R_{Delay} = 500 kΩ	T_{WUP}	18 – –	24 47 194	32 – –	ms
Wake Up Duty Cycle Nominal		t_{WUDC}	45	50	55	%
$\overline{\text{RESET}}$ HIGH to Wakeup Rising Delay Time	50% $\overline{\text{RESET}}$ rising edge to 50% Wake Up edge R_{Delay} = 60 kΩ R_{Delay} = 120 kΩ R_{Delay} = 500 kΩ	t_{RHWU}	 9 – –	 12 23.5 97	 16 – –	ms
Wake Up Response to Watchdog Input	50% WDI falling edge to 50% Wake Up falling edge	t_{WUWH}	–	0.80	2	μs
Wake Up Response to $\overline{\text{RESET}}$	50% $\overline{\text{RESET}}$ falling edge to 50% Wake Up falling edge $V_{OUT} = V_{OUT\_nom} \rightarrow 90\%$ of V_{OUT_nom}	t_{WURT}	 –	 0.012	 1	μs
Output Low	R_{load} = 10 kΩ to V_{OUT}, $V_{OUT} \geq$ 1.0 V	V_{WUL}	–	0.085	0.4	V
Output High	R_{load} = 10 kΩ to GND	V_{WUH}	4.5	4.86	–	V
DELAY						
Output Voltage	R_{Delay} = 60 kΩ, 120 kΩ, 500 kΩ	V_{Delay}	–	0.48	–	V

ELECTRICAL CHARACTERISTICS (continued)
V_{IN} = 13.5 V, C_{IN} = 0.1 μF, C_{OUT} = 1 μF, R_{Delay} = 60 kΩ, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise and are guaranteed by test, design or statical correlation. Typical values are referenced to T_J = 25°C (Note 5).

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
THERMAL SHUTDOWN						
Thermal Shutdown Threshold (Note 7)		T_{SD}	150	175	210	°C
Thermal Shutdown Hysteresis (Note 7)		T_{SH}	–	8	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cyclepulse techniques are used during testing to maintain the junction temperature as close to ambient as possible
6. Measured when the output voltage has dropped 100 mV from the nominal value.
7. Values based on design and/or characterization.

TIMING DIAGRAMS

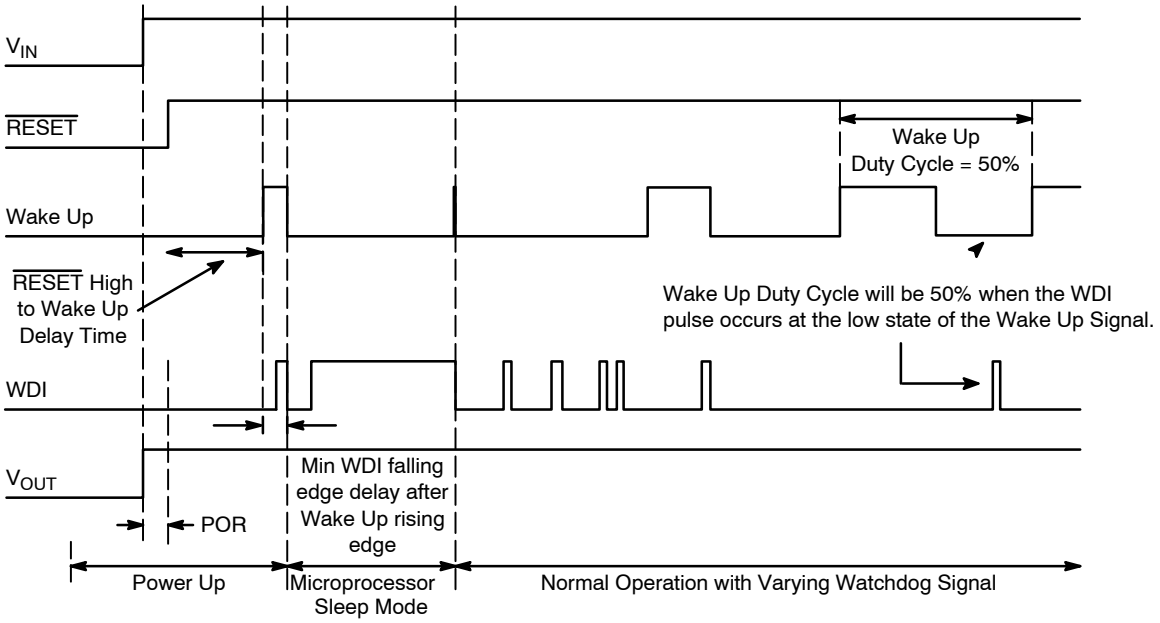


Figure 3. Power Up, Sleep Mode and Normal Operation

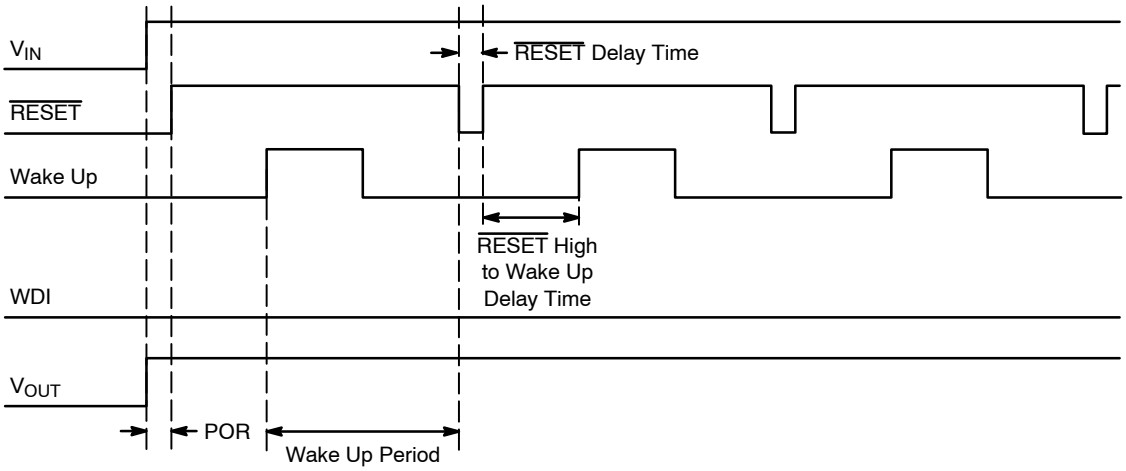


Figure 4. Error Condition: Watchdog Remains Low and a RESET Is Issued

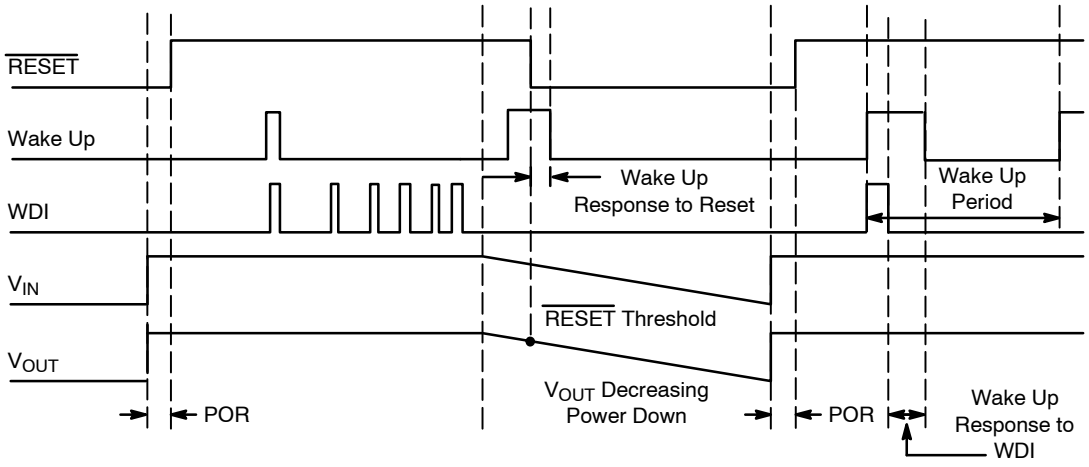


Figure 5. Power Down and Restart Sequence

TYPICAL PERFORMANCE CHARACTERISTICS

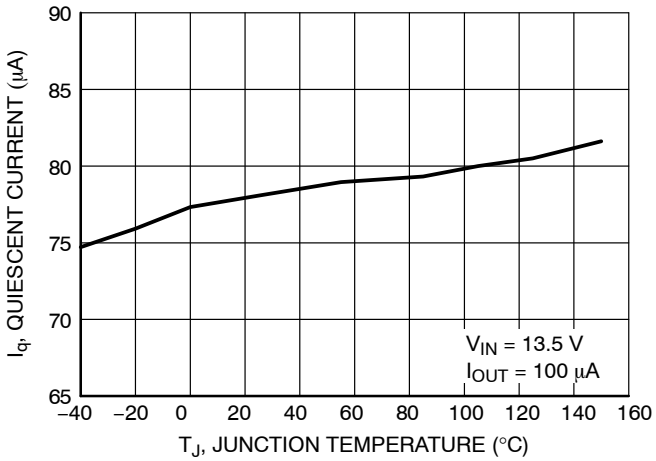


Figure 6. Quiescent Current vs. Junction Temperature

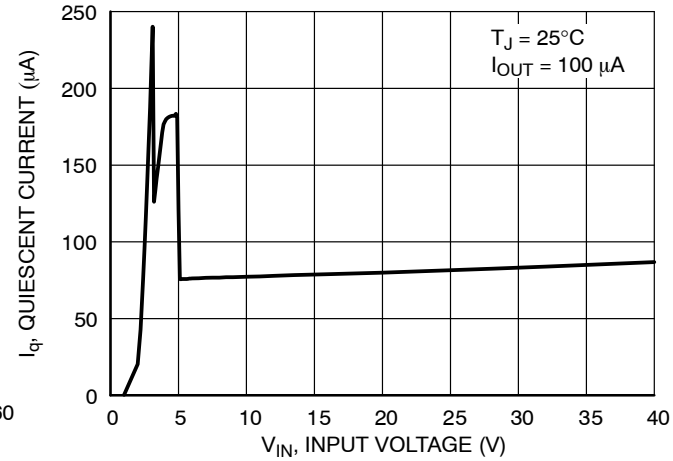


Figure 7. Quiescent Current vs. Input Voltage

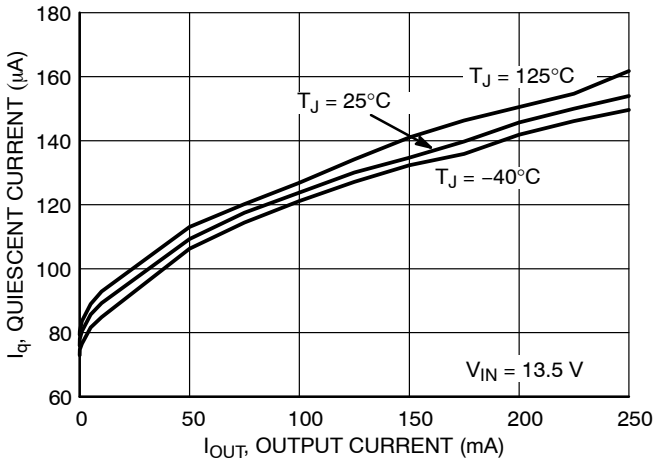


Figure 8. Quiescent Current vs. Output Current

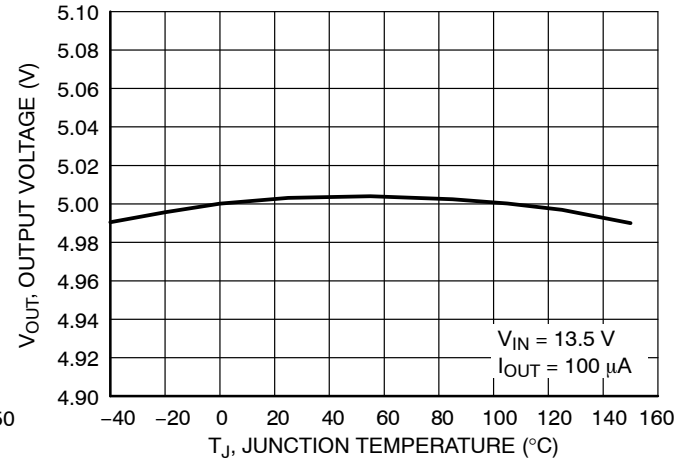


Figure 9. Output Voltage vs. Junction Temperature

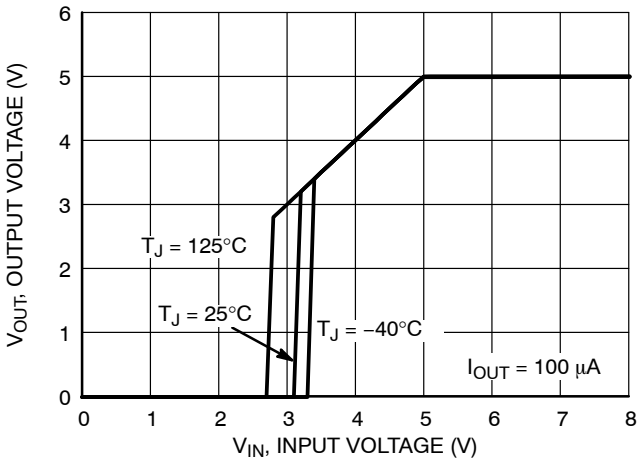


Figure 10. Output Voltage vs. Input Voltage

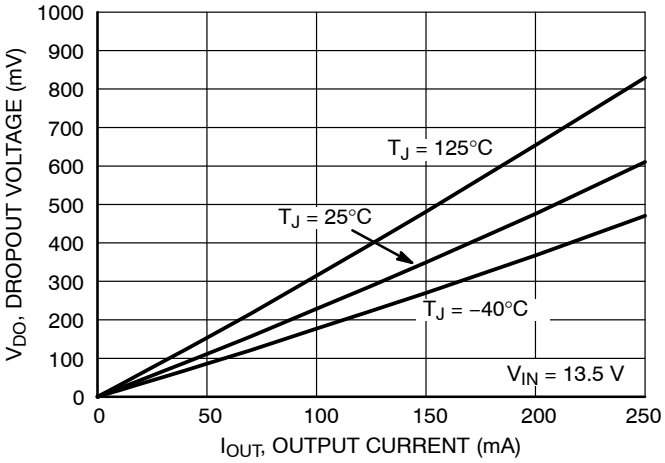


Figure 11. Dropout Voltage vs. Output Current

TYPICAL PERFORMANCE CHARACTERISTICS

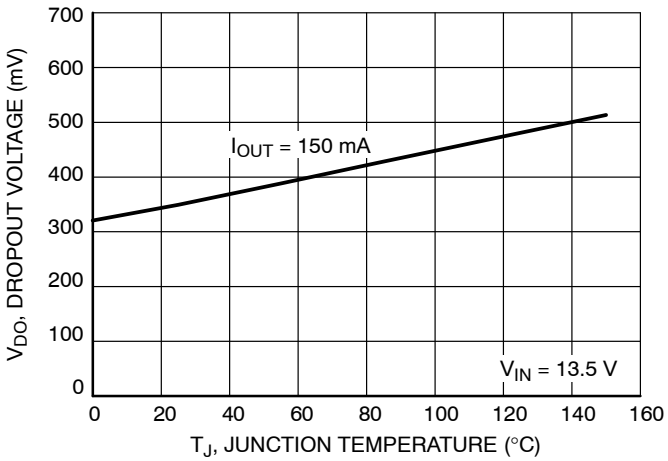


Figure 12. Dropout Voltage vs. Junction Temperature

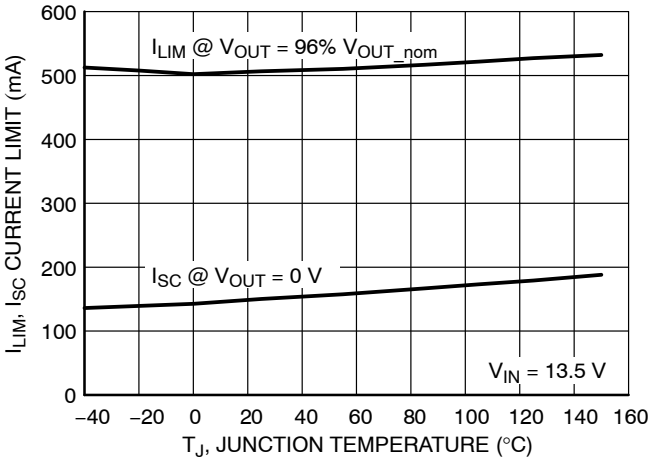


Figure 13. Output Current Limit vs. Junction Temperature

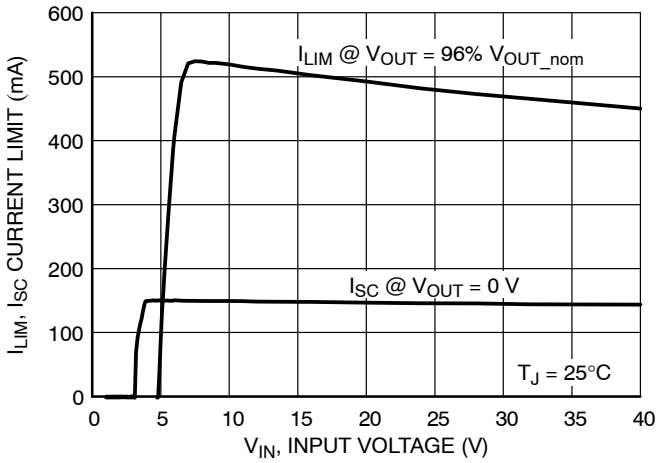


Figure 14. Output Current Limit vs. Input Voltage

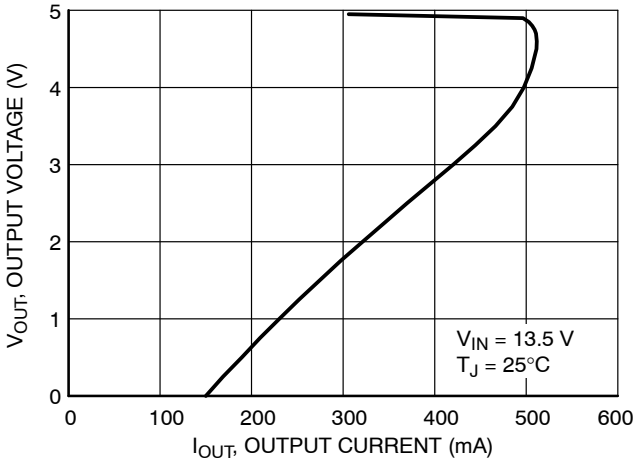


Figure 15. Foldback Characteristic of Output Voltage

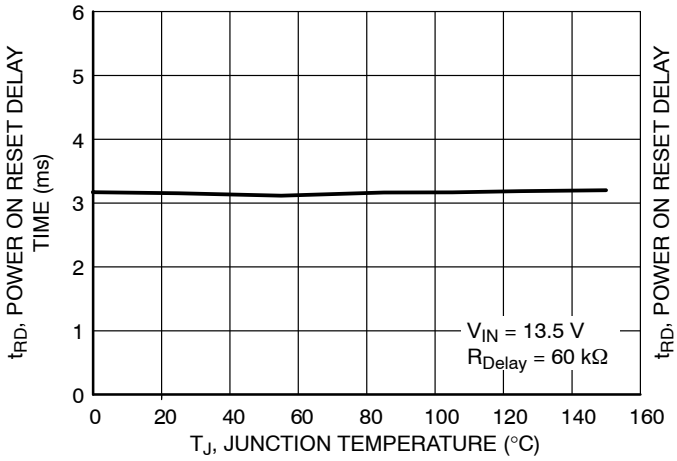


Figure 16. Reset Delay Time vs. Junction Temperature

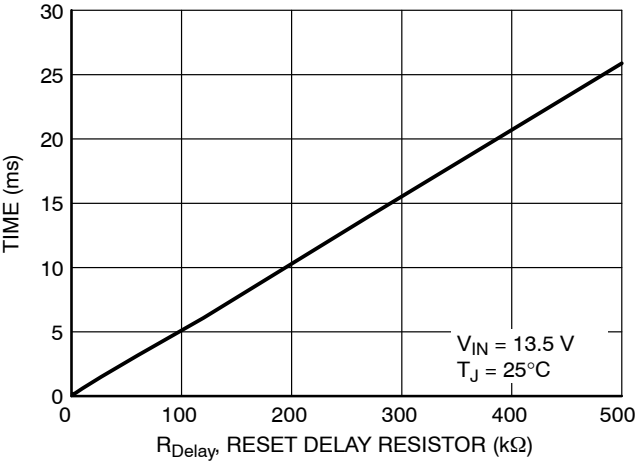


Figure 17. Reset Delay Time vs. Reset Delay Resistor

TYPICAL PERFORMANCE CHARACTERISTICS

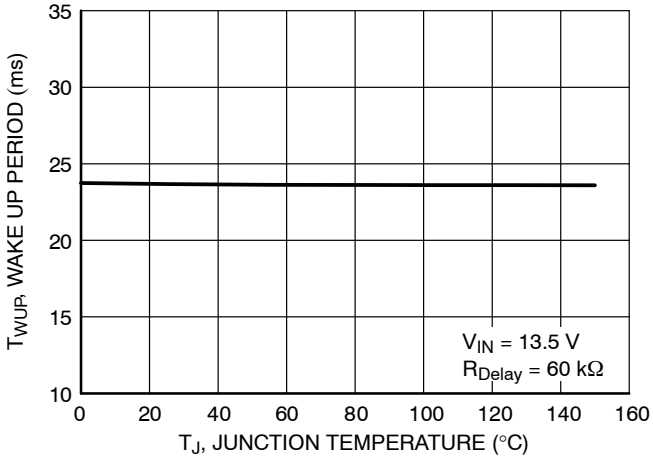


Figure 18. Wakeup Period vs. Junction Temperature

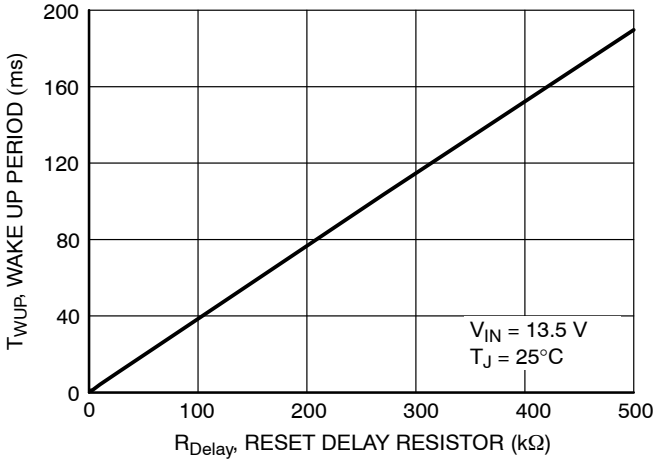


Figure 19. Wakeup Period vs. Reset Delay Resistor

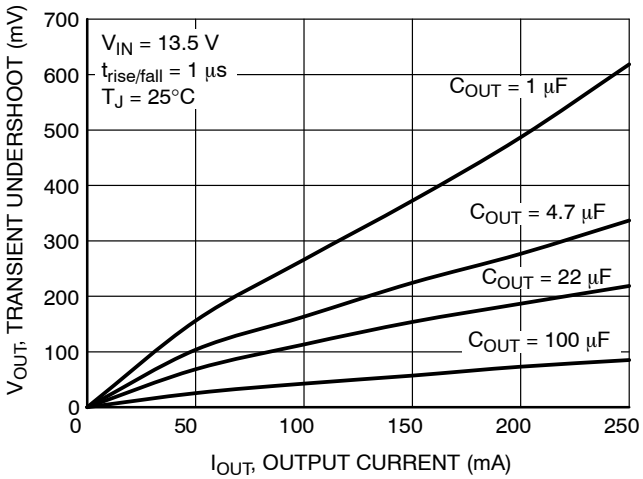


Figure 20. Load Transient Response

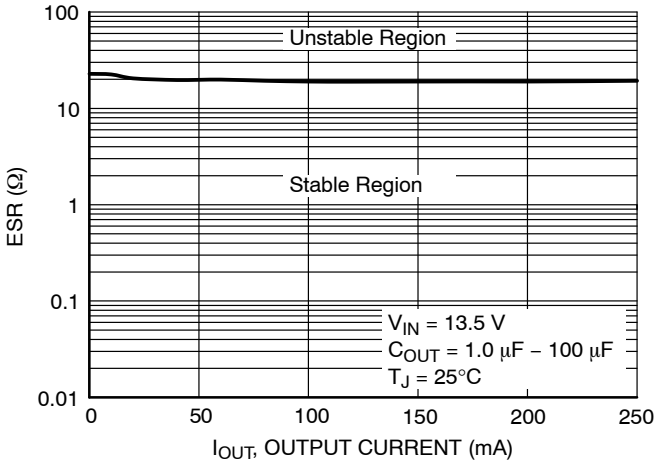


Figure 21. Output Stability with Output Capacitor ESR

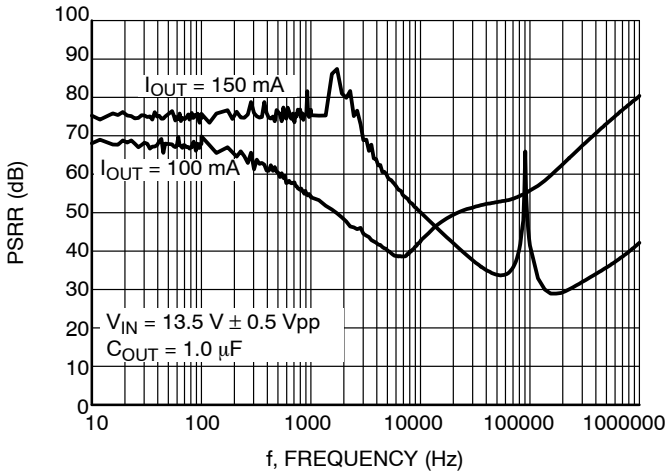


Figure 22. PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

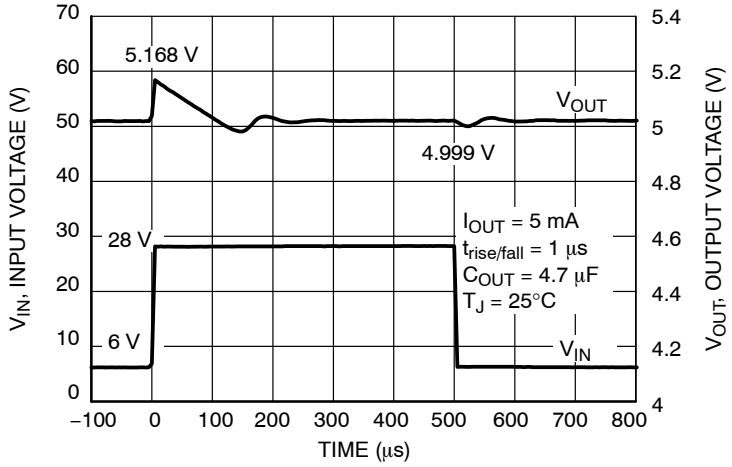


Figure 23. Line Transients

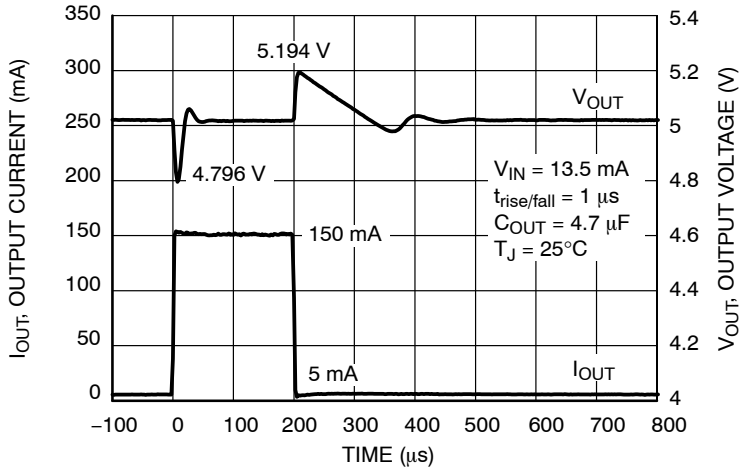


Figure 24. Load Transients

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current.

Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value.

Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

OPERATING DESCRIPTION

General

The NCV8508C is a precision micropower voltage regulator featuring low quiescent current (126 μA typical at 150 mA load) and low dropout voltage (355 mV typical at 150 mA). Integrated microprocessor control functions include Watchdog, Wake Up and $\overline{\text{RESET}}$. The combination of low quiescent current and comprehensive microprocessor interface functions make the NCV8508C ideal for use in both battery operated and automotive applications.

The NCV8508C is internally protected against short circuit and thermal runaway conditions. No external components are required to engage these protective mechanisms. The device continues to operate through 45 V input transients, an important consideration in automotive environments.

Wake Up and Watchdog

To reduce battery drain, a microprocessor or microcontroller can transition to a low current consumption mode (sleep mode) when code execution is suspended or complete. The NCV8508C Wake Up signal is generated and output periodically to interrupt sleep mode. The nominal Wake Up output is a 5 V square wave (generated from V_{OUT}) with a duty cycle of 50%, at a frequency determined by external timing resistor R_{Delay}. In response to the rising edge of the Wake Up signal, the microprocessor will subsequently output a Watchdog pulse and check its inputs to decide if it should resume normal operation or remain in sleep mode.

The NCV8508C responds to the falling edge of the Watchdog signal, which it expects at least once during each Wake Up period. Minimum WDI pulse width must be higher than 1 μs and WDI falling edge must not occur during 5 μs after Wake Up signal rising edge, otherwise WDI falling edge may not be accepted by watchdog logic. This provides higher robustness of watchdog logic against glitch pulses and disturbances in the application. When the correct Watchdog signal is received, the Wake Up output is forced low. Other Watchdog pulses received within the same cycle are ignored. The Watchdog circuitry continuously monitors the input Watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wake Up cycle will cause a Reset pulse to be output at the end of the Wake Up cycle (see Figure 5).

As output voltage falls, the output will maintain its current state down to V_{OUT} = 1 V. A Reset signal (active low) is asserted for any of four conditions:

1. During power up, $\overline{\text{RESET}}$ is held low until the output voltage is in regulation
2. During operation, if the output voltage falls below the Reset Threshold Voltage, $\overline{\text{RESET}}$ switches low, and will remain low until both the output voltage has recovered and the Reset delay timer cycle has completed following that recovery
3. $\overline{\text{RESET}}$ will switch low if the regulator does not receive a Watchdog input signal within a Wake Up period
4. Regardless of output voltage, $\overline{\text{RESET}}$ will switch low if the regulator input voltage V_{IN}, falls below a level required to sustain the internal control circuits. The specific voltage is temperature dependent, and is approximately 4.65 V at 25°C

The Wake Up output is pulled low during a $\overline{\text{RESET}}$ regardless of the cause of the $\overline{\text{RESET}}$. After the $\overline{\text{RESET}}$ returns high, the Wake Up cycle begins again (see Figure 5).

The Reset Delay Time, Wake Up signal period and $\overline{\text{RESET}}$ HIGH to Wake Up Rising Delay Time are all set by one external resistor, R_{Delay}, according to the following equations:

$$T_{WUP} = (3.95 \times 10^{-7}) \times R_{Delay} \quad \text{(eq. 1)}$$

$$t_{RD} = (5.20 \times 10^{-8}) \times R_{Delay} \quad \text{(eq. 2)}$$

$$t_{RHWU} = (1.96 \times 10^{-7}) \times R_{Delay} \quad \text{(eq. 3)}$$

Thermal Considerations

As power in the NCV8508C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8508C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8508C can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} + T_A]}{R_{\theta JA}} \quad \text{(eq. 4)}$$

Since T_J is not recommended to exceed 150°C, then the NCV8508C (SOIC−8 EP) soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 1.48 W when the ambient temperature (T_A) is 25°C. See Figure 25 for $R_{\theta JA}$ versus PCB copper area. The power dissipated by the NCV8508C can be calculated from the following equations:

$$P_D = V_{IN} \times I_{q@I_{OUT}} + I_{OUT} \times (V_{IN} - V_{OUT}) \quad \text{(eq. 5)}$$

or

$$V_{IN(MAX)} = \frac{P_{D(MAX)} + (I_{OUT} \times V_{OUT})}{I_{OUT} + I_q} \quad \text{(eq. 6)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$ less than the calculated value in Equation 4 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

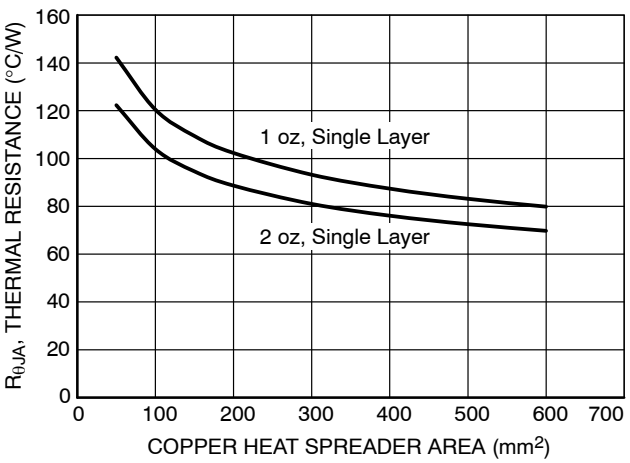


Figure 25. Thermal Resistance vs. PCB Copper Area (SOIC−8 EP)

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 7)}$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

Hints

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8508C and make traces as short as possible.

The NCV8508C is not developed in compliance with ISO26262 standard. If application is safety critical then the below application example diagram shown in Figure 26 can be used.

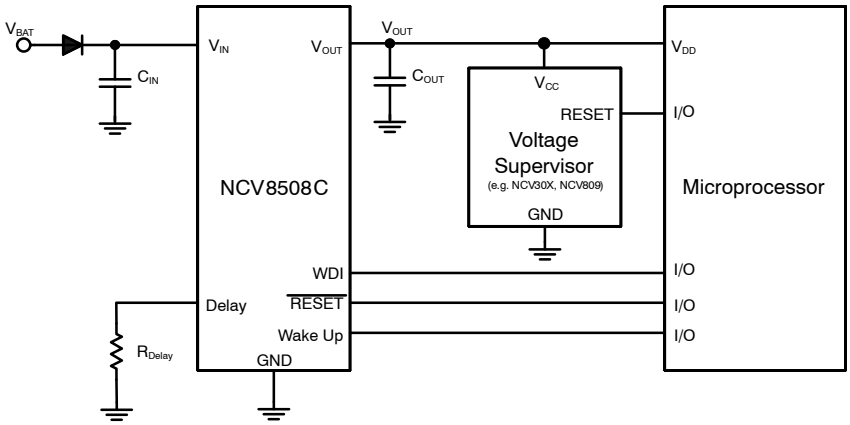


Figure 26. Application Diagram

RECOMMEND THERMAL DATA FOR SOIC−8 EP PACKAGE

Parameter	Test Conditions Typical Value		Unit
Pad is Soldered to PCB Copper	**Min−Pad Board** (Note 8)	**1”−pad Board** (Note 9)	
Junction−to−Lead (psi−JL, Ψ_{JL})	88.3	39.9	°C/W
Junction−to−Lead (psi−JPad, Ψ_{Jp})	21.0	22.3	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	139.6	76.8	°C/W

8. 1 oz. copper, 54 mm^2 copper area, 0.062” thick FR4.
9. 1 oz. copper, 717 mm^2 copper area, 0.062” thick FR4.

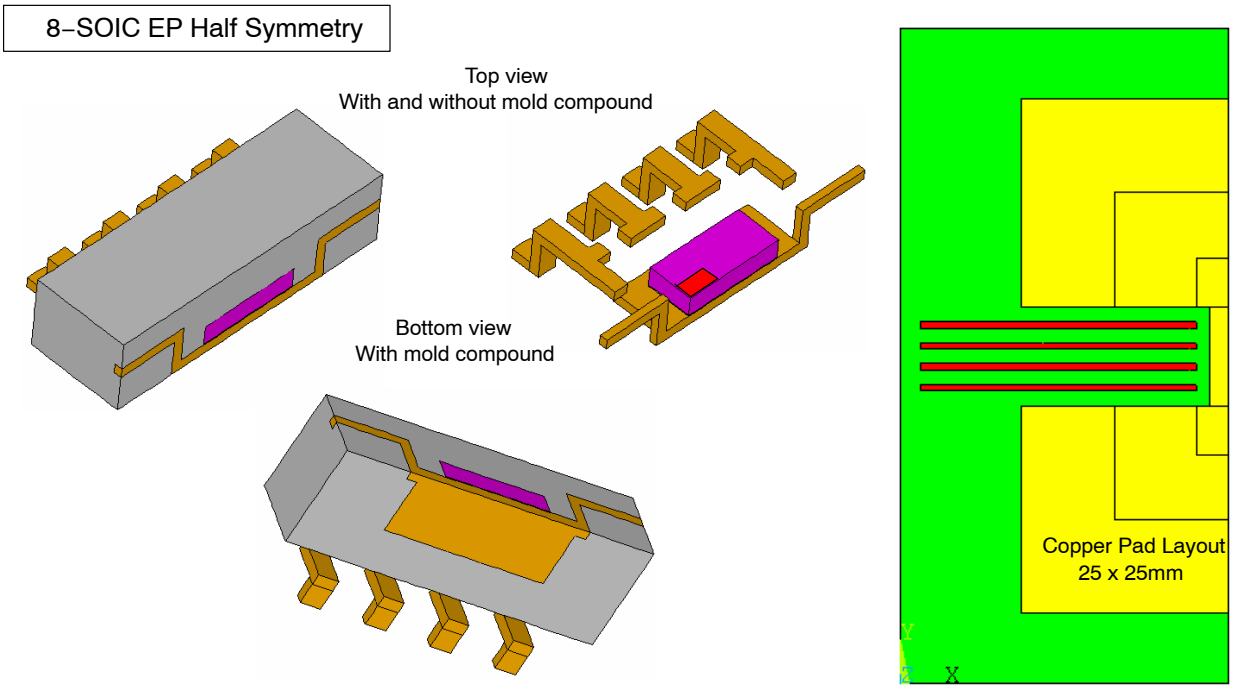


Figure 27. Internal Construction of the Package and PCB Layout for Multiple Pad Area

Table 1. SOIC 8−Lead EP Thermal RC Network Models

	54 mm²	717 mm²		54 mm²	717 mm²	Cu Area
	Cauer Network			Foster Network		
	C's	C's	Units	Tau	Tau	Units
1	1.21E−06	1.21E−06	Ws/°C	1.00E−06	1.00E−06	s
2	4.64E−06	4.64E−06	Ws/°C	1.00E−05	1.00E−05	s
3	1.33E−05	1.33E−05	Ws/°C	1.00E−04	1.00E−04	s
4	6.61E−05	6.61E−05	Ws/°C	4.44E−04	4.44E−04	s
5	5.80E−04	5.82E−04	Ws/°C	1.48E−03	1.48E−03	s
6	8.28E−03	8.64E−03	Ws/°C	3.30E−02	3.30E−02	s
7	2.56E−02	3.14E−02	Ws/°C	6.00E−01	6.00E−01	s
8	1.42E−01	5.01E−01	Ws/°C	4.00E+00	4.00E+00	s
9	3.81E−01	1.98E+00	Ws/°C	1.16E+01	4.83E+01	s
10	1.38E+00	2.93E+01	Ws/°C	5.85E+01	2.37E+02	s
	R's	R's		R's	R's	
1	1.061	1.061	°C/W	0.627	0.627	°C/W
2	2.502	2.502	°C/W	1.357	1.357	°C/W
3	7.018	7.016	°C/W	4.290	4.290	°C/W
4	5.901	5.896	°C/W	6.946	6.946	°C/W
5	2.261	2.247	°C/W	5.026	5.026	°C/W
6	5.048	4.657	°C/W	3.000	3.000	°C/W
7	21.735	15.845	°C/W	15.000	15.000	°C/W
8	41.592	9.514	°C/W	11.494	7.797	°C/W
9	25.463	20.786	°C/W	34.982	20.473	°C/W
10	27.050	7.289	°C/W	56.911	12.298	°C/W

NOTE: Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant R(t) = 225 * sqrt(time(sec)). The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

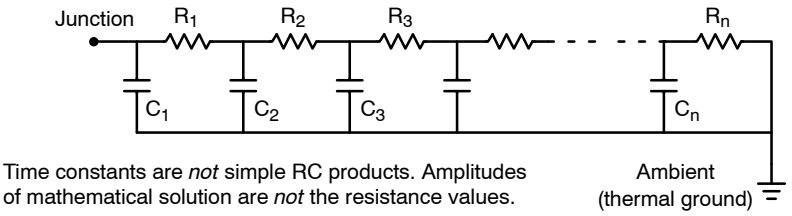


Figure 28. Grounded Capacitor Thermal Network (“Cauer” Ladder)

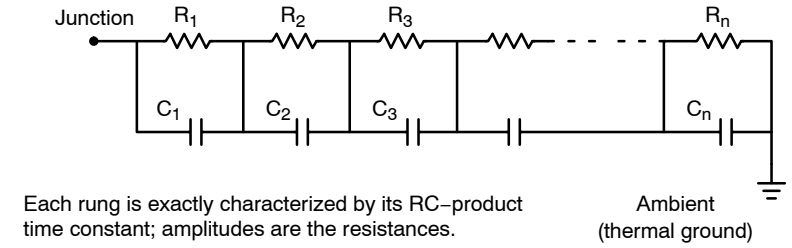


Figure 29. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

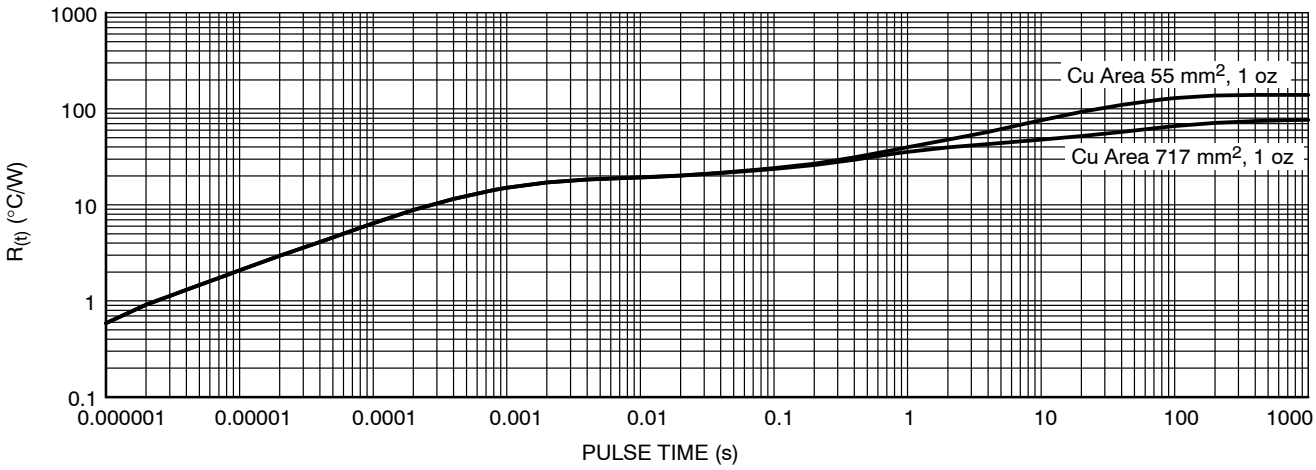


Figure 30. SOIC−8 EP Single Pulse Heating Curve

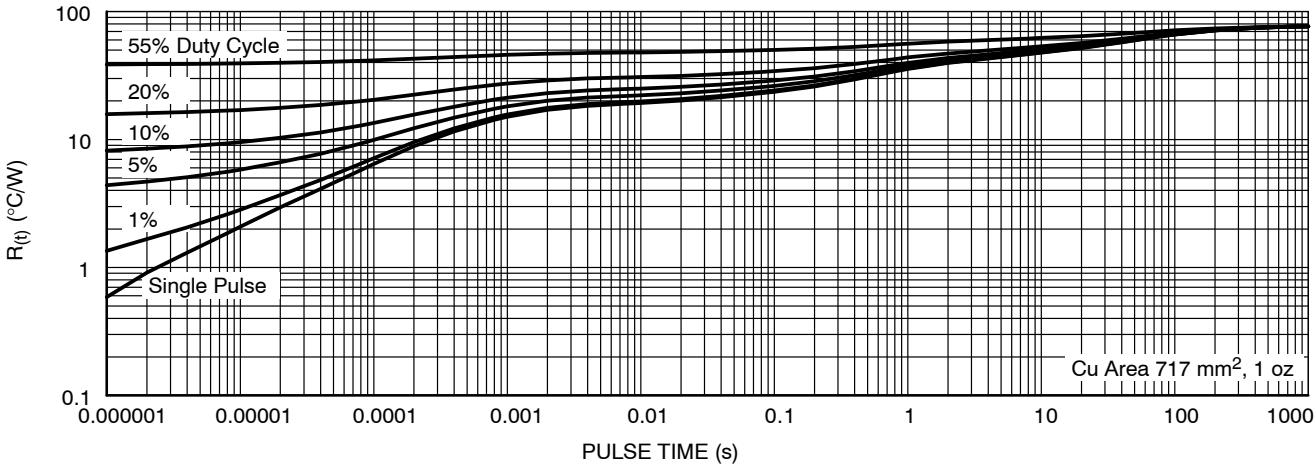


Figure 31. SOIC−8 EP Thermal Duty Cycle Curves on 1” Spreader Test Board

ORDERING INFORMATION

Device	Output Voltage	Timing Option	Package	Shipping†
NCV8508CPD501R2G	5.0 V	1	SOIC−8 EP (Pb−Free)	2500 / Tape & Reel

NOTE: Contact factory for other options.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

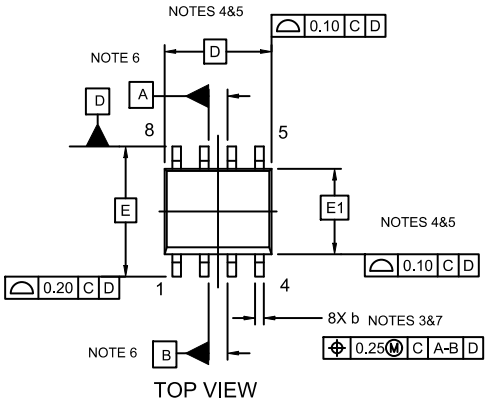
SCALE 1:1

SOIC−8 EP
CASE 751AC
ISSUE E

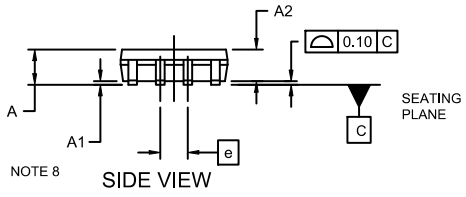
DATE 05 OCT 2022

NOTES:

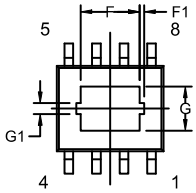
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



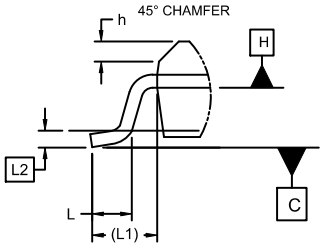
TOP VIEW



SIDE VIEW

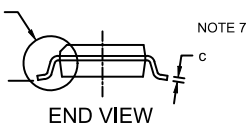


BOTTOM VIEW

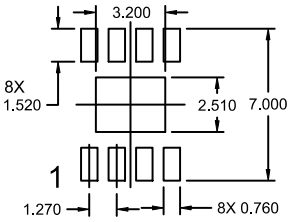


DETAIL A

DETAIL A



END VIEW

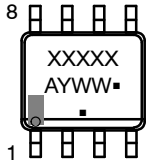


RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	---	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1		0.20 REF	
G	1.55	2.03	2.51
G1		0.46 REF	
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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