DATA SHEET
www.onsemi.com

Current-Shunt Monitors, 40 V Common Mode, Unidirectional, Single, Dual

NCS21673, NCV21673, NCS21674, NCV21674

The NCS21673 and NCS21674 are a series of current sense amplifiers offered in gains of 20, 50, 100 and 200 V/V. These parts can measure voltage across shunts at common mode voltages from −0.1 V to 40 V, independent of supply voltage. This helps measuring of fast transients and allows the same type of part to be used for high side and low side current sensing. These devices can operate from a single 2.7 V to 5.5 V power supply. With a −3 dB BW of up to 350 kHz and a Slew Rate of 2 V/us typical, the fast detection of current changes is ensured. These parts are available in TSOP−5 and Micro−8 packages. The dual version makes current sensing in multiple points of a system both space and cost effective.

Features

- Wide Common Mode Input Range: −0.1 V to 40 V
- Supply Voltage Range: 2.7 V to 5.5 V
- Low Offset Voltage
- Low Offset Drift
- Low Current Consumption: 300 μA max per channel
- NCV Prefix for Automotive Grade 1 and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High−Side Current Sensing
- Low−Side Current Sensing
- Power Management
- Automotive

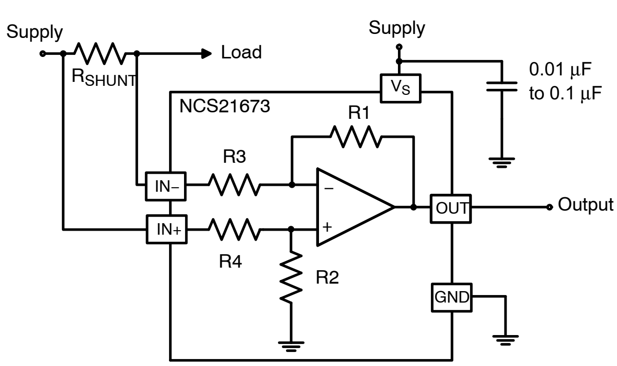
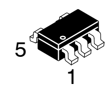
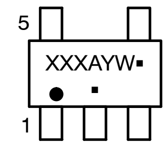


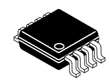
Figure 1. Example Application Schematic of High−Side Current Sensing

MARKING DIAGRAMS

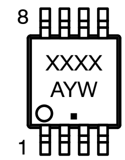


TSOP−5
CASE 483





Micro8
CASE 846A−02



XXX	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

See pin connections on page 2 of this data sheet.

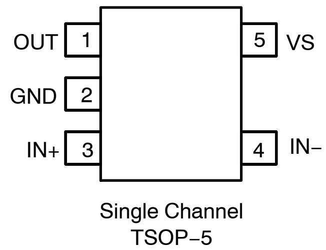
ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

September, 2022 − Rev. 1

Publication Order Number:
NCS21673/D

PIN FUNCTION DESCRIPTION



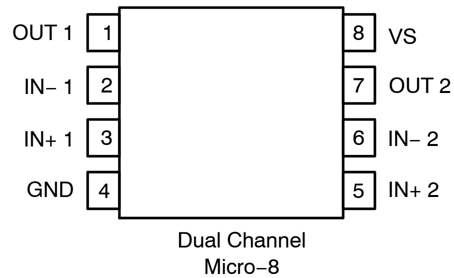


Figure 2. Pin Function Description

PIN DESCRIPTION

Pin Name	Type	Description
IN+	Input	This pin is connected to the positive side of the sense resistor or current shunt.
IN−	Input	This pin is connected to the negative side of the sense resistor or current shunt.
OUT	Output	The output pin provides a low impedance voltage output.
V_S	Supply	This is the positive supply pin that provides power to the internal circuitry. An external bypass capacitor of 0.1 μF is recommended to be placed as close as possible to this pin.
GND	Supply	This is the negative supply rail of the circuit.

MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply Voltage (Note 1)		V_S	−0.3 to 5.5	V
Analog Inputs	Differential (V_{IN+})−($V_{IN−}$) (Note 2)	V_{IN+}, $V_{IN−}$	±42	Analog Inputs
	Common−Mode (Note 2)		−0.3 to +42	
Output		V_{OUT}	GND−0.3 to (V_s) +0.3	V
Input Current into Any Pin		I_{IN}	±10	mA
Maximum Junction Temperature		$T_{J(max)}$	+150	°C
Storage Temperature Range		T_{STG}	−65 to +150	°C
ESD Capability, Human Body Model (Note 3)		HBM	±2000	V
Charged Device Model (Note 3)		CDM	±1000	V
Latch−up Current (Note 4)			±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters.
2. Input voltage at any pin may exceed the voltage shown if current at that pin is limited to ±10 mA
3. This device series incorporates ESD protection and is tested by the following methods: ESD Human Body Model tested per JEDEC standard JS−001−2017
   ESD Charged Device Model tested per JEDEC standard JS−002−2014
4. Latch−up Current tested per JEDEC standard: JESD78E

THERMAL CHARACTERISTICS

Parameter	Symbol	Package	Value	Unit
Thermal Resistance, Junction−to−Air (Notes 5, 6)	θ_{JA}	TSOP−5 / SOT23−5	208	°C/W
		Micro8 / MSOP−8	162	

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Temperature	T_A	NCS prefix	–40	125	°C
		NCV prefix	–40	150	
Common Mode Input Voltage	V_{CM}	Full temperature range	–0.1	40	V
Supply Voltage	V_S	Full temperature range	2.7	5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
*During operation at Ta = 150°C the limitation for junction temperature (Tj(max) = 150°C) must be considered.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{SENSE} = (V_{IN+}) – ($V_{IN–}$); V_S = 5 V, V_{IN+} = 12 V, unless otherwise noted. **Boldface** limits apply over the specified temperature range, T_A = –40°C to 125°C unless otherwise noted, guaranteed by characterization and/or design.ss

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT							
Common Mode Rejection Ratio (RTI)*	CMRR	V_{IN+} = –0.1 V to 40 V, V_{SENSE} = 0 mV for G20, G50 and G100 V_{SENSE} = 5 mV for G200	G = 20	–	TBD	–	dB
				TBD	–	–	
			G = 50	–	100	–	
				86	–	–	
			G = 100	–	110	–	
				96	–	–	
			G = 200	–	120	–	
				100	–	–	
Input Offset Voltage (RTI)*	V_{OS}	T_A = 25°C, (V_{IN+}) = ($V_{IN–}$) = 12 V	G = 20	–	TBD	TBD	μV
			G = 50	–	±100	±550	
			G = 100	–	±100	±500	
			G = 200	–	±100	±500	
		T_A= 25°C, (V_{IN+}) = ($V_{IN–}$) = 0 V	G = 20	–	±25	TBD	
			G = 50	–	±25	±175	
			G = 100	–	±25	±175	
			G = 200	–	±25	±210	
Input Offset Voltage Drift vs. Temperature (RTI)*	dV_{OS}/dT	T_A = –40°C to +125°C	–	–	±0.2	±1	μV/°C
Power Supply Rejection Ratio (RTI)*	PSRR	VS = 2.7 V to 5.5 V, V_{SENSE} = 10 mV for G20, G50 and G100 V_{SENSE} = 5 mV for G200	–	–	8	**40**	μV/V
Input Bias Current	I_{IB}	V_{IN+} = 0 V	–	–	1	–	μA
		(V_{IN+}) = ($V_{IN–}$) = 12 V	–	–	100	–	
Input Offset Current	I_{IO}	V_{IN+} = 12 V, V_{SENSE} = 10 mV for G20, G50 and G100 V_{SENSE} = 5 mV for G200	–	–	±15	–	μA
OUTPUT							
Gain	G	G 20		–	20	–	V/V
		G 50		–	50	–	
		G 100		–	100	–	
		G 200		–	200	–	
Gain Error		T_A = 25°C		–	±0.1	–	%
		T_A = –40°C to +125°C		–	–	**±0.4**	

ELECTRICAL CHARACTERISTICS (continued)
At T_A = +25°C, V_{SENSE} = (V_{IN+}) – (V_{IN-}); V_S = 5 V, V_{IN+} = 12 V, unless otherwise noted. **Boldface** limits apply over the specified temperature range, T_A = –40°C to 125°C unless otherwise noted, guaranteed by characterization and/or design.ss

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
OUTPUT							
Gain Error vs Temperature		T_A = –40°C to +125°C		–	±1.5	**±20**	ppm/°C
Nonlinearity Error				–	±0.01	–	%
Maximum Capacitive Load	C_L	No sustained oscillation		–	1	–	nF
Settling Time to 1%				–	5	–	µs
VOLTAGE OUTPUT							
Output Voltage High, Swing from V_S Supply Rail	V_S – V_{OH}	V_S = 5.5 V R_L = 10 kΩ to GND, T_A = 25°C		–	0.02	–	V
		V_S = 5.5 V R_L = 10 k to GND, T_A = –40°C to 125°C		–	–	**0.03**	
Output Voltage Low, Swing from GND	V_{OL} – GND	V_S = 5.5 V R_L = 10 k to GND, T_A = 25°C		–	0.0005	–	V
		V_S = 5.5 V R_L = 10 k to GND, T_A = –40°C to 125°C		–	–	**0.005**	
FREQUENCY RESPONSE							
Bandwidth (f_{-3dB})	BW	C_L = 25 pF	G = 20	–	409	–	kHz
			G = 50	–	270	–	
			G = 100	–	240	–	
			G = 200	–	150	–	
Slew Rate	SR			–	2	–	V/µs
NOISE							
Voltage Noise Density (RTI)*	e_n	F = 1 kHz, G100		–	25	–	nV/√Hz
POWER SUPPLY							
Quiescent Current per Channel	I_Q	T_A = 25°C		–	195	260	µA
		T_A = –40°C to +125°C		–	–	**300**	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*RTI = Referred to input.

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = (V_{IN+}) − (V_{IN-}), V_S = 5.0 V, V_{IN+} = 12 V, and all gains unless otherwise noted.)

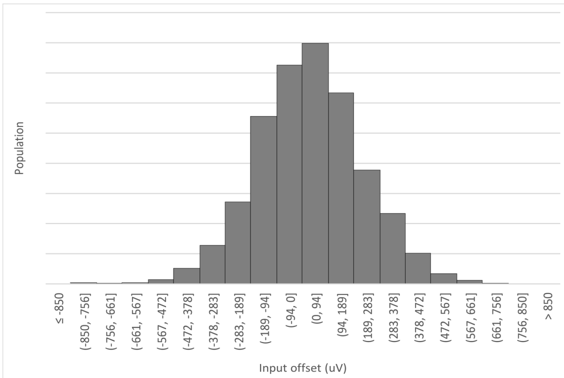


Figure 3a. Input Offset Voltage Distribution, G20

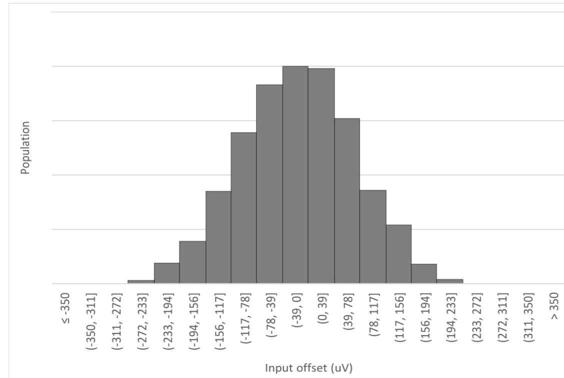


Figure 3b. Input Offset Voltage Distribution, G50

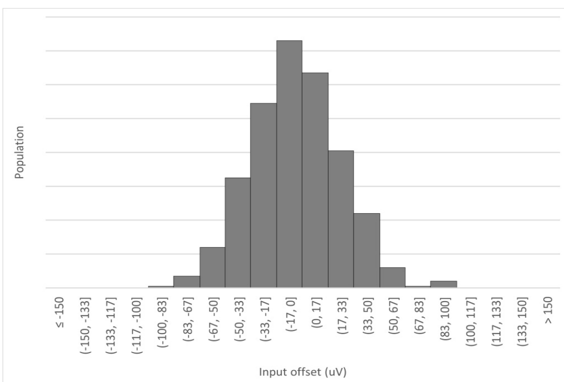


Figure 3c. Input Offset Voltage Distribution, G100

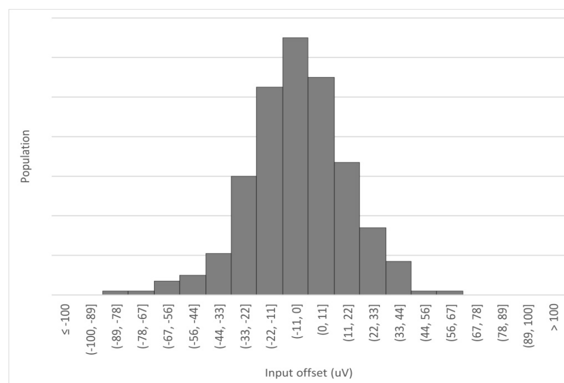


Figure 3d. Input Offset Voltage Distribution, G200

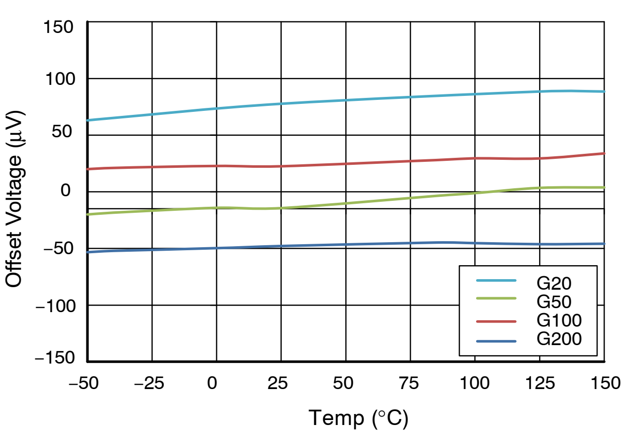


Figure 4. Input Offset vs. Temperature

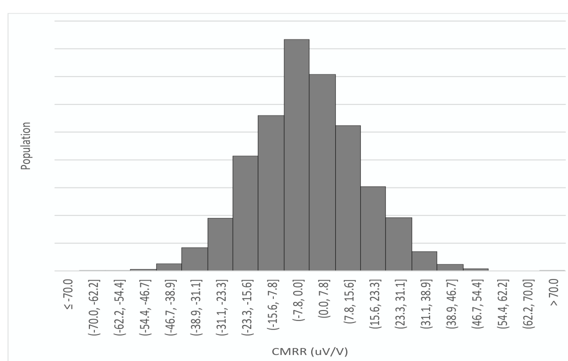


Figure 5a. Common Mode Rejection Ratio Distribution, G20

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = (V_{IN+}) – ($V_{IN–}$), V_S = 5.0 V, V_{IN+} = 12 V, and all gains unless otherwise noted.) (continued)

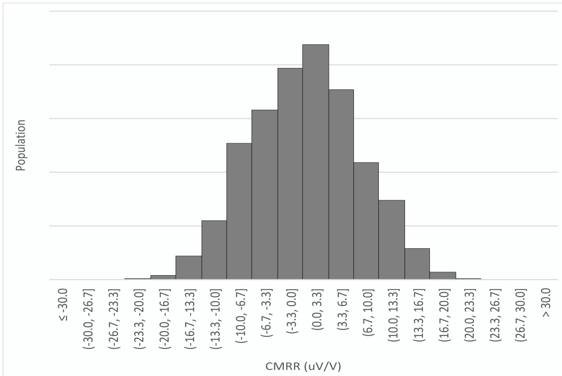


Figure 5b. Common Mode Rejection Ratio Distribution, G50

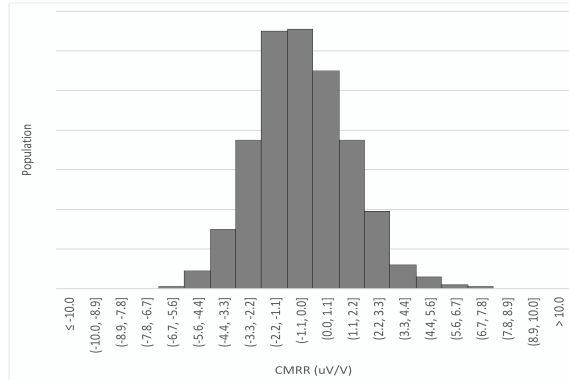


Figure 5c. Common Mode Rejection Ratio Distribution, G100

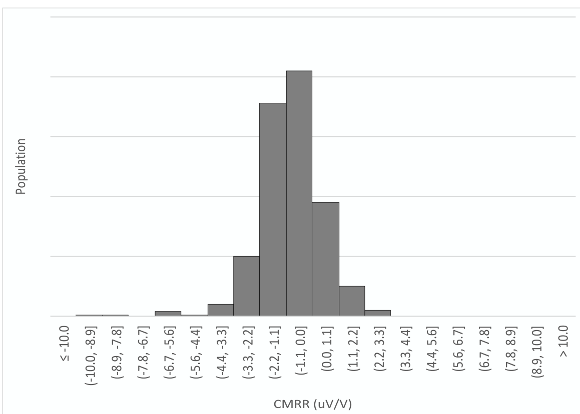


Figure 5d. Common Mode Rejection Ratio Distribution, G200

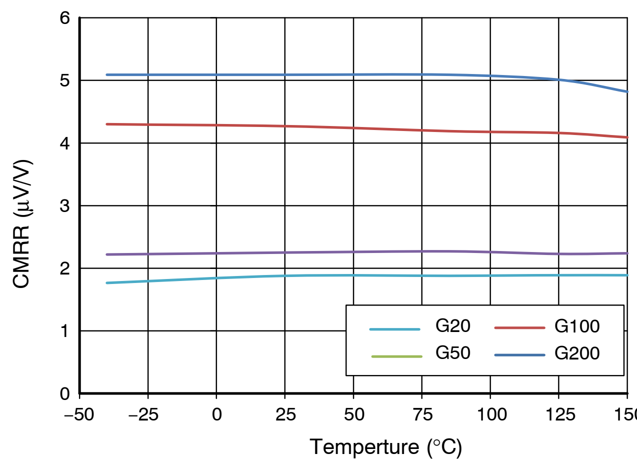


Figure 6. Common Mode Rejection Ratio vs Temperature

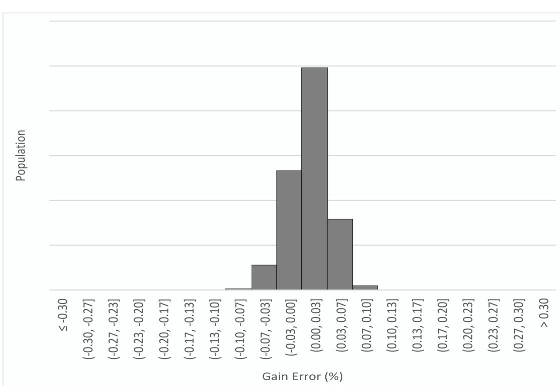


Figure 7a. Gain Error Distribution, G20

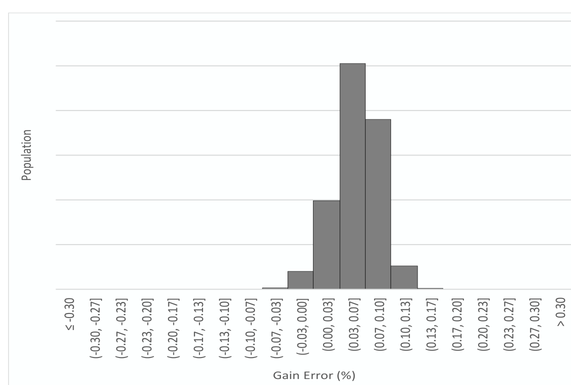


Figure 7b. Gain Error Distribution, G50

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = (V_{IN+}) − ($V_{IN−}$), V_S = 5.0 V, V_{IN+} = 12 V, and all gains unless otherwise noted.) (continued)

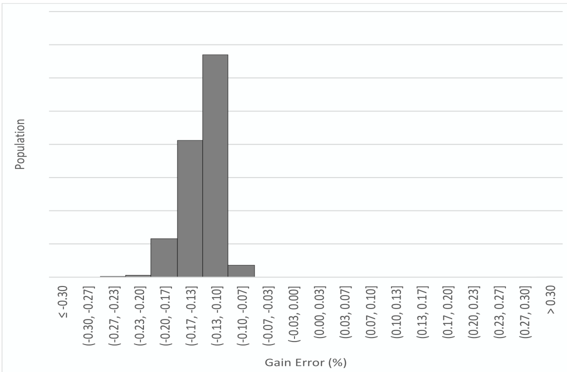


Figure 7c. Gain Error Distribution, G100

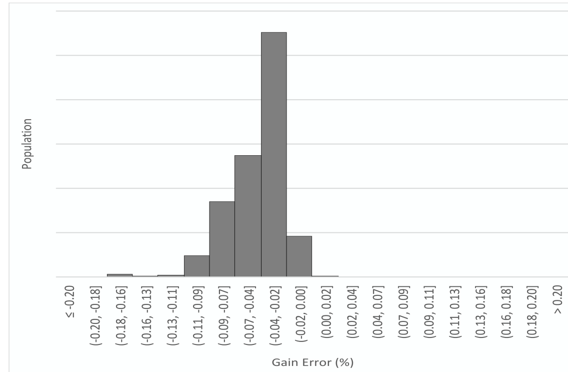


Figure 7d. Gain Error Distribution, G200

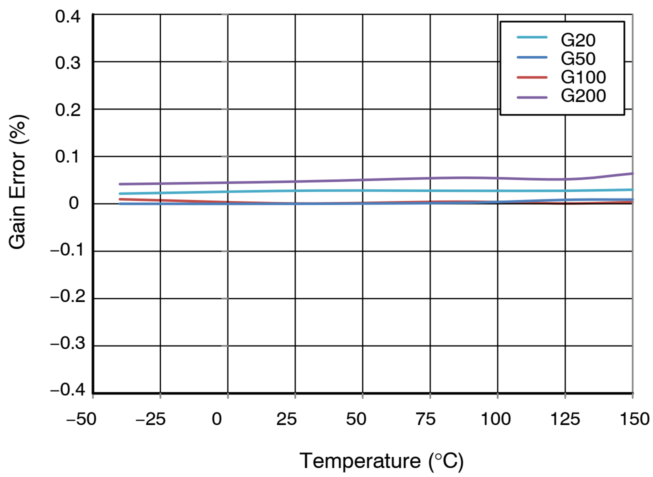


Figure 8. Gain Error vs Temperature

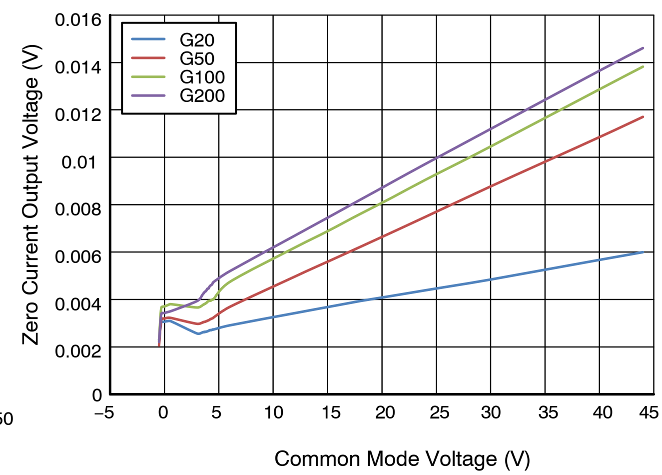


Figure 9. Zero Current Output vs Common Mode Voltage

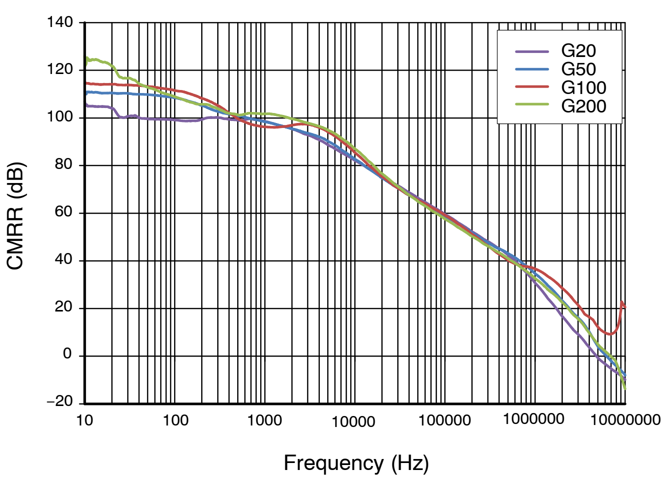


Figure 10. Common Mode Rejection Ratio vs Frequency

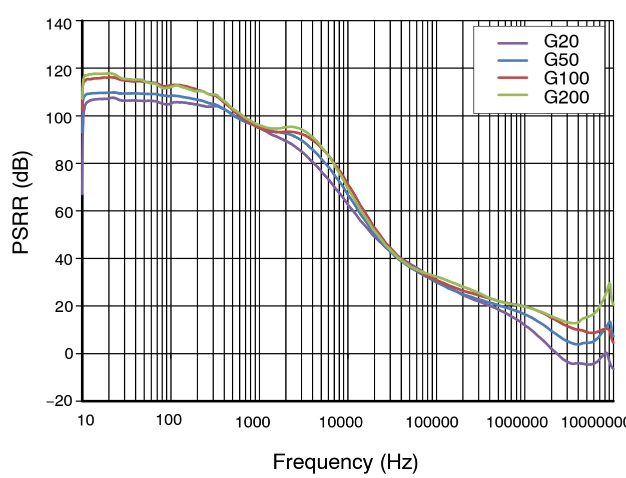


Figure 11. Power Supply Rejection Ratio vs Frequency

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = (V_{IN+}) − ($V_{IN−}$), V_S = 5.0 V, V_{IN+} = 12 V, and all gains unless otherwise noted.) (continued)

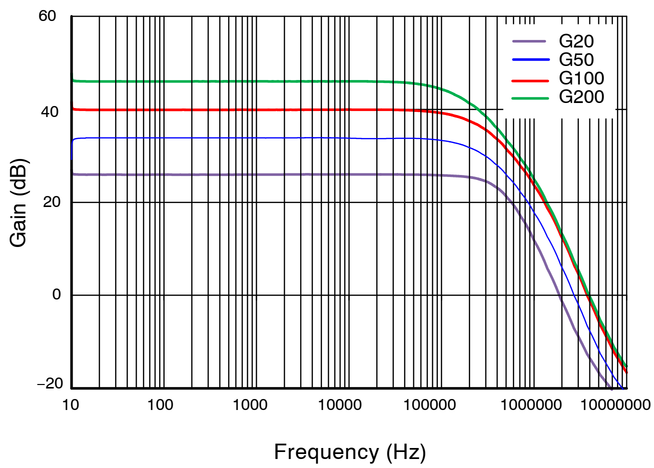


Figure 12. Gain vs Frequency

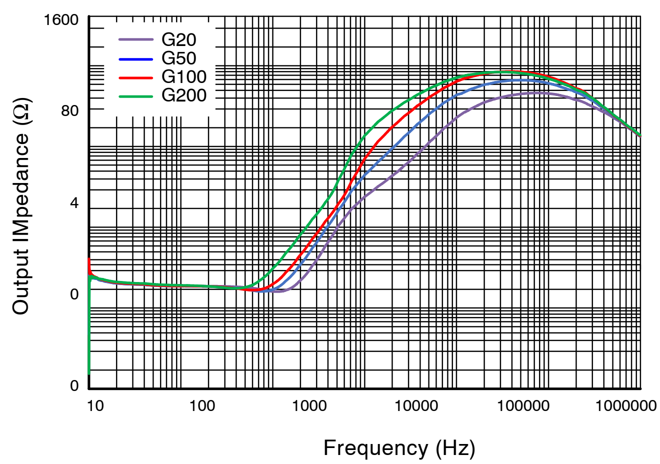


Figure 13. Output Impedance vs Frequency

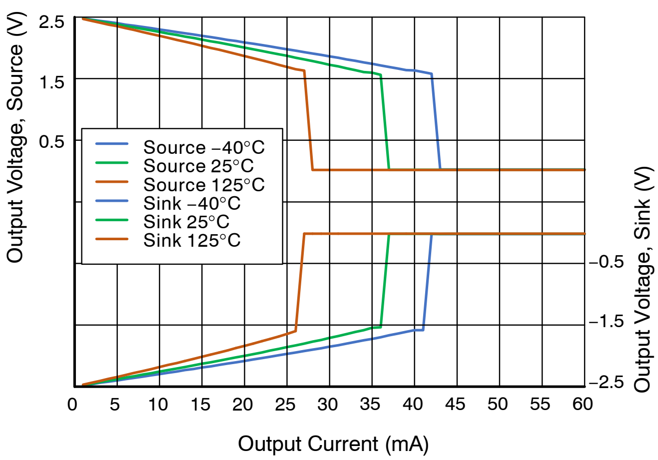


Figure 14. Output Voltage Swing vs Current

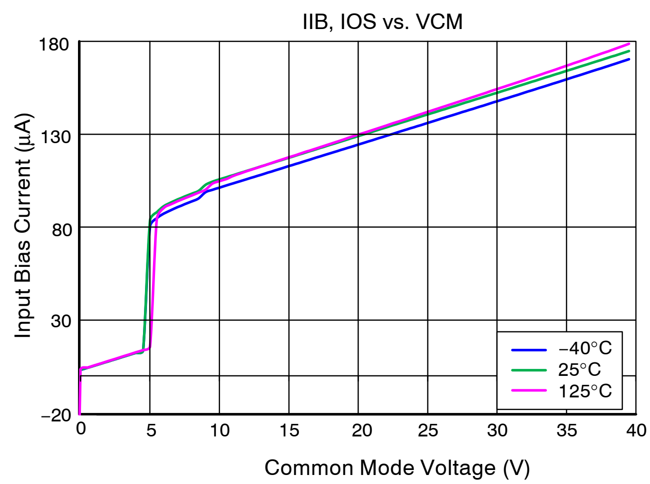


Figure 15. Input Bias Current vs Common Mode Voltage

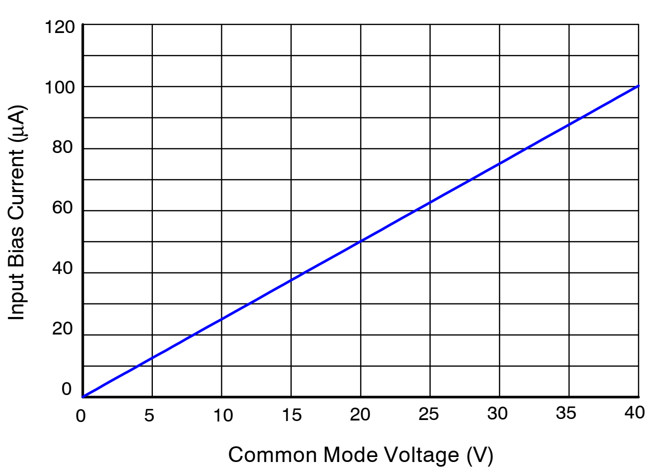


Figure 16. Input Bias Current vs Common Mode Voltage (VS open circuit)

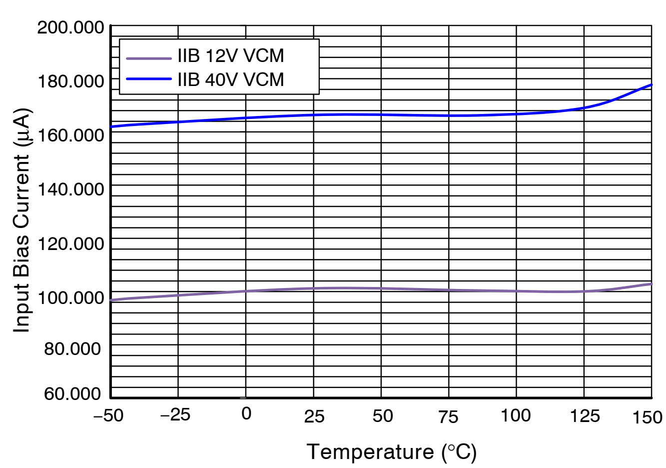


Figure 17. Input Bias Current vs Temperature

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = (V_{IN+}) − ($V_{IN−}$), V_S = 5.0 V, V_{IN}+ = 12 V, and all gains unless otherwise noted.) (continued)

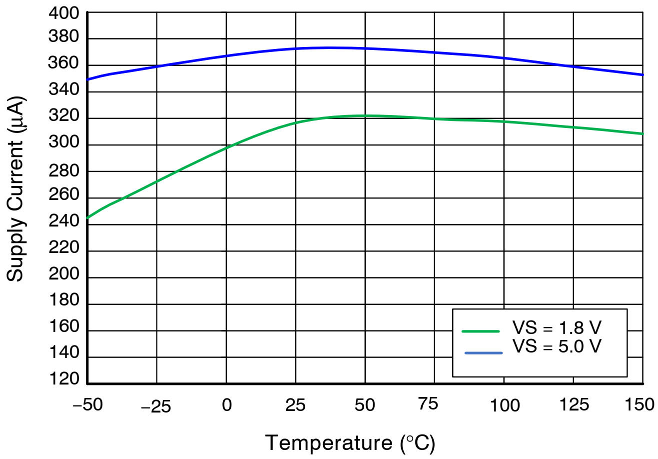


Figure 18. Quiescent Current vs Temperature

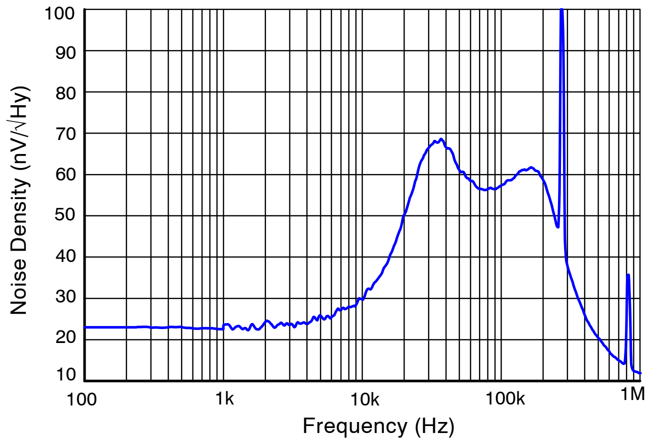


Figure 19. Noise Density, G100

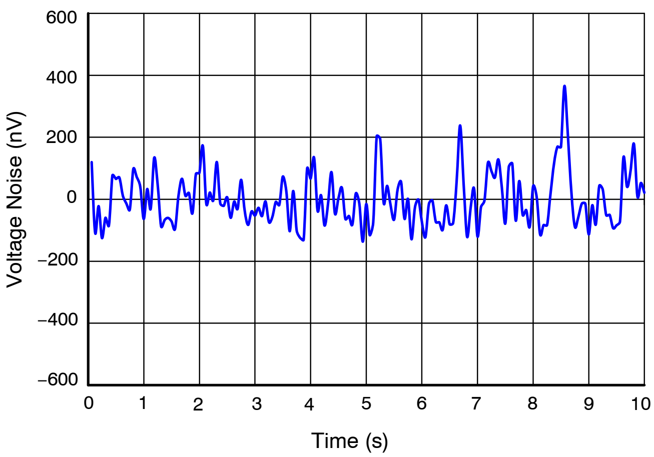


Figure 20. 0.1−Hz to 10−Hz Voltage Noise (Referred−To−Input)

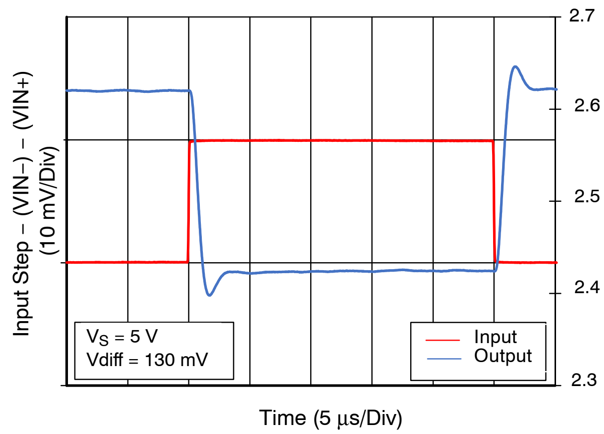


Figure 21a. Small Signal Step Response Inverting, G20

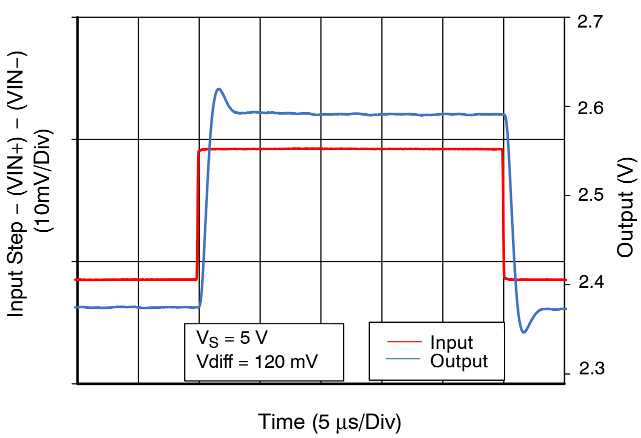


Figure 21b. Small Signal Step Response Non−Inverting, G20

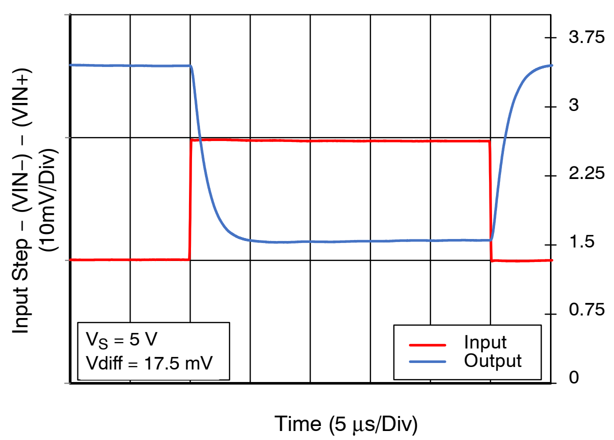


Figure 21c. Small Signal Step Response Inverting, G200

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = (V_{IN+}) − (V_{IN-}), V_S = 5.0 V, V_{IN+} = 12 V, and all gains unless otherwise noted.) (continued)

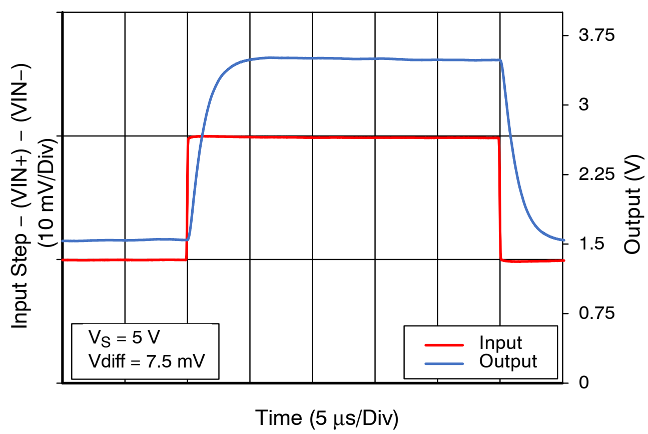


Figure 21d. Small Signal Step Response Non−Inverting, G200

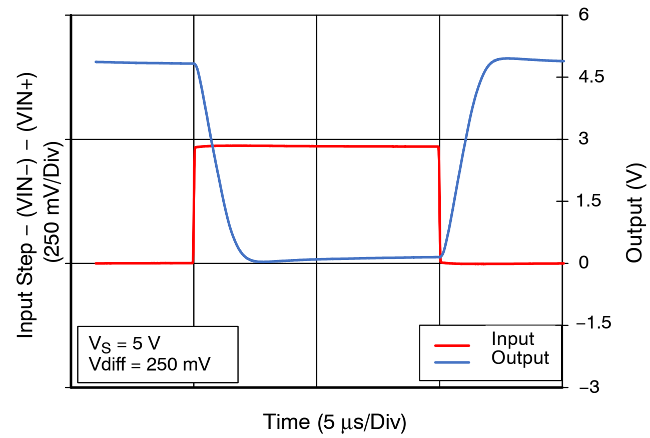


Figure 22a. Large Signal Step Response Inverting, G20

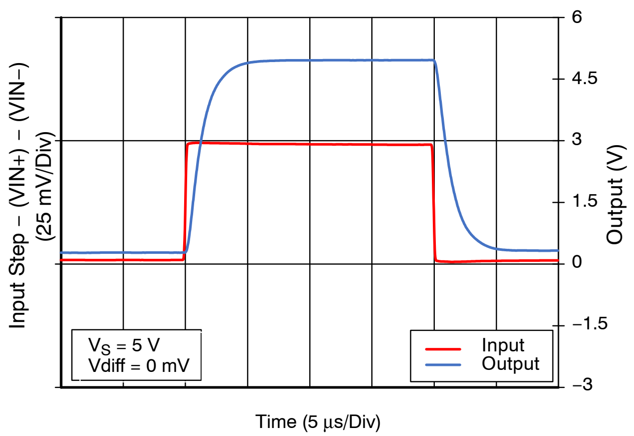


Figure 22b. Large Signal Step Response Non−Inventiring, G20

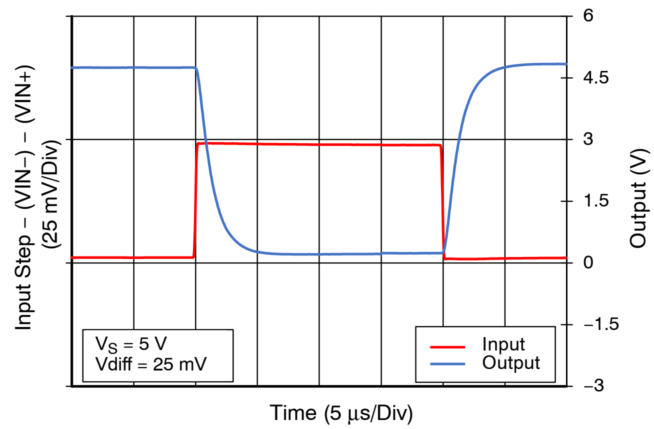


Figure 22c. Small Signal Step Response Inventiring, G200

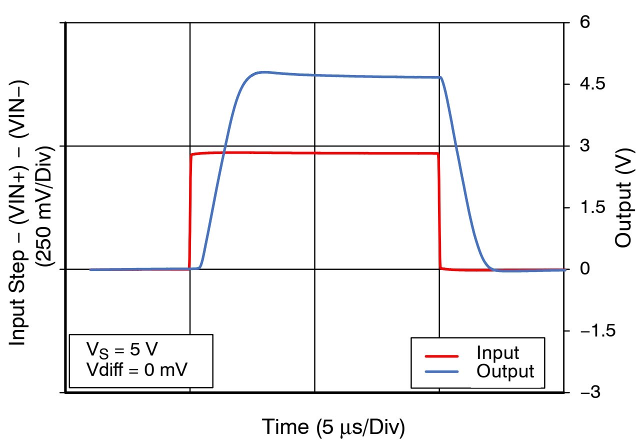


Figure 22d. Large Signal Step Response Non−Inventiring, G200

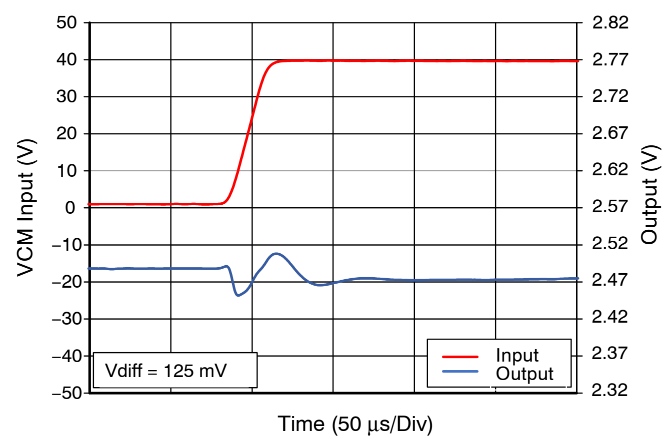


Figure 23a. Common Mode Step Response Rising, G20

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = (V_{IN+}) − ($V_{IN−}$), V_S = 5.0 V, V_{IN+} = 12 V, and all gains unless otherwise noted.) (continued)

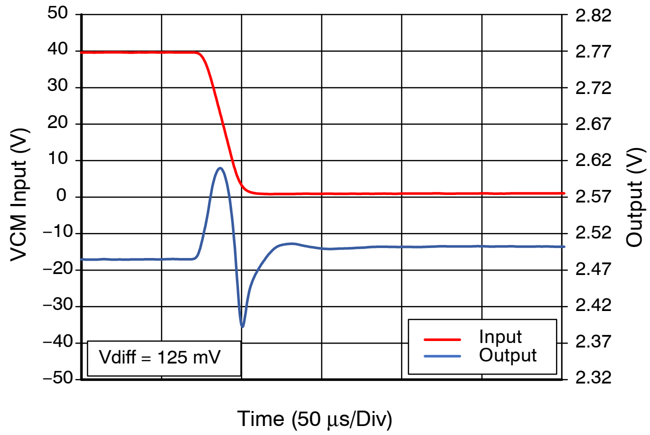


Figure 23b. Common Mode Step Response Falling, G20

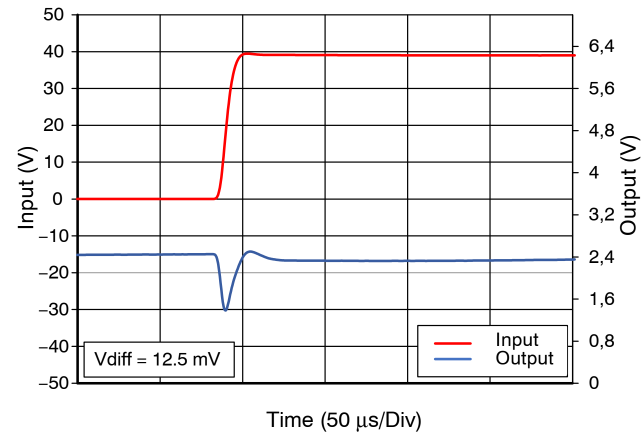


Figure 23c. Common Mode Step Response Rising, G200

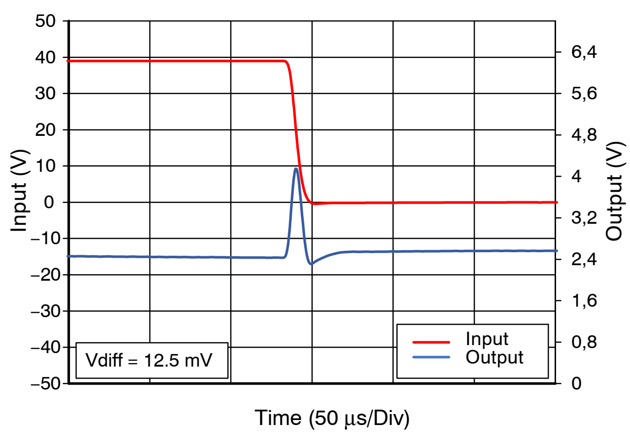


Figure 23d. Common Mode Step Response Rising, G200

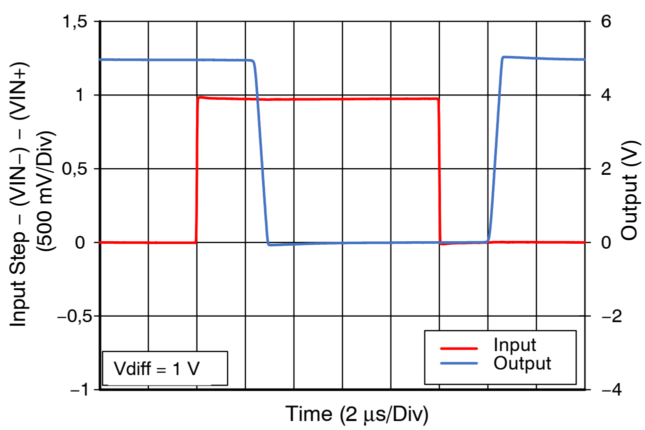


Figure 24a. Overload Response Inverting, G100

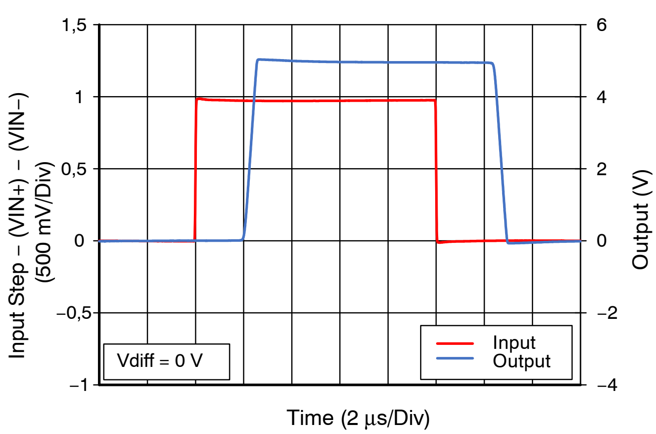


Figure 24b. Overload Response Non−Inverting, G100

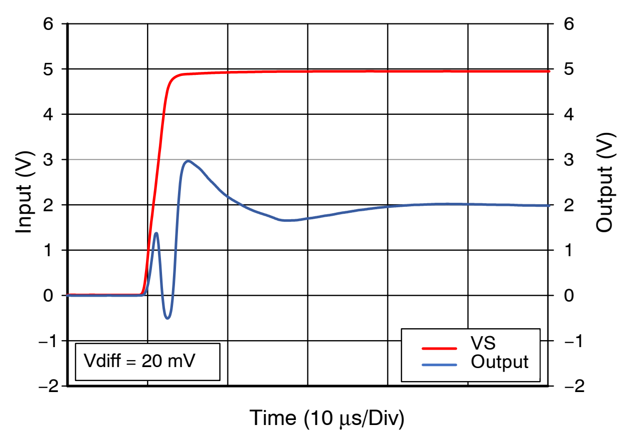


Figure 25a. Startup Response, G100

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = (V_{IN+}) − ($V_{IN−}$), V_S = 5.0 V, V_{IN}+ = 12 V, and all gains unless otherwise noted.) (continued)

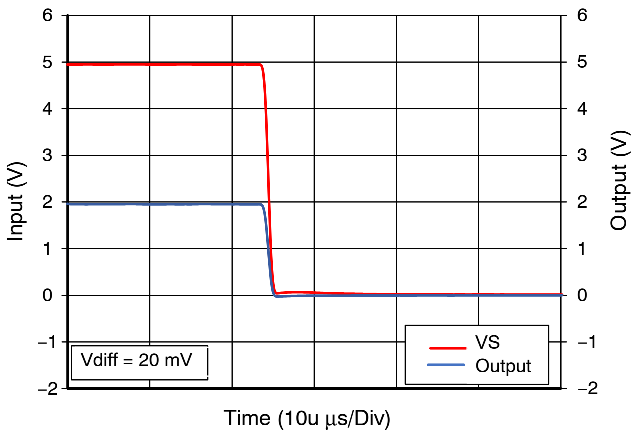


Figure 25b. Shutdown Response, G100

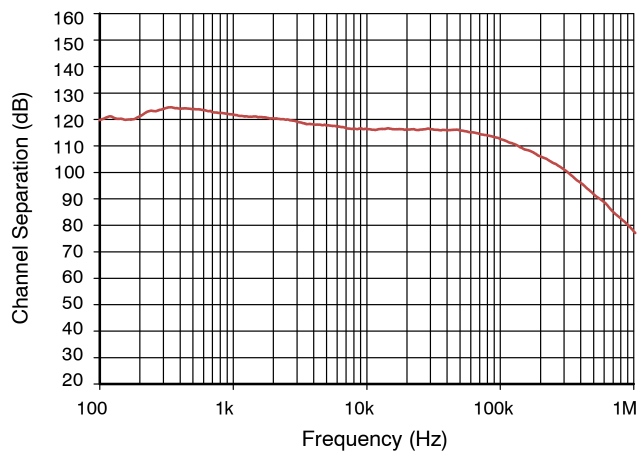


Figure 26. Channel Separation, G 200

APPLICATION INFORMATION

Current Sensing Techniques

NCS(V)21673 and NCS(V)21674 are current sense amplifiers featuring a wide common mode voltage range that spans from −0.1 V to −40 V independent of the supply voltage. These amplifiers can be configured for low−side and high−side current sensing.

Unidirectional Operation

In unidirectional current sensing, the measured load current always flows in the same direction. Common applications for unidirectional operation include power supplies and load current monitoring. In this configuration, the IN+ pin should be connected to the high side of the sense resistor, while the IN− pin should be connected to the low side of the sense resistor.

Input Filtering

As shunt resistors decrease in value, shunt inductance can significantly affect frequency response. At values below 1 m, the shunt inductance causes a zero in the transfer function that often results in corner frequencies in the low 100's of kHz. This inductance increases the amplitude of high frequency spike transient events on the current sensing line that can overload the front end of any shunt current sensing IC. This problem must be solved by external filtering at the input of the amplifier. Note that all current sensing IC's are vulnerable to this problem, regardless of manufacturer claims. Filtering is required at the input of the device to resolve this problem, even if the spike frequencies are above the rated −3 dB bandwidth of the device.

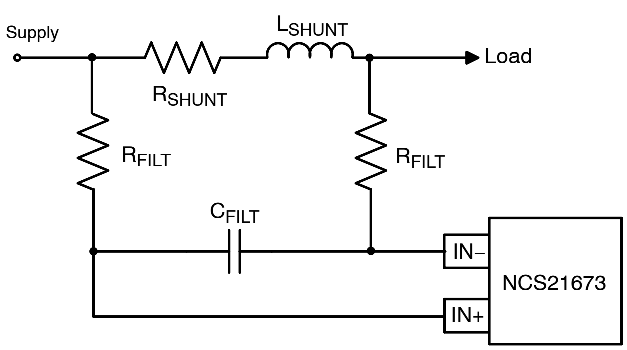


Figure 27.

Ideally, select the capacitor to exactly match the time constant of the shunt resistor and its inductance; alternatively, select the capacitor to provide a pole below that point. Make the input filter time constant equal to or larger than the shunt and its inductance time constant:

$$Freq_{Zero} = 2\pi R_{Shunt} L_{Shunt} \quad \text{(eq. 1)}$$

$$Freq_{Pole} = \frac{1}{2\pi(2R_{Filt})C_{Filt}} \quad \text{(eq. 2)}$$

While this time constant can be the product of any RFILT and C_{FILT} values, the designer needs to take into account that the RFILT resistors are connected in series with the internal feedback resistors R3 and R4, hence changing the amplifier's overall gain. Also, the Opamp's input (IIB) currents create a voltage drop across the filtering resistors, which is added to the differential voltage presented to the Opamp's inputs. This voltage is gained by the amplifier adding to the overall error. A good practice is to keep the filtering resistors in the range of a few ohms then size the filtering capacitor accordingly.

The zero−drift architecture contains a 250 KHz sampling circuit that can induce aliasing effects on the current signal. It is recommended to add filtering to the input stage that limits the signal bandwidth to <100 KHz for current signals with high ac spectral content.

Selecting the Shunt Resistor

The desired accuracy of the current measurement determines the precision, shunt size, and the resistor value. The larger the resistor value, the more accurate the measurement possible, but a large resistor value also results in greater current loss.

For the most accurate measurements, use four−terminal current sense resistors. They provide two terminals for the current path in the application circuit, and a second pair for the voltage detection path of the sense amplifier. This technique is also known as *Kelvin Sensing*. This ensures that the voltage measured by the sense amplifier is the actual voltage across the resistor and does not include the small resistance of a combined connection. When using non−Kelvin shunts, follow manufacturer recommendations on how to lay out the sensing traces closely.

Gain Options

The gain is set by integrated, precision, ratio−matched resistors. These current sense amplifiers are available in gain options of 20 V/V, 50 V/V, 100 V/V, and 200 V/V. Adding external resistors to adjust the gain can contribute to the overall system error and is not recommended for multiple reasons. First, the series resistor's mismatch increases the overall gain error and temperature coefficient and lowers the CMRR. Second, the IIB flowing through the external resistors change the differential voltage seen by the opamp's input. Finally, while the internal resistors are well matched in terms of ratio, they have a high tolerance in their absolute value so the resulting gain value may not match the expectations.

Shutdown

While the NCS21673/4 series do not include a shutdown feature, a simple MOSFET, power switch, or logic gate can be used to switch off power and eliminate quiescent current. Note that the input pins connected to the shunt resistor will always have a current flow via the input and feedback resistors (total resistance of each leg is always ~ 400 kΩ). If unpowered, common mode voltage will feedthrough the

VIN− terminal to the output which forms a divider with the 400 kΩ.. Vout under unpowered conditions will be:

$$Vout = \frac{VIN\_(Rload)}{400K + (Rload)} \quad \text{(eq. 3)}$$

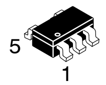
Load resistance to ground should be added to keep Vout within required system limits under this condition.

Also note that when powered, the shunt input pins will exhibit the specified and well−matched bias current. The shunt input pins support the rated common mode voltage when the power is not applied

ORDERING INFORMATION

Device	Channels	Package	Gain	OPN	Marking	Shipping†
INDUSTRIAL AND CONSUMER						
NCS21673	Single	TSOP−5	20	NCS21673SN2G020T1G**	TBD	Tape and Reel 3000 / Reel
			50	NCS21673SN2G050T1G**	TBD	
			100	NCS21673SN2G100T1G**	TBD	
			200	NCS21673SN2G200T1G**	TBD	
NCS21674	Dual	Micro8	20	NCS21674DMG020R2G**	G020	Tape and Reel 4000 / Reel
			50	NCS21674DMG050R2G	G050	
			100	NCS21674DMG100R2G	G100	
			200	NCS21674DMG200R2G	G200	
AUTOMOTIVE QUALIFIED						
NCV21673*	Single	TSOP−5	20	NCV21673SN2G020T1G**	TBD	Tape and Reel 3000 / Reel
			50	NCV21673SN2G050T1G**	TBD	
			100	NCV21673SN2G100T1G**	TBD	
			200	NCV21673SN2G200T1G**	TBD	
NCV21674*	Dual	Micro8	20	NCV21674DMG020R2G**	G020	Tape and Reel 4000 / Reel
			50	NCV21674DMG050R2G	G050	
			100	NCV21674DMG100R2G	G100	
			200	NCV21674DMG200R2G	G200	

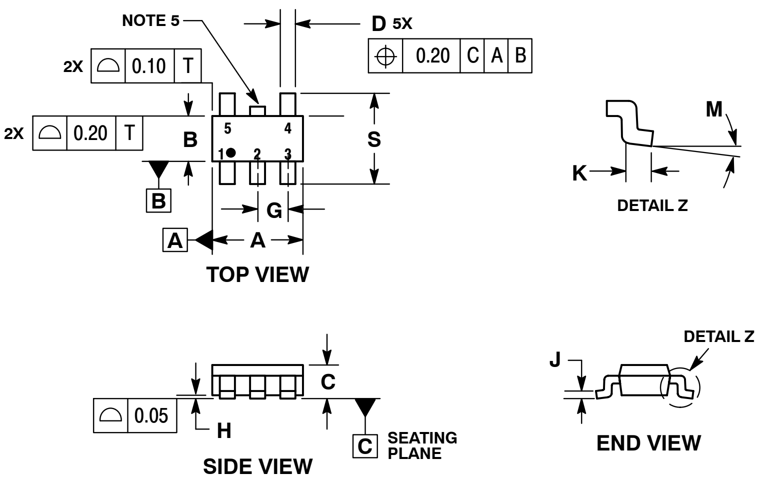
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
**In Development / Consult Sales



SCALE 2:1

TSOP−5
CASE 483
ISSUE N

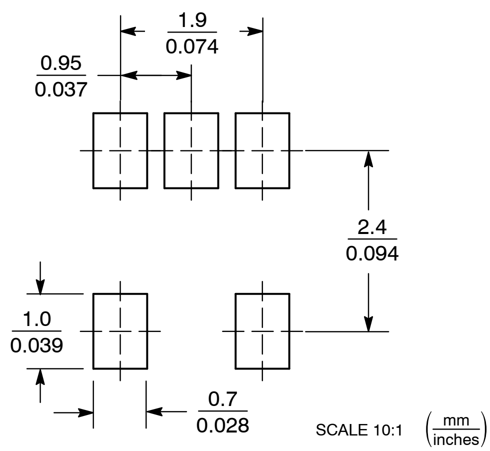
DATE 12 AUG 2020



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

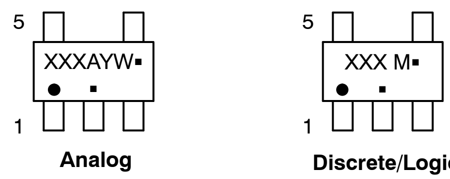
	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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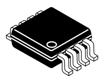
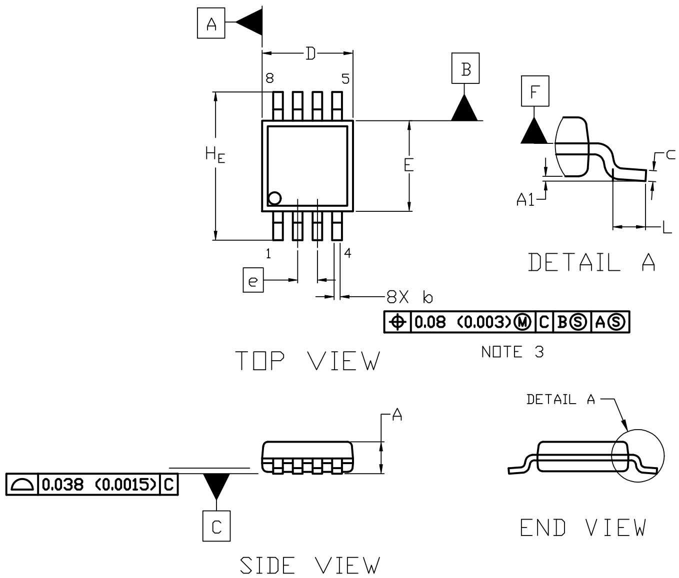


SCALE 2:1

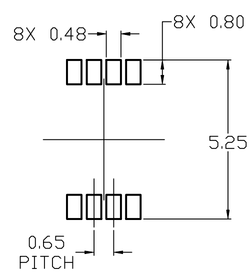
Micro8
CASE 846A−02
ISSUE K

DATE 16 JUL 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

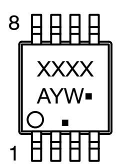


RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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