650V N-Channel MOSFET

## General Description

The 4N65 have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications.

## Product Summary

| BVDSS | RDSON | ID |
|---|---|---|
| 650V | 2.6 Ω | 4A |

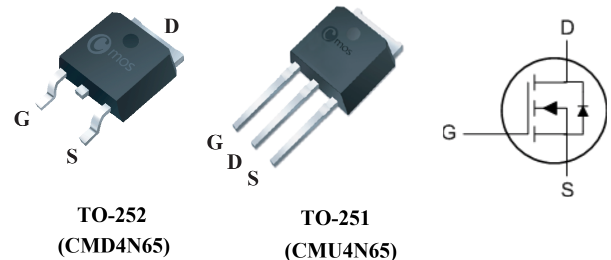
## Applications

- Power Supply
- PFC
- Ballast

## Features

- 4.0A, 650V, RDS (on) = 2.6 Ω @VGS = 10 V
- 100% Avalanche Tested
- Improved dv/dt capability

## TO-252/251 Pin Configuration




TO-252 (CMD4N65)

TO-251 (CMU4N65)

## Absolute Maximum Ratings

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 650 | V |
| $I_D$ | Drain Current - Continuous ($T_C$ = 25°C) [1] | 4 | A |
| | - Continuous ($T_C$ = 100°C) [1] | 2.6 | A |
| $I_{DM}$ | Drain Current - Pulsed [2] | 12 | A |
| $V_{GSS}$ | Gate-Source Voltage | ± 30 | V |
| $I_{AR}$ | Avalanche Current | 4 | A |
| $P_D$ | Power Dissipation ($T_C$ = 25°C) [3] | 60 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | -25 to +150 | °C |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8 from case for 5 seconds | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case Max. [1] | 2 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient Max. (Steady State) [1] | 62 | °C/W |

## Electrical Characteristic

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 650 | -- | -- | V |
| $\triangle BV_{DSS}$ / $\triangle T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 1mA , Referenced to 25°C | -- | 0.69 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 650 V, $V_{GS}$ = 0 V | -- | -- | 10 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 2.5 | -- | 4.5 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 2A | -- | -- | 2.6 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 15 V, $I_D$ =2A | -- | 3 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 800 | -- | pF |
| $C_{oss}$ | Output Capacitance | | -- | 60 | -- | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 4 | -- | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 300 V , $V_{GS}$=10V, $I_D$ = 1A, $R_G$ = 10Ω | -- | 15 | -- | ns |
| $t_r$ | Turn-On Rise Time | | -- | 20 | -- | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 30 | -- | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 30 | -- | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 520V, $I_D$ = 1A, $V_{GS}$ = 10 V | -- | 18 | -- | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 5 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 6 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current [1,4] | | -- | -- | 4 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current [2,4] | | -- | -- | 12 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1A [2] | -- | -- | 1 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 1A, dI / dt = 100 A/μs | -- | 200 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 580 | -- | nC |

Notes:
1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3.The power dissipation is limited by 150℃ junction temperature.
4.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

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