

CMP65R280Q/CMB65R280Q/CMI65R280Q/CMF65R280Q

General Description

The 65R280Q is power MOSFET using Cmos's advanced super junction technology that can realize very low on resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of low EMI to designers as well as low switching loss.

N-Channel Super Junction Power MOSFET

Product Summary

BVDSS	RDSON	ID
650V	0.3Ω	14A

Applications

- Charger
- Adaptor
- Power Supply

TO-220/263/262/220F Pin Configuration

Features

- Fast switching
- 100% avalanche tested
- RoHS Compliant

Absolute Maximum Ratings

				D
G D S	GSS	G D S	GDS	
TO-220 (CMP65R280Q)	TO-263 (CMB65R280Q)	TO-262 (CMI65R280Q)	TO-220F (CMF65R280Q)	s s

Symbol	Parameter		220/263/262	220F	Units
V _{DS}	Drain-Source Voltage		650		V
V _{GS}	Gate-Source Voltage		±30		V
I _D @T _C =25℃	Continuous Drain Current		14	14*	А
I _D @T _C =100℃	Continuous Drain Current		9	9*	А
I _{DM}	Pulsed Drain Current (Note 1)		56	56*	А
EAS	single Pulse Avalanche Energy (۴	Note 2)	400		mJ
P₀@T₀=25℃	Total Power Dissipation		105	35	W
T _{STG}	Storage Temperature Range		-55 to 150		°C
TJ	Operating Junction Temperature Range		150		°C

Thermal Data

Symbol	Parameter		220/263/262	220F	Unit
R _{θJA}	Thermal Resistance Junction-ambient	(Note 3,4)	62	80	°C/W
R _{eJC}	Thermal Resistance Junction-case		1.2	3.9	°C/W



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Electrical Characteristics (T_J=25 $^\circ\!\!\mathbb{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	650			V	
R _{DS(ON)}	Static Drain-Source On-Resistance	V_{GS} =10V , I_{D} =4.4A			0.3	Ω	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS} , I_D =250uA	2		4	V	
	Drain Source Lookage Current	V _{DS} =650V , V _{GS} =0V, T _j =25℃			1		
I _{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}\text{=}650\text{V}$, $~V_{\text{GS}}\text{=}0\text{V}$, T_{j} =150 $^{\circ}\text{C}$		10		- uA	
I _{GSS}	Gate-Source Leakage Current	V_{GS} = ±30V , V_{DS} =0V			±100	nA	
gfs	Forward Transconductance	V _{DS} =20V, I _D =4.4A		9.5		S	
R _g	Gate Resistance	V_{DS} =0V , V_{GS} =0V , f=1MHz		21		Ω	
Qg	Total Gate Charge	I _D =14A		30			
Q_gs	Gate-Source Charge	V _{DD} =520V		7.1		nC	
Q_gd	Gate-Drain Charge	V _{GS} =10V		10			
T _{d(on)}	Turn-On Delay Time	V _{DD} =325V		25			
Tr	Rise Time	Vgs = 10V		60		ns	
T _{d(off)}	Turn-Off Delay Time	I _D =14A		150		115	
T _f	Fall Time	R _G =25Ω		52			
C _{iss}	Input Capacitance			1050			
C _{oss}	Output Capacitance	$V_{\text{DS}}\text{=}25V$, $V_{\text{GS}}\text{=}0V$, f=1MHz		1200		pF	
C _{rss}	Reverse Transfer Capacitance			50			

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
ls	Continuous Source Current	V _G =V _D =0V , Force Current			14	А
I _{SM}	Pulsed Source Current	VG-VD-OV, FOICe Cullent			56	А
V _{SD}	Diode Forward Voltage	V _{GS} =0V , I _S =13.8A			1.2	V

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.

2. The EAS data shows Max. rating . The test condition is $V_{\text{DS}}\text{=}50V$, $V_{\text{GS}}\text{=}10V$, L=20mH , I_{\text{AS}}\text{=}6.4A.

3. The value of ReJA is measured with the device in a still air environment with TA=25 $^\circ\!\mathrm{C}.$

4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

This product has been designed and qualified for the counsumer market.

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Cmos reserver the right to improve product design ,functions and reliability wihtout notice.