

CMP4N65/CMB4N65/CMF4N65

650V N-Channel MOSFET

General Description

The 4N65 have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications.

Features

- 4.0A, 650V, RDS (on) = 2.6 Ω @VGS = 10 V
- 100% Avalanche Tested
- Improved dv/dt capability

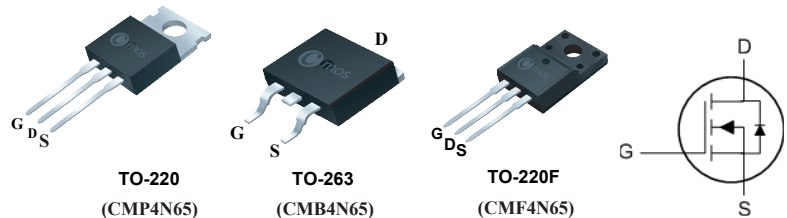
Product Summary

BVDSS	RDSON	ID
650V	2.6 Ω	4A

Applications

- Power Supply
- PFC
- Ballast

TO-220/263/220F Pin Configuration



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	220/263	220F	Units
V_{DSS}	Drain-Source Voltage	650		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) ¹	4	4*	A
		2.6	2.6*	A
I_{DM}	Drain Current - Pulsed ²	12	12*	A
V_{GSS}	Gate-Source Voltage	± 30		V
I_{AR}	Avalanche Current	4	4*	A
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) ³	100	33	W
T_J, T_{STG}	Operating and Storage Temperature Range	-25 to +150		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	220/263	220F	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case Max. ¹	1.2	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Max. (Steady State) ¹	62	62	°C/W

Electrical Characteristic

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	650	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$, Referenced to 25°C	--	0.69	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.5	--	4.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2\text{ A}$	--	--	2.6	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 2\text{ A}$	--	3	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$	--	800	--	pF
C_{oss}	Output Capacitance		$V_{GS} = 0\text{ V}$	--	60	--
C_{rss}	Reverse Transfer Capacitance	$f = 1.0\text{ MHz}$	--	4	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, V_{GS} = 10\text{ V}$ $I_D = 1\text{ A}$ $R_G = 10\ \Omega$	--	15	--	ns
t_r	Turn-On Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	30	--	ns
t_f	Turn-Off Fall Time		--	30	--	ns
Q_g	Total Gate Charge	$V_{DS} = 520\text{ V}$ $I_D = 1\text{ A}$ $V_{GS} = 10\text{ V}$	--	18	--	nC
Q_{gs}	Gate-Source Charge		--	5	--	nC
Q_{gd}	Gate-Drain Charge		--	6	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current ^{1,4}	--	--	4	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current ^{2,4}	--	--	12	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1\text{ A}$ ²	--	--	1	V
t_{rr}	Reverse Recovery Time	$I_F = 1\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$	--	200	--	ns
Q_{rr}	Reverse Recovery Charge		--	580	--	nC

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- The power dissipation is limited by 150°C junction temperature.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

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