

FEATURES

- Ultra-low Noise
- Ultra-Fast Response in Line/Load Transient
- 0.01 μ A Standby Current When Shutdown
- Low Dropout: 205mV@300mA
- Wide Operating Voltage Ranges: 2.2V to 6V
- Low Temperature Coefficient
- Current Limiting Protection
- Thermal Shutdown Protection
- Only 1 μ F Output Capacitor Required for Stability
- High Power Supply Rejection Ratio
- Fast output discharge
- Available in SOT23-5, SOT23-3, SC70-5 and DFN1 \times 1-4L Package

- Hand-Held Instruments
- PCMCIA Cards
- MP3/MP4/MP5 Players
- Portable Information Appliances

DESCRIPTION

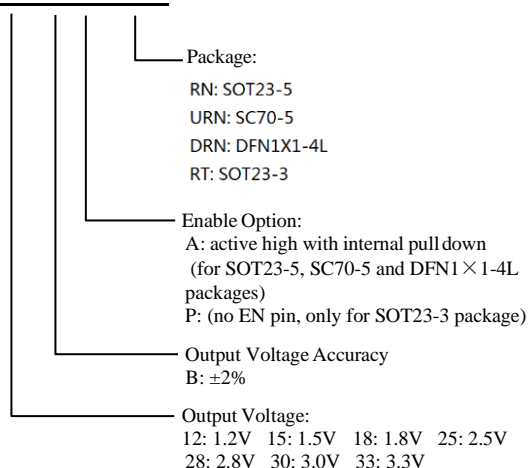
The BL9161G is designed for portable applications with demanding performance and space requirements. The BL9161G performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The BL9161G also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The BL9161G consumes only 0.01 μ A current in shutdown mode and has fast turn-on time (Typical 50 μ s). The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio.

APPLICATIONS

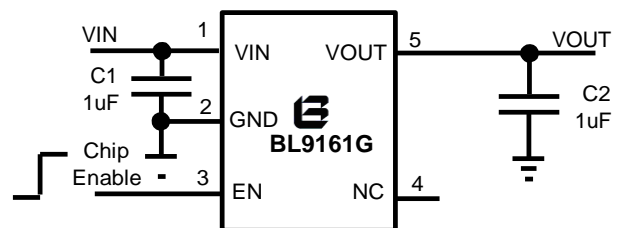
- Cellular and Smart Phones
- Cordless Telephones
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers

ORDERING INFORMATION

BL9161G XX X X XXX



TYPICAL APPLICATION



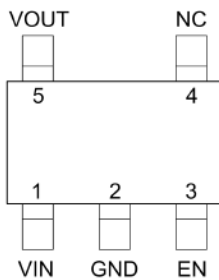
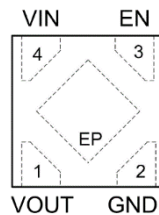
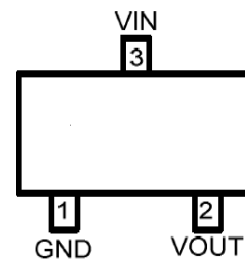
Application hints:

Output capacitor ($C2 \geq 2.2\mu$ F) is recommended in BL9161G-1.2V, BL9161G-1.5V and BL9161G-1.8V application to assure the stability of circuit.

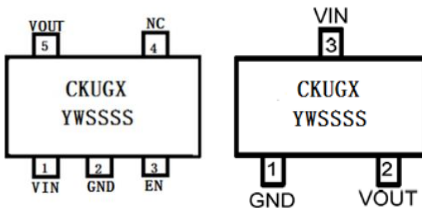
Absolute Maximum Rating (Note 1)

| | | | |
|----------------------------|-------------------|--|----------------|
| Input Supply Voltage (VIN) | -0.3V to +6V | Maximum Junction Temperature | 150°C |
| EN Pin Input Voltage | -0.3V to VIN | Operating Temperature Range <small>(Note2)</small> | -40°C to 85°C |
| Output Voltages | -0.3V to VIN+0.3V | Storage Temperature Range | -65°C to 125°C |
| Output Current | 300mA | Lead Temperature (Soldering, 10s) | 300°C |

PIN CONFIGURATIONS

SOT23-5 & SC70-5 (TOP VIEW)

DFN1X1-4L (TOP VIEW)

SOT23-3 (TOP VIEW)


Package Marking

SOT23-5 & SC70-5
SOT23-3


CKUG: Chip ID
 X: Output voltage
 Y: Data code—Year
 W: Data code—Week

DFN1 × 1-4L


G: Chip ID
 X: Output voltage
 W: Data code—Week

Thermal Resistance (Note3):

| Package | θ_{JA} | θ_{JC} |
|---------|---------------|---------------|
| SOT23-5 | 250°C/W | 130°C/W |
| SC70-5 | 333°C/W | 170°C/W |

| Output voltage | 1.2V | 1.5V | 1.8V | 2.5V | 2.8V | 3.0V | 3.3V |
|-----------------------------|------|------|------|------|------|------|------|
| X(SOT23-5, SOT23-3& SC70-5) | B | C | D | E | G | I | K |
| X(DFN1 × 1-4L) | B | C | D | E | G | I | K |

| Y | 4 | 5 | 6 | ... | 0 | 1 | ... |
|------|------|------|------|-----|------|------|-----|
| Year | 2014 | 2015 | 2016 | ... | 2020 | 2021 | ... |

| W | A | ... | Y | Z | a | ... | y | z |
|------|---|-----|----|----|----|-----|----|----|
| Week | 1 | ... | 25 | 26 | 27 | ... | 51 | 52 |

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The BL9161G is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Thermal Resistance is specified with approximately 1 square of 1 oz copper.

Pin Description

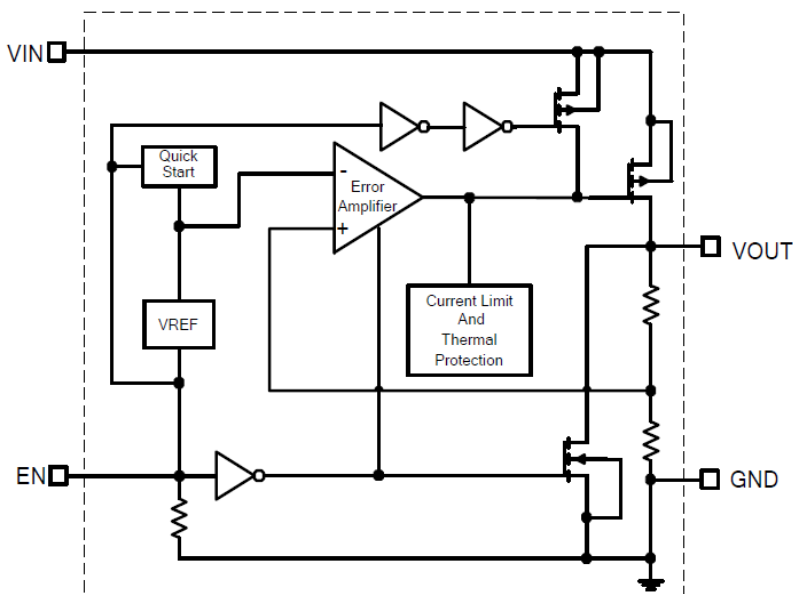
SOT23-5 , SC70-5 & SOT23-3

| PIN | | NAME | FUNCTION |
|------------------|---------|------|--|
| SOT23-5 & SC70-5 | SOT23-3 | | |
| 1 | 3 | VIN | Power Input Voltage. |
| 2 | 1 | GND | Ground. |
| 3 | | EN | Chip Enable Pin, This pin has an internal pull-down resistor |
| 4 | | NC | No Connection. |
| 5 | 2 | VOUT | Output Voltage. |

DFN1X1-4L

| PIN | NAME | FUNCTION |
|-------------|------|--|
| 1 | VOUT | Output Voltage. |
| 2 | GND | Ground. |
| 3 | EN | Chip Enable Pin, This pin has an internal pull-down resistor |
| 4 | VIN | Power Input Voltage. |
| Exposed Pad | | The exposed pad should be connected to a large ground plane to maximize thermal performance. |

Block Diagram



Electrical Characteristics (Note 4)

($V_{IN}=V_{OUT}+1V$, $EN=V_{IN}$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, unless otherwise noted.)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | unit |
|--|-------------------|---|----------------------------------|----------|------|-----------------|
| Input Voltage | V_{IN} | | 2.2 | | 6 | V |
| Output Voltage Accuracy | ΔV_{OUT} | $V_{IN}=V_{OUT}+1V$, $I_{OUT}=1mA$ | -2 | | +2 | % |
| Current Limit | I_{LIM} | $R_{LOAD}=1\Omega$ | 360 | 450 | | mA |
| Quiescent Current | I_Q | $V_{EN}>1.2V$, $I_{OUT}=0mA$ | | 70 | 110 | μA |
| Dropout Voltage | V_{DROP} | $I_{OUT}=200mA$, $V_{OUT}=3.3V$ | | 135 | 200 | mV |
| | | $I_{OUT}=300mA$, $V_{OUT}=3.3V$ | | 205 | 300 | |
| Line Regulation (Note 5) | ΔV_{LINE} | $V_{IN}=V_{OUT}+1V$ to 5.5V $I_{OUT}=1mA$ | | 0.02 | 0.17 | %/V |
| Load Regulation (Note 6) | ΔV_{LOAD} | $1mA < I_{OUT} < 300mA$ | | 20 | | mV |
| Output Voltage (Note 7) Temperature Coefficient | $TC_{V_{OUT}}$ | $I_{OUT}=1mA$ | | ± 60 | | ppm/ $^\circ C$ |
| Standby Current | I_{STBY} | $V_{EN}=GND$, Shutdown | | 0.01 | 1 | μA |
| EN Input Bias Current | I_{IBSD} | $V_{EN}=GND$ or V_{IN} | | | 2 | μA |
| EN Input Threshold | Logic Low | V_{IL} | $V_{IN}=3V$ to 5.5V, Shutdown | | 0.4 | V |
| | Logic High | V_{IH} | $V_{IN}=3V$ to 5.5V, Start up | 1.2 | | V |
| Output Noise Voltage | e_{NO} | 10Hz to 100KHz, $I_{OUT}=100mA$ | | 180 | | μV_{RMS} |
| Power Supply Rejection Ratio | $f=217Hz$ | PSRR | $I_{OUT}=10mA$ | | -75 | dB |
| | $f=1KHz$ | | | | -71 | |
| | $f=10KHz$ | | | | -55 | |
| Thermal Shutdown Temperature | T_{SD} | Shutdown, Temp increasing | | 170 | | $^\circ C$ |
| Thermal Shutdown Hysteresis | T_{SDHY} | | | 30 | | $^\circ C$ |

Note 4: Production test at $+25^\circ C$. Specifications over the temperature range are guaranteed by design and characterization.

Note 5: Line regulation is calculated by $\Delta V_{LINE} = \left| \frac{V_{OUT1} - V_{OUT2}}{\Delta V_{IN} \times V_{OUT(normal)}} \right| \times 100$

Where V_{OUT1} is the output voltage when $V_{IN}=5.5V$, and V_{OUT2} is the output voltage when $V_{IN}=4.3V$,
 $\Delta V_{IN}=1.2V$. $V_{OUT(normal)}=3.3V$.

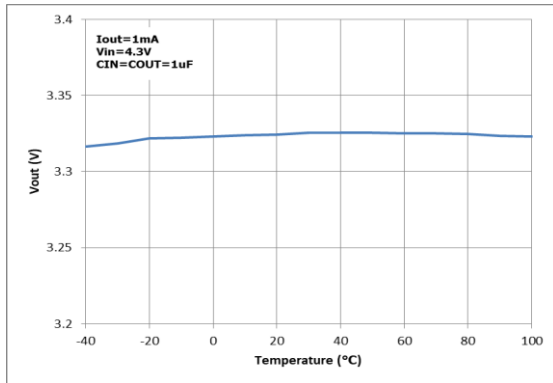
Note 6: Load regulation is calculated by $V_{load}=V_{out1}-V_{out2}$

Where V_{OUT1} is the output voltage when $I_{OUT}=1mA$, and V_{OUT2} is the output voltage when $I_{OUT}=300mA$.

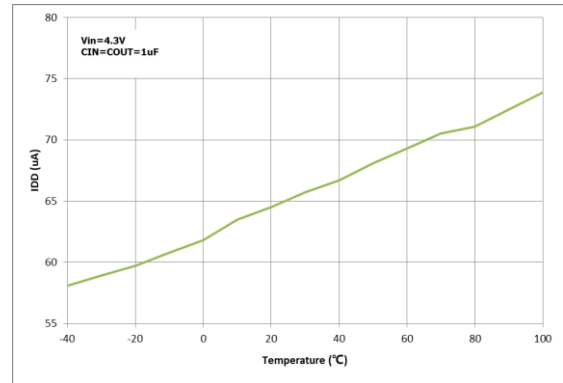
Note 7: The temperature coefficient is calculated by $TC_{V_{OUT}} = \frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$

Typical Performance Characteristics

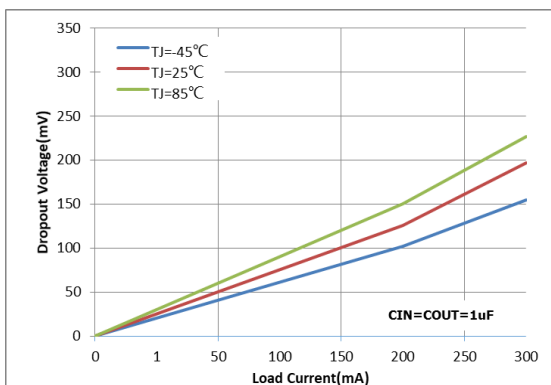
Output Voltage Vs. Temperature



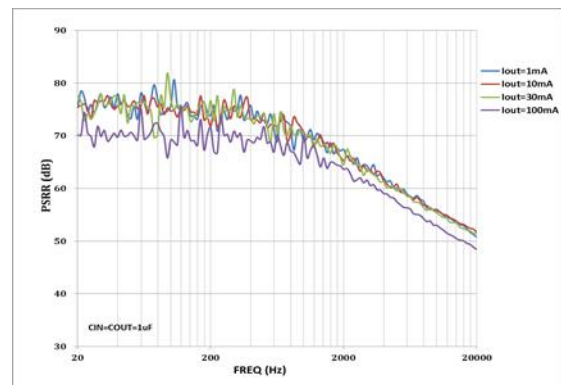
Quiescent Current Vs. Temperature



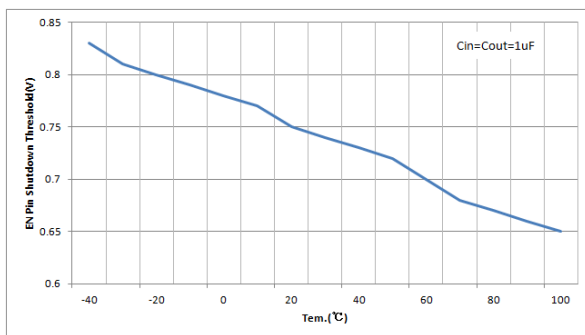
Dropout Voltage Vs. Load Current



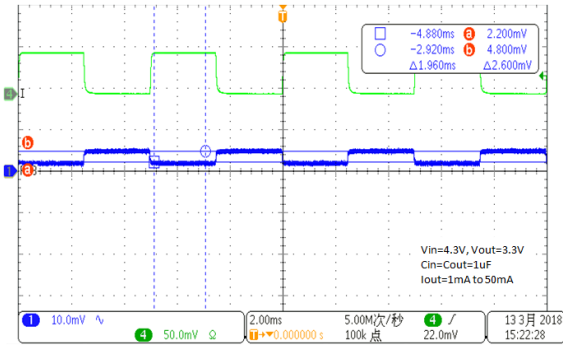
PSRR



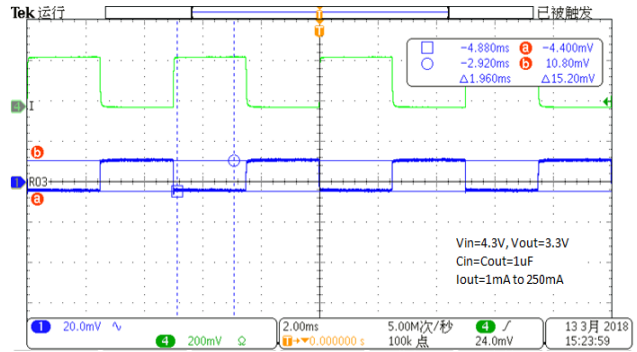
EN Pin Shutdown Threshold Vs. Temperature



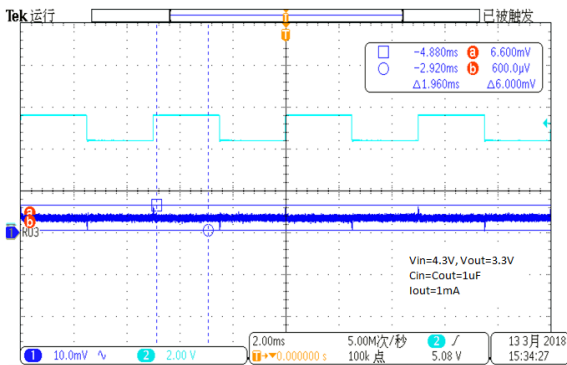
Load Transient Response



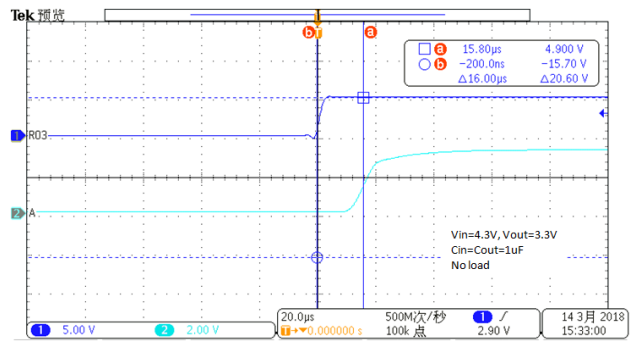
Load Transient Response



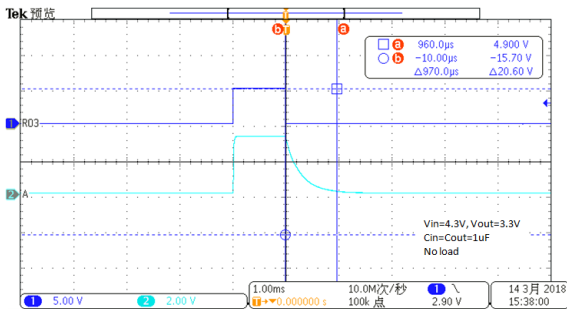
Line transient Response



Start up



EN Pin Shutdown Response



Applications Information

Like any low-dropout regulator, the external capacitors used with the BL9161G must be carefully selected for regulator stability and performance. Using a capacitor whose value is $> 1\mu\text{F}$ on the BL9161G input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The BL9161G is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least $1\mu\text{F}$ with ESR is $> 25\text{m}\Omega$ on the BL9161G output ensures stability. The BL9161G still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the V_{OUT} pin of the BL9161G and returned to a clean analog ground.

Enable Function

The BL9161G features an LDO regulator enable/disable function. To assure the LDO regulator will switch on; the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shut-

down mode when the voltage on the EN pin falls below 0.4 volts. For to protect the system, the BL9161G have a quick discharge function. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in BL9161G. When the operation junction temperature exceeds 170°C , the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 30°C .

For continue operation, do not exceed absolute maximum operation junction temperature 125°C . The power dissipation definition in device is:

$$P_{\text{D}}(\text{MAX}) = (T_{\text{J}}(\text{MAX}) - T_{\text{A}}) / \theta_{\text{JA}}$$

Where $T_{\text{J}}(\text{MAX})$ is the maximum operation junction temperature 125°C , T_{A} is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of BL9161G, where $T_{\text{J}}(\text{MAX})$ is the maximum junction temperature of the die (125°C) and T_{A} is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOT-23-5 package is $250^{\circ}\text{C}/\text{W}$, on standard JEDEC 51-3 thermal test board. The maximum power dissipation at $T_{\text{A}} = 25^{\circ}\text{C}$ can be calculated by following formula:

$$P_D(\text{MAX}) = (125^\circ\text{C} - 25^\circ\text{C}) / 250 = 400\text{mW}$$

(SOT-23-5)

The maximum power dissipation depends on operating ambient temperature for fixed $T_J(\text{MAX})$ and thermal resistance θ_{JA} . It is also useful to calculate the junction of temperature of the BL9161G under a set of specific conditions. In this example let the input voltage $V_{IN}=3.3\text{V}$, the output current $I_O=300\text{mA}$ and the case temperature $T_A=40^\circ\text{C}$ measured by a thermal couple during operation. The power dissipation for the $V_{OUT}=2.8\text{V}$ version of the BL9161G can be calculated as:

$$P_D = (3.3\text{V} - 2.8\text{V}) \times 300\text{mA} + 3.6\text{V} \times 100\mu\text{A}$$
$$= 150\text{mW}$$

And the junction temperature, T_J , can be calculated as follows:

$$T_J = T_A + P_D \times \theta_{JA} = 40^\circ\text{C} + 0.15\text{W} \times 250^\circ\text{C}/\text{W}$$
$$= 40^\circ\text{C} + 37.5^\circ\text{C} = 77.5^\circ\text{C} < T_J(\text{MAX}) = 125^\circ\text{C}$$

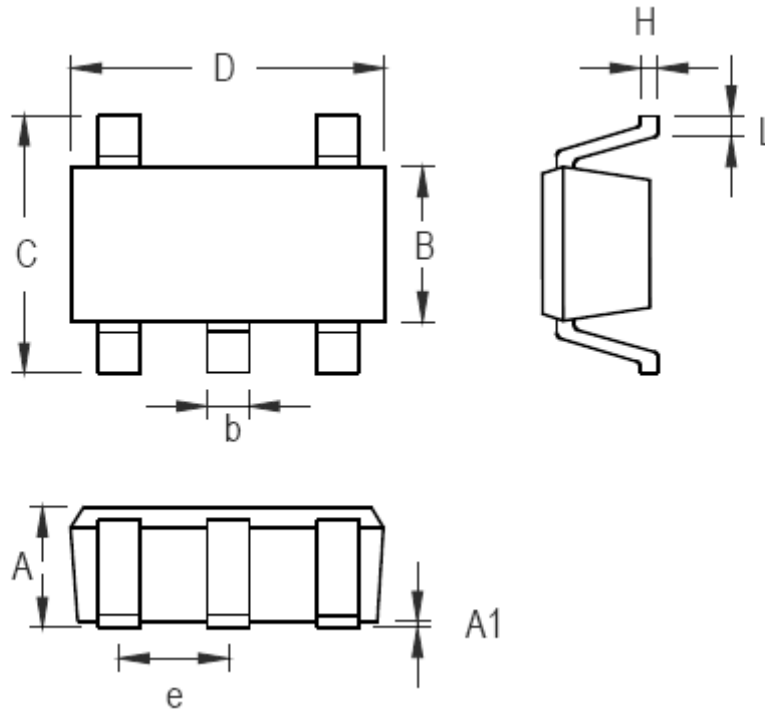
For this operating condition, T_J is lower than the absolute maximum operating junction temperature, 125°C , so it is safe to use the BL9161G in this configuration.

Layout considerations

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device.

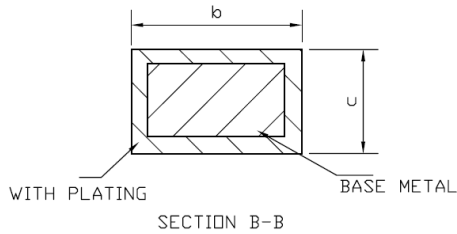
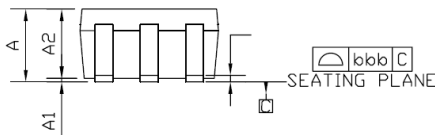
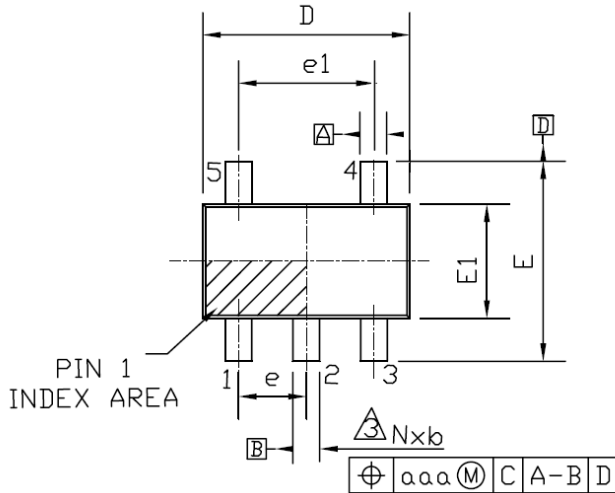
Package Description

SOT23-5

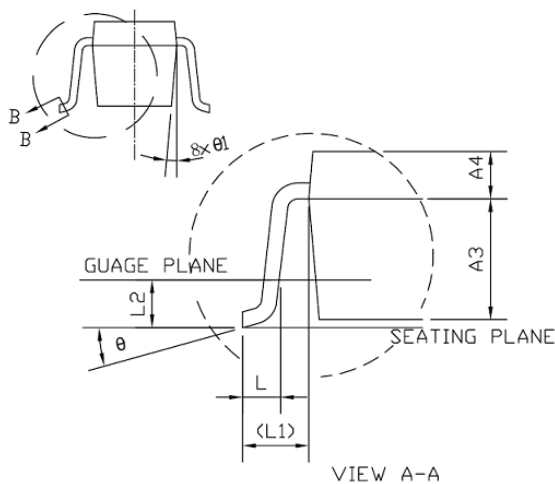


| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.889 | 1.295 | 0.035 | 0.051 |
| A1 | 0.000 | 0.152 | 0.000 | 0.006 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.356 | 0.559 | 0.014 | 0.022 |
| C | 2.591 | 2.997 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| e | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

SC70-5

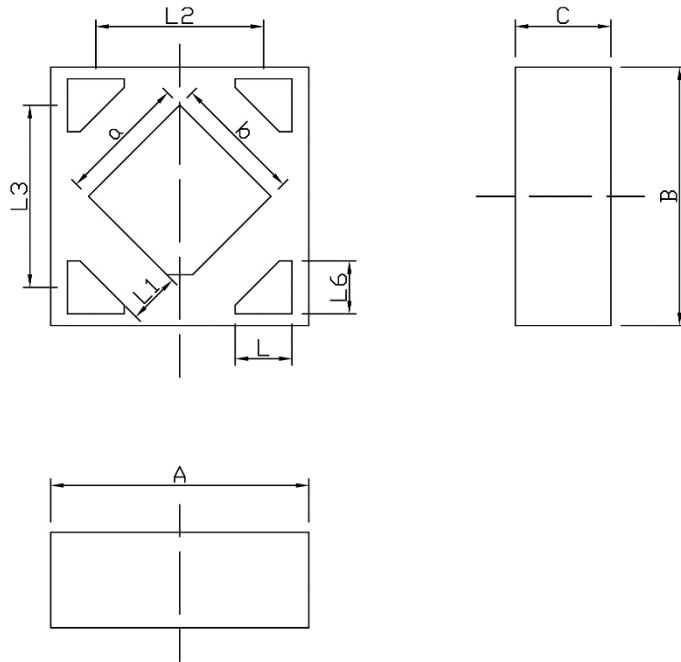


SEE VIEW A-A



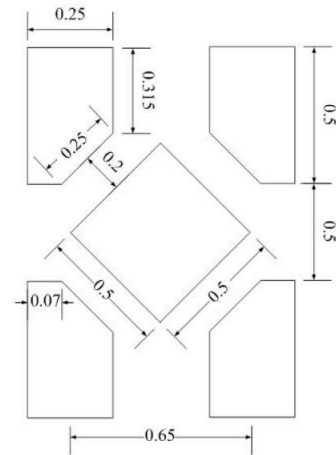
| SYMBOL | IN MILLIMETERS | | |
|------------|----------------|-------|------|
| | MIN | NOMAL | MAX |
| A | 0.80 | - | 1.10 |
| A1 | 0 | - | 0.10 |
| A2 | 0.80 | 0.90 | 1.00 |
| A3 | 0.47 | 0.52 | 0.57 |
| A4 | 0.33 | 0.38 | 0.43 |
| b | 0.15 | - | 0.30 |
| c | 0.10 | - | 0.25 |
| D | 1.85 | 2.00 | 2.20 |
| e | 0.65 BSC | | |
| e1 | 1.30 BSC | | |
| E | 1.80 | 2.10 | 2.40 |
| E1 | 1.15 | 1.25 | 1.35 |
| L | 0.10 | - | 0.45 |
| L1 | 0.42 REF. | | |
| L2 | 0.20 BSC | | |
| θ | 0° | 4° | 30° |
| θ_1 | 4° | - | 12° |
| aaa | 0.10 | | |
| bbb | 0.10 | | |

DFN1×1-4L



| Dimensions In Millimeter | | | |
|--------------------------|-------|-------|-------|
| Symbol | MIN | TYP | MAX |
| A | 0.950 | 1.000 | 1.050 |
| B | 0.950 | 1.000 | 1.050 |
| C | 0.320 | 0.370 | 0.420 |
| L | 0.170 | 0.220 | 0.270 |
| L1 | 0.140 | 0.190 | 0.240 |
| L2 | 0.600 | 0.650 | 0.700 |
| L3 | 0.625 | 0.675 | 0.725 |
| L6 | 0.175 | 0.225 | 0.275 |
| a | 0.440 | 0.490 | 0.540 |
| b | 0.440 | 0.490 | 0.540 |

There may be slight differences in shape



RECOMMENDED LAND PATTERN (Unit: mm)

SOT23-3

