

## 2-Kbit I<sup>2</sup>C Serial EEPROM with Half-Array Write Protect

### Device Selection Table

| Part Number | Vcc Range | Max. Clock             | Temp. Range | Available Packages |
|-------------|-----------|------------------------|-------------|--------------------|
| 24AA024H    | 1.7V-5.5V | 400 kHz <sup>(1)</sup> | I           | MNY, MS, P, SN, ST |
| 24LC024H    | 2.5V-5.5V | 1 MHz                  | I, E        | MNY, MS, P, SN, ST |

**Note 1:** 100 kHz for Vcc < 1.8V

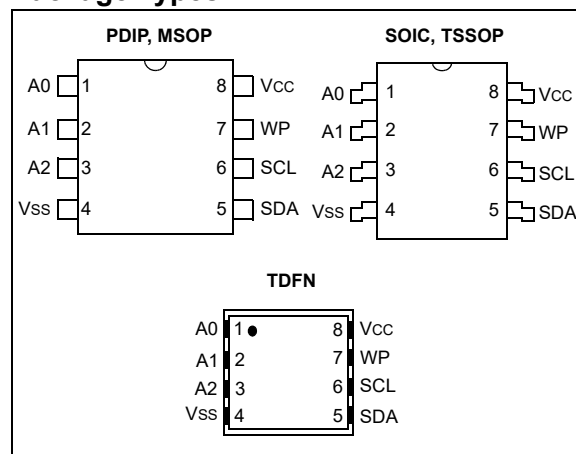
### Features

- Single-Supply with Operation Down to 1.7V for 24AA024H Devices, 2.5V for 24LC024H Devices
- Low-Power CMOS Technology:
  - 400  $\mu$ A active current, max.
  - 1  $\mu$ A standby current, max.
- Organized as a Single Block of 256 Bytes (256 x 8)
- Two-Wire Serial Interface Bus, I<sup>2</sup>C Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Compatibility
- 1 MHz Compatibility (24LC024H Only)
- Page Write Time: 5 ms, Maximum
- Self-Timed Erase/Write Cycle
- 16-Byte Page Write Buffer
- Hardware Write Protection for Half Array (80h-FFh)
- Cascadable up to Eight Devices
- High Reliability:
  - More than one million erase/write cycles
  - Data retention: > 200 Years
  - ESD protection: > 4,000V
- Factory Programming Available
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C

### Description

The Microchip Technology Inc. 24AA024H/24LC024H is a 2-Kbit Serial Electrically Erasable PROM (EEPROM). The device is organized as a single block of 256 x 8-bit memory with a two-wire serial interface. Its low-voltage design permits operation down to 1.7V, with maximum standby and active currents of only 1  $\mu$ A and 400  $\mu$ A, respectively. The device has a page write capability for up to 16 bytes of data. Functional address lines allow the connection of up to eight 24AA024H/24LC024H devices on the same bus for up to 16 Kbits of contiguous EEPROM memory.

### Package Types

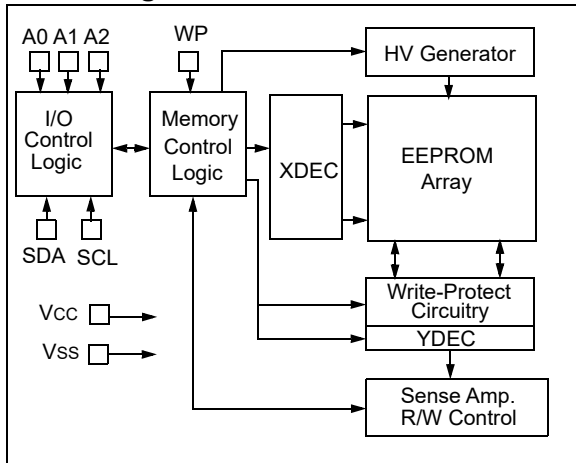


### Packages

- 8-Lead TDFN, 8-Lead MSOP, 8-Lead PDIP, 8-Lead SOIC and 8-Lead TSSOP

# 24AA024H/24LC024H

## Block Diagram



# 24AA024H/24LC024H

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings (†)

|   |                                |
|---|--------------------------------|
| V <sub>CC</sub> .....                               | 6.5V                           |
| All inputs and outputs w.r.t. V <sub>SS</sub> ..... | -0.6V to V <sub>CC</sub> +1.0V |
| Storage temperature.....                            | -65°C to +150°C                |
| Ambient temperature with power applied.....         | -40°C to +125°C                |
| ESD protection on all pins.....                     | ≥ 4 kV                         |

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| DC CHARACTERISTICS |                                       |  | Electrical Characteristics:                     |                     |                                  |  |
|--------------------|---------------------------------------|--|---|---------------------|----------------------------------|--|
|                    |                                       |  | Industrial (I): V <sub>CC</sub> = +1.7V to 5.5V |                     | T <sub>A</sub> = -40°C to +85°C  |  |
|                    |                                       |  | Extended (E): V <sub>CC</sub> = +2.5V to 5.5V   |                     | T <sub>A</sub> = -40°C to +125°C |  |
| Param. No.         | Sym.                                  | Characteristic                                       | Min.  | Max.                | Units                            | Conditions   |
| D1                 | V <sub>IH</sub>                       | High-level input voltage                             | 0.7 V <sub>CC</sub>                             | —                   | V                                | —  |
| D2                 | V <sub>IL</sub>                       | Low-level input voltage                              | —   | 0.3 V <sub>CC</sub> | V                                | —  |
| D3                 | V <sub>HYS</sub>                      | Hysteresis of Schmitt Trigger inputs (SDA, SCL pins) | 0.05 V <sub>CC</sub>                            | —                   | V                                | (Note 1)   |
| D4                 | V <sub>OL</sub>                       | Low-level output voltage                             | —   | 0.40                | V                                | I <sub>OL</sub> = 3.0 ma @ V <sub>CC</sub> = 4.5V<br>I <sub>OL</sub> = 2.1 ma @ V <sub>CC</sub> = 2.5V     |
| D5                 | I <sub>LI</sub>                       | Input leakage current                                | —   | ±1                  | μA                               | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub> , WP = V <sub>SS</sub>                                |
| D6                 | I <sub>LO</sub>                       | Output leakage current                               | —   | ±1                  | μA                               | V <sub>OUT</sub> = V <sub>SS</sub> or V <sub>CC</sub>  |
| D7                 | C <sub>IN</sub> ,<br>C <sub>OUT</sub> | Pin capacitance (all inputs/outputs)                 | —   | 10                  | pF                               | V <sub>CC</sub> = 5.0V (Note 1)<br>T <sub>A</sub> = 25°C, f = 1 MHz  |
| D8                 | I <sub>CC</sub> Read                  | Operating current                                    | —   | 400                 | μA                               | V <sub>CC</sub> = 5.5V, SCL = 400 kHz  |
|                    | I <sub>CC</sub> Write                 |  | —   | 3                   | mA                               | V <sub>CC</sub> = 5.5V   |
| D9                 | I <sub>CCS</sub>                      | Standby current                                      | —   | 1                   | μA                               | V <sub>CC</sub> = 5.5V, SCL = SDA = V <sub>CC</sub><br>WP = V <sub>SS</sub> , A0, A1, A2 = V <sub>SS</sub> |

**Note 1:** This parameter is periodically sampled and not 100% tested.

# 24AA024H/24LC024H

**TABLE 1-2: AC CHARACTERISTICS**

| AC CHARACTERISTICS |         |                            | Electrical Characteristics: |                                 |                                  |   |
|--------------------|---------|----------------------------|-----------------------------|---------------------------------|----------------------------------|---|
|                    |         |                            | Industrial (I):             | V <sub>CC</sub> = +1.7V to 5.5V | T <sub>A</sub> = -40°C to +85°C  |   |
|                    |         |                            | Extended (E):               | V <sub>CC</sub> = +2.5V to 5.5V | T <sub>A</sub> = -40°C to +125°C |   |
| Param. No.         | Symbol  | Characteristic             | Min.                        | Max.                            | Units                            | Conditions  |
| 1                  | FCLK    | Clock frequency            | —                           | 100                             | kHz                              | 1.7V ≤ V <sub>CC</sub> < 1.8V                     |
|                    |         |                            | —                           | 400                             | kHz                              | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V                     |
|                    |         |                            | —                           | 1000                            | kHz                              | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)          |
| 2                  | THIGH   | Clock high time            | 4000                        | —                               | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V                     |
|                    |         |                            | 600                         | —                               | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V                     |
|                    |         |                            | 500                         | —                               | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)          |
| 3                  | TLOW    | Clock low time             | 4700                        | —                               | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V                     |
|                    |         |                            | 1300                        | —                               | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V                     |
|                    |         |                            | 500                         | —                               | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)          |
| 4                  | TR      | SDA and SCL rise time      | —                           | 1000                            | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V (Note 1)            |
|                    |         |                            | —                           | 300                             | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V (Note 1)            |
|                    |         |                            | —                           | 300                             | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H) (Note 1) |
| 5                  | TF      | SDA and SCL fall time      | —                           | 1000                            | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V (Note 1)            |
|                    |         |                            | —                           | 300                             | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V (Note 1)            |
|                    |         |                            | —                           | 300                             | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H) (Note 1) |
| 6                  | THD:STA | Start condition hold time  | 4000                        | —                               | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V                     |
|                    |         |                            | 600                         | —                               | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V                     |
|                    |         |                            | 250                         | —                               | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)          |
| 7                  | TSU:STA | Start condition setup time | 4700                        | —                               | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V                     |
|                    |         |                            | 600                         | —                               | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V                     |
|                    |         |                            | 250                         | —                               | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)          |
| 8                  | THD:DAT | Data input hold time       | 0                           | —                               | ns                               | (Note 2)  |
| 9                  | TSU:DAT | Data input setup time      | 250                         | —                               | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V                     |
|                    |         |                            | 100                         | —                               | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V                     |
|                    |         |                            | 100                         | —                               | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)          |
| 10                 | TSU:STO | Stop condition setup time  | 4000                        | —                               | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V                     |
|                    |         |                            | 600                         | —                               | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V                     |
|                    |         |                            | 250                         | —                               | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)          |
| 11                 | TSU:WP  | WP setup time              | 4000                        | —                               | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V                     |
|                    |         |                            | 600                         | —                               | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V                     |
|                    |         |                            | 600                         | —                               | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)          |
| 12                 | THD:WP  | WP hold time               | 4700                        | —                               | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V                     |
|                    |         |                            | 600                         | —                               | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5                      |
|                    |         |                            | 600                         | —                               | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)          |
| 13                 | TAA     | Output valid from clock    | —                           | 3500                            | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V (Note 2)            |
|                    |         |                            | —                           | 900                             | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V (Note 2)            |
|                    |         |                            | —                           | 400                             | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H) (Note 2) |

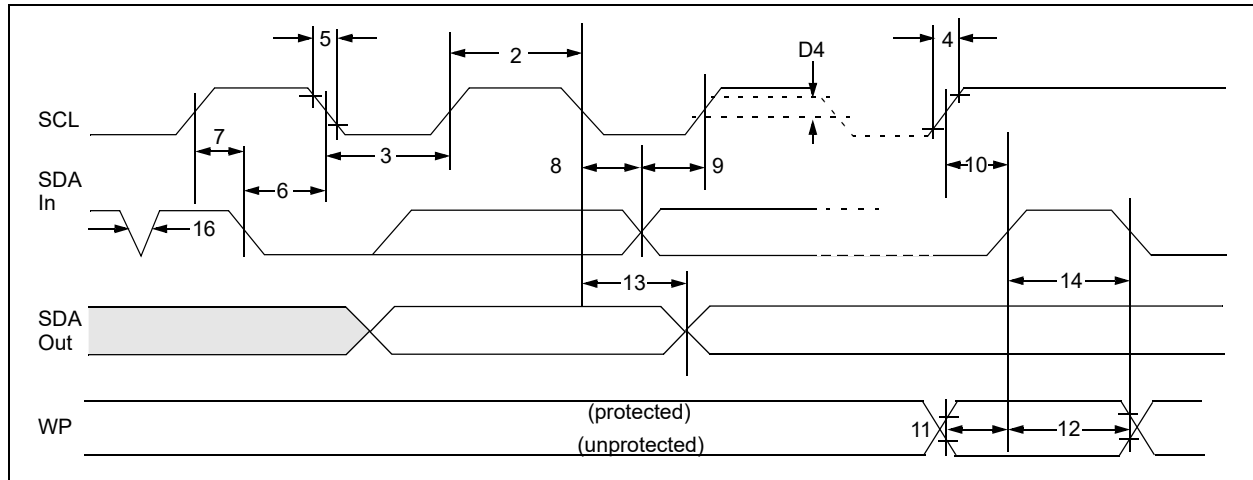
- Note**
- 1: Not 100% tested. C<sub>B</sub> = total capacitance of one bus line in pF.
  - 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
  - 3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.
  - 4: This parameter is not tested but ensured by characterization.

# 24AA024H/24LC024H

| AC CHARACTERISTICS |                  |  | Electrical Characteristics: |                                 |                                  |   |
|--------------------|------------------|--|-----------------------------|---------------------------------|----------------------------------|---|
|                    |                  |  | Industrial (I):             | V <sub>CC</sub> = +1.7V to 5.5V | T <sub>A</sub> = -40°C to +85°C  |   |
|                    |                  |  | Extended (E):               | V <sub>CC</sub> = +2.5V to 5.5V | T <sub>A</sub> = -40°C to +125°C |   |
| Param. No.         | Symbol           | Characteristic   | Min.                        | Max.                            | Units                            | Conditions  |
| 14                 | T <sub>BUF</sub> | Bus free time: Time the bus must be free before a new transmission can start | 1300                        | —                               | ns                               | 1.7V ≤ V <sub>CC</sub> < 1.8V                       |
|                    |                  |  | 4700                        | —                               | ns                               | 1.8V ≤ V <sub>CC</sub> ≤ 5.5V                       |
|                    |                  |  | 4700                        | —                               | ns                               | 2.5V ≤ V <sub>CC</sub> ≤ 5.5V (24LC024H)            |
| 16                 | T <sub>SP</sub>  | Input filter spike suppression (SDA and SCL pins)                            | —                           | 50                              | ns                               | 24AA024H<br>(Note 1 and Note 3)                     |
| 17                 | T <sub>WC</sub>  | Write cycle time (byte or page)  | —                           | 5                               | ms                               | —   |
| 18                 | —                | Endurance  | 1,000,000                   | —                               | cycles                           | 25°C, V <sub>CC</sub> = 5.5V, Page mode<br>(Note 4) |

- Note** 1: Not 100% tested. C<sub>B</sub> = total capacitance of one bus line in pF.  
 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.  
 3: The combined T<sub>SP</sub> and V<sub>HYS</sub> specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a T<sub>I</sub> specification for standard operation.  
 4: This parameter is not tested but ensured by characterization.

**FIGURE 1-1: BUS TIMING DATA**



# 24AA024H/24LC024H

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

**TABLE 2-1: PIN FUNCTION TABLE**

| Name | PDIP | SOIC | TSSOP | MSOP | TDFN <sup>(1)</sup> | Function                             |
|------|------|------|-------|------|---------------------|--------------------------------------|
| A0   | 1    | 1    | 1     | 1    | 1                   | User Configurable Chip Address Input |
| A1   | 2    | 2    | 2     | 2    | 2                   | User Configurable Chip Address Input |
| A2   | 3    | 3    | 3     | 3    | 3                   | User Configurable Chip Address Input |
| Vss  | 4    | 4    | 4     | 4    | 4                   | Ground                               |
| SDA  | 5    | 5    | 5     | 5    | 5                   | Serial Address/Data I/O              |
| SCL  | 6    | 6    | 6     | 6    | 6                   | Serial Clock                         |
| WP   | 7    | 7    | 7     | 7    | 7                   | Write-Protect Input                  |
| Vcc  | 8    | 8    | 8     | 8    | 8                   | Power Supply                         |

**Note 1:** The exposed pad on the TDFN package can be connected to Vss or left floating.

### 2.1 Chip Address Inputs (A0,A1,A2)

The A0, A1 and A2 inputs are used by the 24AA024H/24LC024H for multiple device operations. The levels on these inputs are compared with the corresponding bits in the client address. The chip is selected if the compare is true. Up to eight 24AA024H/24LC024H devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either Vcc or Vss. In most applications, the chip address inputs A0, A1 and A2 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

### 2.2 Serial Address/Data Input/Output (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

### 2.3 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

### 2.4 Write-Protect (WP)

WP is the hardware write-protect pin. It must be tied to Vcc or Vss. If tied to Vcc, the hardware write protection is enabled and will protect half of the array (80h-FFh). If the WP pin is tied to Vss the hardware write protection is disabled.

### 2.5 Noise Protection

The 24AA024H/24LC024H employs a Vcc threshold detector circuit that disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits that suppress noise spikes to assure proper device operation even on a noisy bus.

## 3.0 FUNCTIONAL DESCRIPTION

The 24AA024H/24LC024H supports a bidirectional, two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a host device that generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions while the 24AA024H/24LC024H works as client. Both host and client can operate as transmitter or receiver, but the host device determines which mode is activated.

# 24AA024H/24LC024H

## 4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

### 4.1 Bus Not Busy (A)

Both data and clock lines remain high.

### 4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

### 4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

### 4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the host device and is, theoretically, unlimited, though only the last 16 bytes will be stored when doing a write operation. When an overwrite does occur, it will replace data in a First-In-First-Out (FIFO) principle.

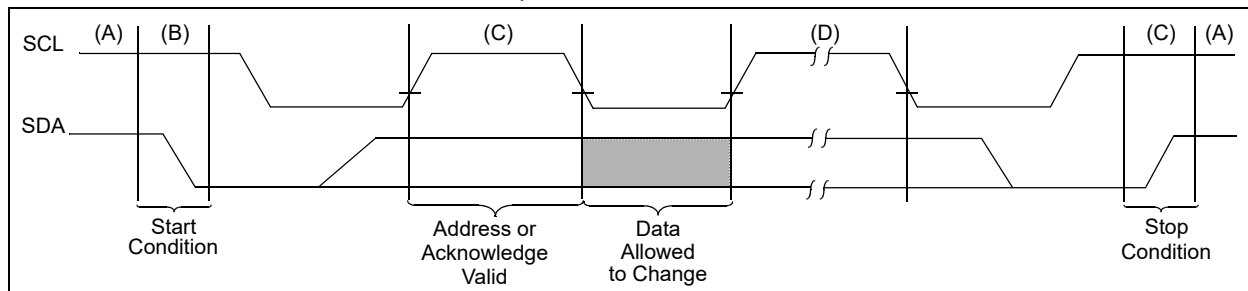
### 4.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The host device must generate an extra clock pulse which is associated with this Acknowledge bit.

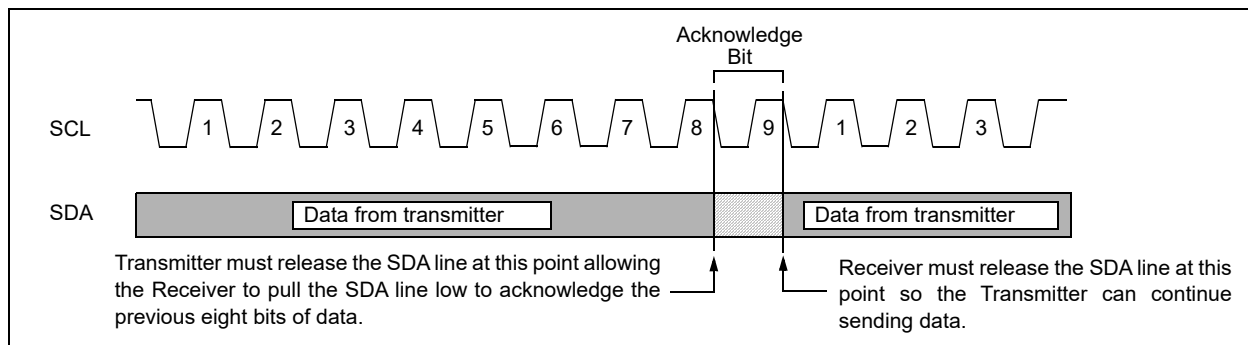
**Note:** The 24AA024H/24LC024H does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. A host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client must leave the data line high to enable the host to generate the Stop condition (Figure 4-2).

**FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS**



**FIGURE 4-2: ACKNOWLEDGE TIMING**





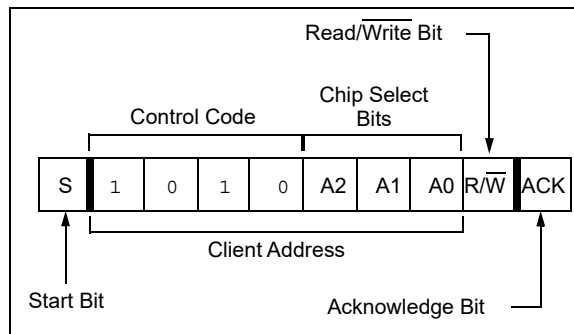
## 5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the host device. The control byte consists of a four-bit control code; for the 24AA024H/24LC024H this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24AA024H/24LC024H devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address. The combination of the 4-bit control code and the next three bits are called the client address.

The last bit of the control byte is the Read/Write ( $\overline{R/W}$ ) bit and it defines the operation to be performed. When set to a '1', a read operation is selected. When set to a '0', a write operation is selected. The next byte received defines the address of the first data byte (Figure 5-2).

Following the Start condition, the 24AA024H/24LC024H monitors the SDA bus, checking the control byte being transmitted. Upon receiving a valid client address and the  $\overline{R/W}$  bit, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the  $\overline{R/W}$  bit, the 24AA024H/24LC024H will select a read or write operation.

FIGURE 5-1: CONTROL BYTE FORMAT

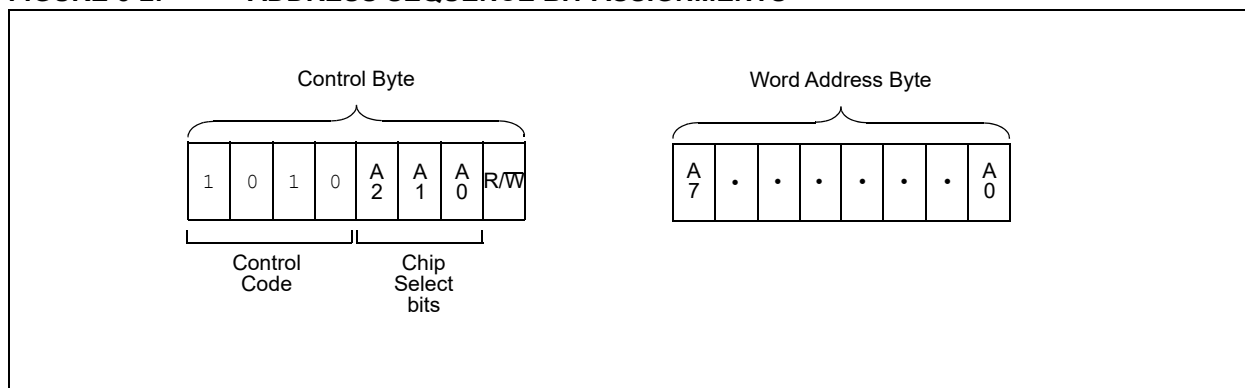


### 5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 16 Kbits by adding up to eight 24AA024H/24LC024H devices on the same bus.

In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9, and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



# 24AA024H/24LC024H

## 6.0 WRITE OPERATIONS

### 6.1 Byte Write

Following the Start signal from the host, the device code (4 bits), the Chip Select bits (3 bits) and the R/W bit (which is a logic low) are placed onto the bus by the host transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the host is the word address and will be written into the Address Pointer of the 24AA024H/24LC024H. After receiving another Acknowledge signal from the 24AA024H/24LC024H, the host device will transmit the data word to be written into the addressed memory location. The 24AA024H/24LC024H acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and the 24AA024H/24LC024H will not generate Acknowledge signals during this time (Figure 6-1). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if write protection is enabled.

### 6.2 Page Write

The write-control byte, word address and the first data byte are transmitted to the 24AA024H/24LC024H in the same way as in a byte write. But instead of generating a Stop condition, the host transmits up to 15 additional data bytes to the 24AA024H/24LC024H that are temporarily stored in the on-chip page buffer and will be written into the memory once the host has transmitted a Stop condition. Upon receipt of each word, the four lower order Address Pointer bits, which form the byte counter, are internally incremented by one.

The higher order four bits of the word address remain constant. If the host should transmit more than 16 bytes prior to generating the Stop condition, the Address Pointer will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if write protection is enabled.

**Note:** Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size - 1. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary that the application software prevent page write operations that would attempt to cross a page boundary.

### 6.3 Write Protection

The WP pin must be tied to VCC or VSS. If tied to VCC, half of the array will be write-protected (80h-FFh). If the WP pin is tied to VSS, write operations to all address locations are allowed.

FIGURE 6-1: BYTE WRITE

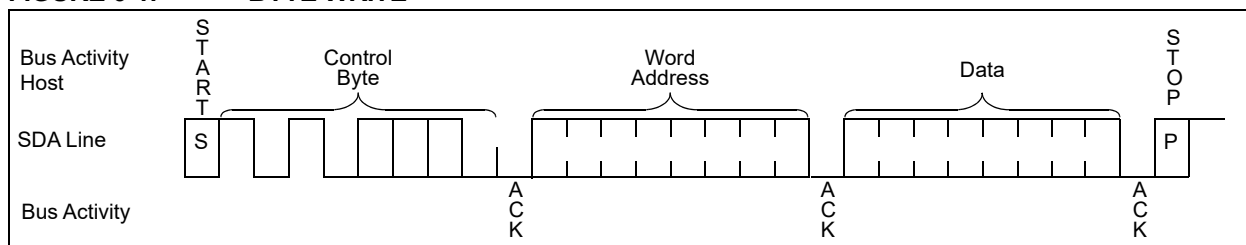
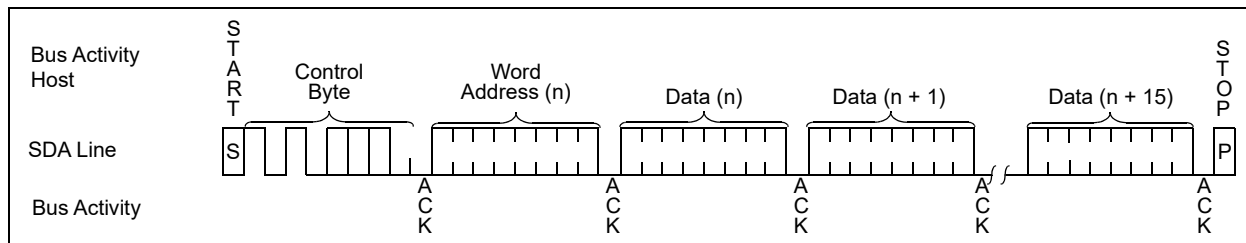


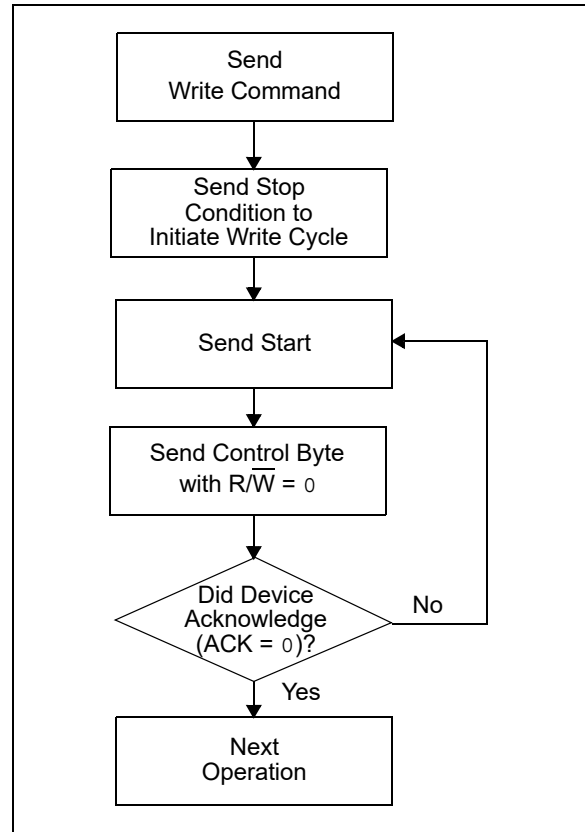
FIGURE 6-2: PAGE WRITE



## 7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the host, the device initiates the internally-timed write cycle and ACK polling can be initiated immediately. This involves the host sending a Start condition followed by the control byte for a write command ( $R/\overline{W} = 0$ ). If the device is still busy with the write cycle, no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, the device will return the ACK and the host can then proceed with the next read or write command. See [Figure 7-1](#) for a flow diagram of this operation.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



# 24AA024H/24LC024H

## 8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations, with the exception that the R/W bit of the client address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

### 8.1 Current Address Read

The 24AA024H/24LC024H contains an Address Pointer that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the client address with the R/W bit set to '1', the 24AA024H/24LC024H issues an acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24AA024H/24LC024H discontinues transmission (Figure 8-1).

### 8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 24AA024H/24LC024H as part of a write operation.

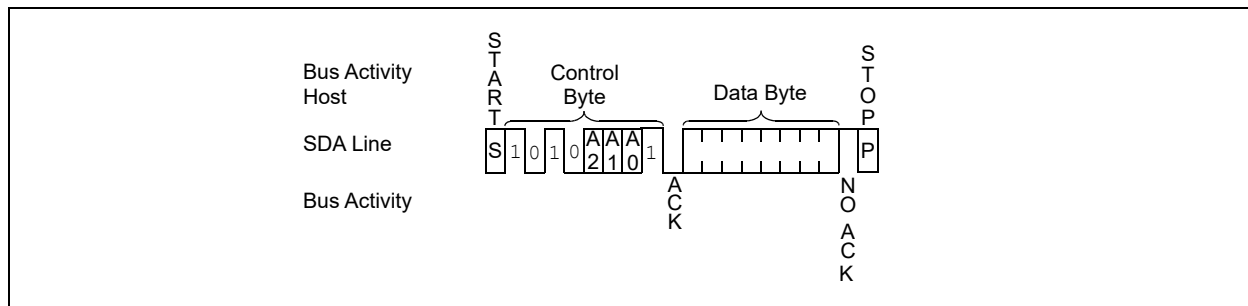
Once the word address is sent, the host generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again but with the R/W bit set to a '1'. The 24AA024H/24LC024H will then issue an acknowledge and transmits the eight-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24AA024H/24LC024H discontinues transmission (Figure 8-2). After this command, the internal Address Pointer will point to the address location following the one that was just read.

### 8.3 Sequential Read

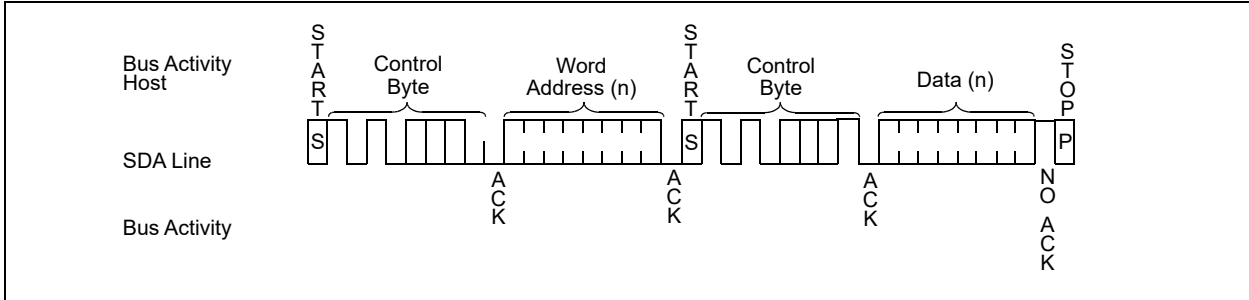
Sequential reads are initiated in the same way as a random read except that after the 24AA024H/24LC024H transmits the first data byte, the host issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24AA024H/24LC024H to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads, the 24AA024H/24LC024H contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address FFh to address 00h.

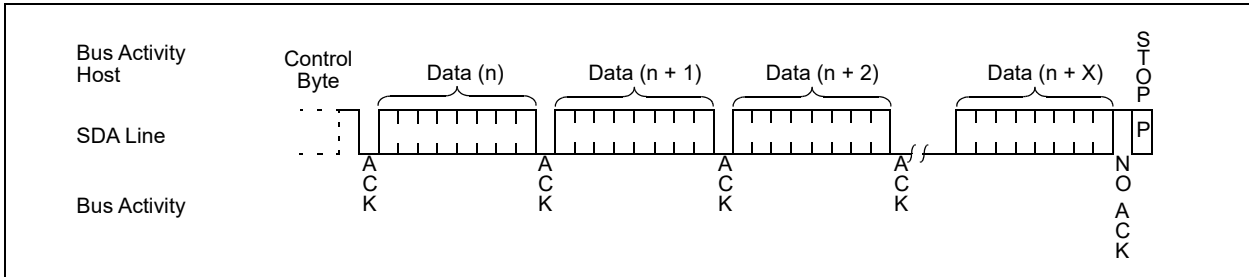
FIGURE 8-1: CURRENT ADDRESS READ



**FIGURE 8-2: RANDOM READ**



**FIGURE 8-3: SEQUENTIAL READ**

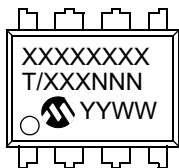


# 24AA024H/24LC024H

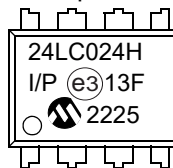
## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information

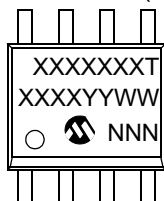
8-Lead PDIP (300 mil)



Example:



8-Lead SOIC (3.90 mm)



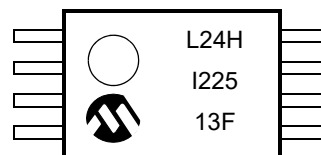
Example:



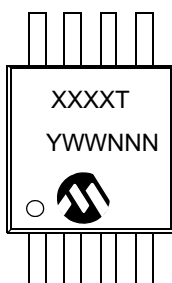
8-Lead TSSOP



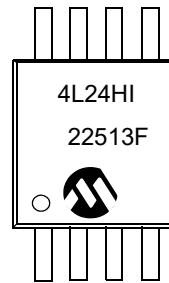
Example:



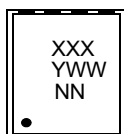
8-Lead MSOP



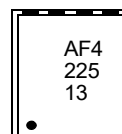
Example:



8-Lead 2x3 TDFN



Example:



# 24AA024H/24LC024H

| Part Number | 1st Line Marking Codes |        |        |        |
|-------------|------------------------|--------|--------|--------|
|             | TSSOP                  | MSOP   | TDFN   |        |
|             |                        |        | I-Temp | E-Temp |
| 24AA024H    | A24H                   | 4A24HT | AF1    | —      |
| 24LC024H    | L24H                   | 4L24HT | AF4    | AF5    |

|                |        |  |
|----------------|--------|--|
| <b>Legend:</b> | XX...X | Part number or part number code                                  |
|                | T      | Temperature (I, E)   |
|                | Y      | Year code (last digit of calendar year)                          |
|                | YY     | Year code (last 2 digits of calendar year)                       |
|                | WW     | Week code (week of January 1 is week '01')                       |
|                | NNN    | Alphanumeric traceability code (2 characters for small packages) |
|                | (e3)   | RoHS-compliant JEDEC® designator for Matte Tin (Sn)              |

**Note:** Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

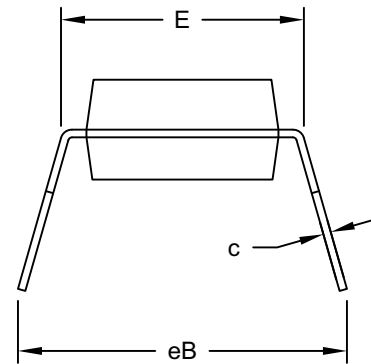
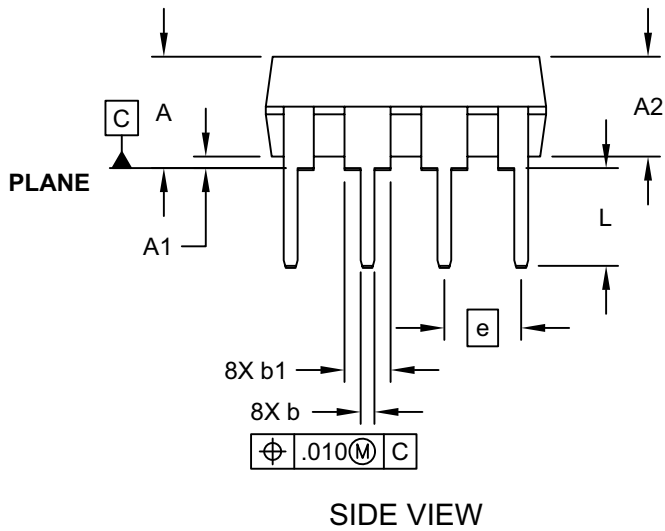
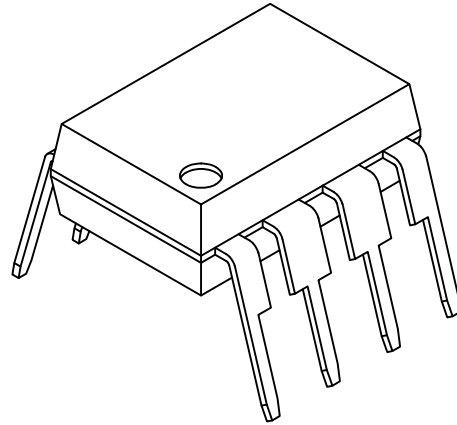
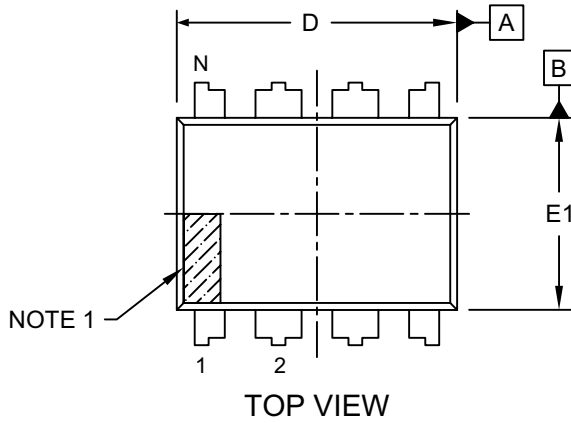
**Note:** For small packages with no room for RoHS-compliant JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# 24AA024H/24LC024H

## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



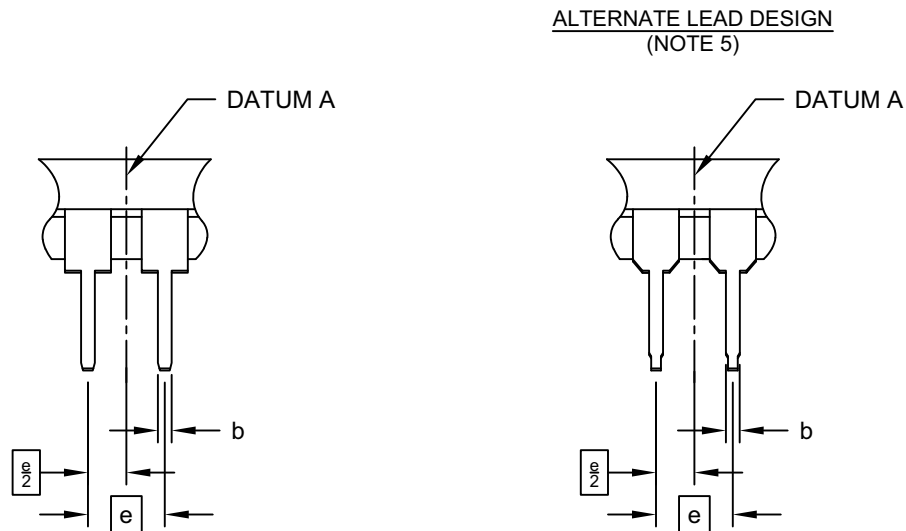
Microchip Technology Drawing No. C04-018-P Rev F Sheet 1 of 2



# 24AA024H/24LC024H

## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits           | Units | INCHES   |      |      |
|----------------------------|-------|----------|------|------|
|                            |       | MIN      | NOM  | MAX  |
| Number of Pins             | N     | 8        |      |      |
| Pitch                      | e     | .100 BSC |      |      |
| Top to Seating Plane       | A     | -        | -    | .210 |
| Molded Package Thickness   | A2    | .115     | .130 | .195 |
| Base to Seating Plane      | A1    | .015     | -    | -    |
| Shoulder to Shoulder Width | E     | .290     | .310 | .325 |
| Molded Package Width       | E1    | .240     | .250 | .280 |
| Overall Length             | D     | .348     | .365 | .400 |
| Tip to Seating Plane       | L     | .115     | .130 | .150 |
| Lead Thickness             | c     | .008     | .010 | .015 |
| Upper Lead Width           | b1    | .040     | .060 | .070 |
| Lower Lead Width           | b     | .014     | .018 | .022 |
| Overall Row Spacing        | §     | eB       | -    | .430 |

**Notes:**

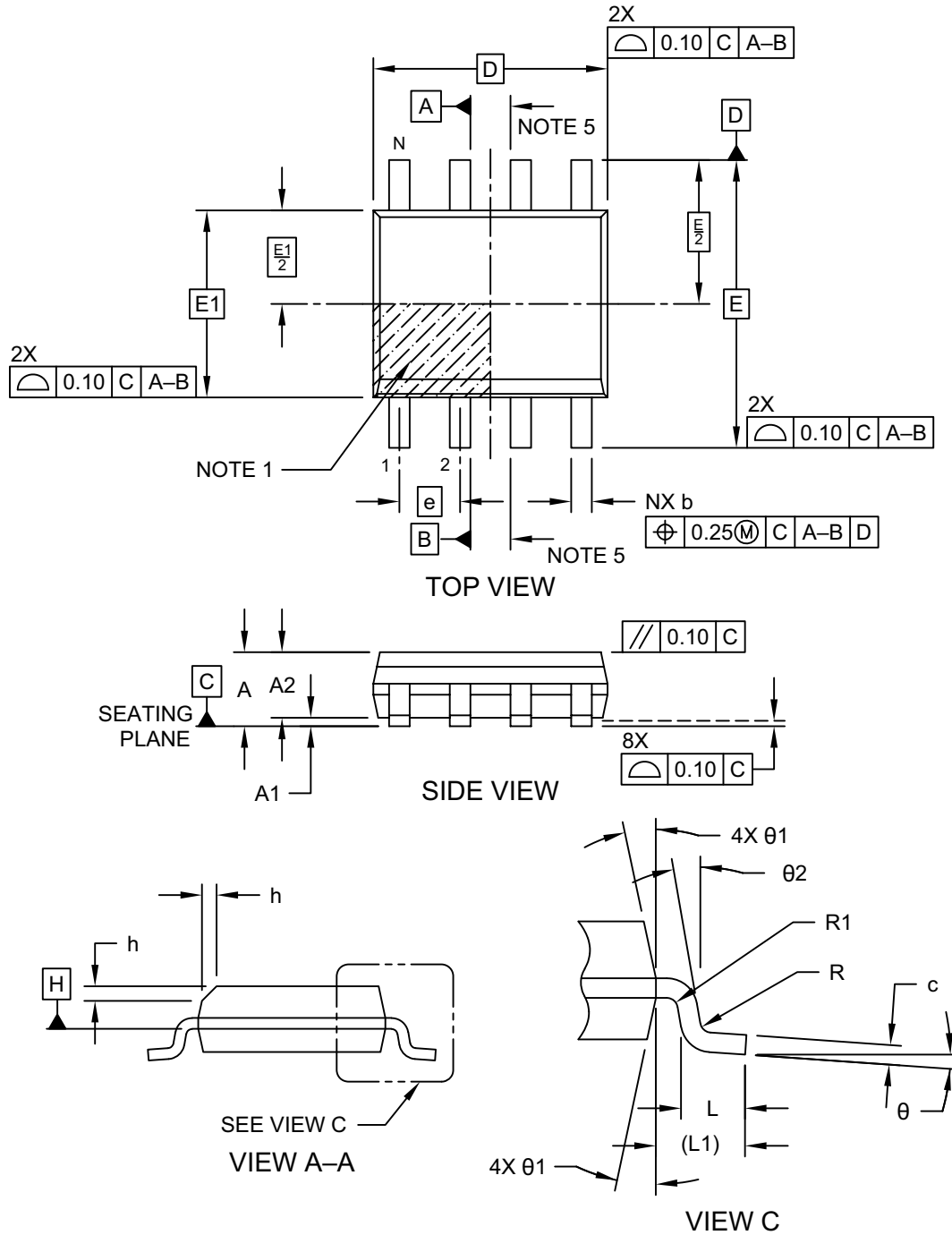
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev F Sheet 2 of 2

# 24AA024H/24LC024H

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

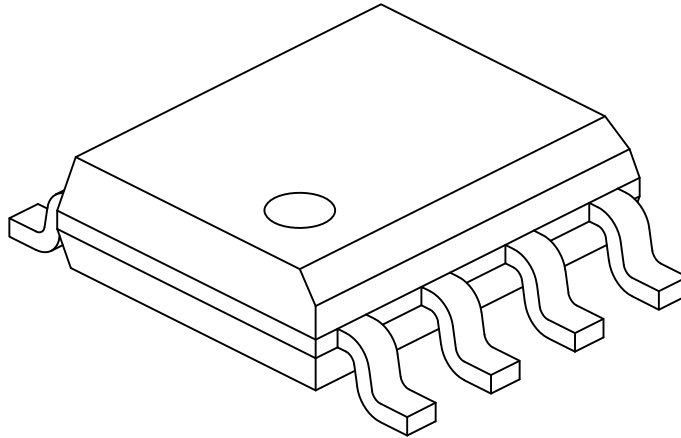


Microchip Technology Drawing No. C04-057-SN Rev J Sheet 1 of 2

# 24AA024H/24LC024H

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units | MILLIMETERS |     |      |
|--------------------------|-------|-------------|-----|------|
|                          |       | MIN         | NOM | MAX  |
| Number of Pins           | N     | 8           |     |      |
| Pitch                    | e     | 1.27 BSC    |     |      |
| Overall Height           | A     | –           | –   | 1.75 |
| Molded Package Thickness | A2    | 1.25        | –   | –    |
| Standoff §               | A1    | 0.10        | –   | 0.25 |
| Overall Width            | E     | 6.00 BSC    |     |      |
| Molded Package Width     | E1    | 3.90 BSC    |     |      |
| Overall Length           | D     | 4.90 BSC    |     |      |
| Chamfer (Optional)       | h     | 0.25        | –   | 0.50 |
| Foot Length              | L     | 0.40        | –   | 1.27 |
| Footprint                | L1    | 1.04 REF    |     |      |
| Lead Thickness           | c     | 0.17        | –   | 0.25 |
| Lead Width               | b     | 0.31        | –   | 0.51 |
| Lead Bend Radius         | R     | 0.07        | –   | –    |
| Lead Bend Radius         | R1    | 0.07        | –   | –    |
| Foot Angle               | θ     | 0°          | –   | 8°   |
| Mold Draft Angle         | θ1    | 5°          | –   | 15°  |
| Lead Angle               | θ2    | 0°          | –   | 8°   |

**Notes:**

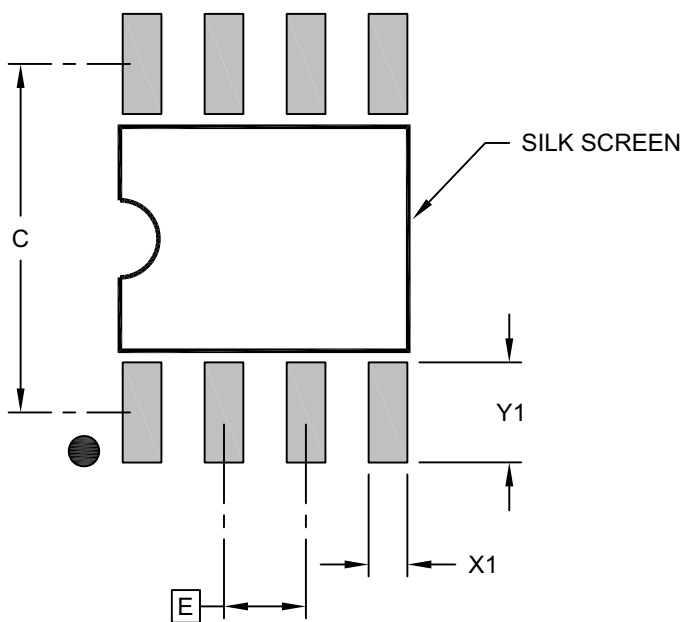
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev J Sheet 2 of 2

# 24AA024H/24LC024H

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits        | Units | MILLIMETERS |      |      |
|-------------------------|-------|-------------|------|------|
|                         |       | MIN         | NOM  | MAX  |
| Contact Pitch           | E     | 1.27 BSC    |      |      |
| Contact Pad Spacing     | C     |             | 5.40 |      |
| Contact Pad Width (X8)  | X1    |             |      | 0.60 |
| Contact Pad Length (X8) | Y1    |             |      | 1.55 |

Notes:

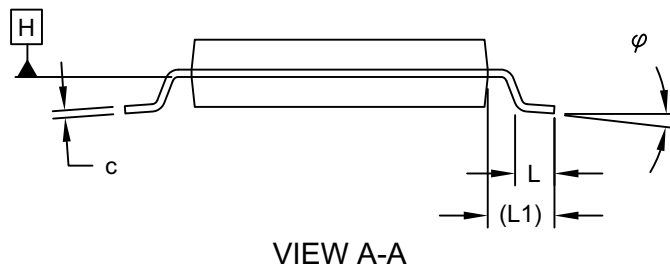
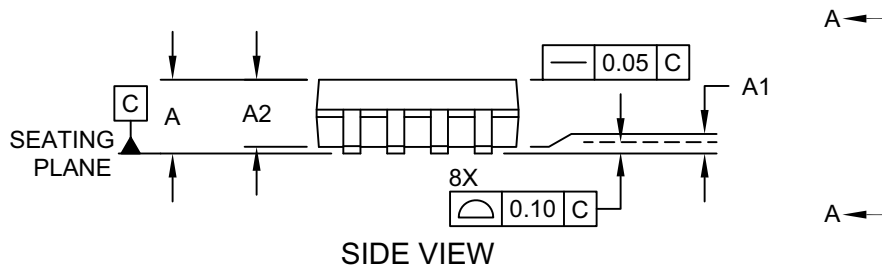
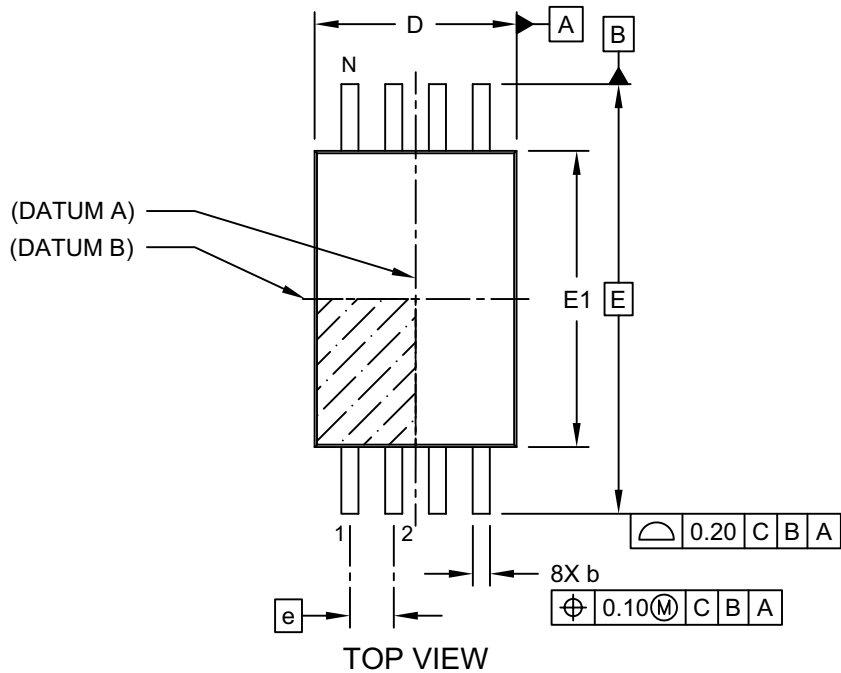
1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev J

# 24AA024H/24LC024H

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

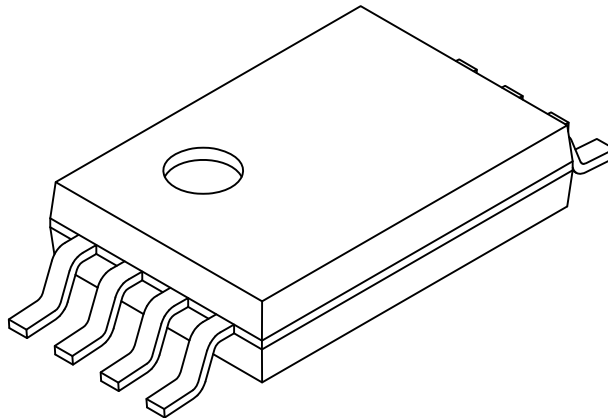


Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

# 24AA024H/24LC024H

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units  | MILLIMETERS |      |      |
|--------------------------|--------|-------------|------|------|
|                          |        | MIN         | NOM  | MAX  |
| Number of Pins           | N      | 8           |      |      |
| Pitch                    | e      | 0.65 BSC    |      |      |
| Overall Height           | A      | -           | -    | 1.20 |
| Molded Package Thickness | A2     | 0.80        | 1.00 | 1.05 |
| Standoff                 | A1     | 0.05        | -    | -    |
| Overall Width            | E      | 6.40 BSC    |      |      |
| Molded Package Width     | E1     | 4.30        | 4.40 | 4.50 |
| Overall Length           | D      | 2.90        | 3.00 | 3.10 |
| Foot Length              | L      | 0.45        | 0.60 | 0.75 |
| Footprint                | L1     | 1.00 REF    |      |      |
| Lead Thickness           | c      | 0.09        | -    | 0.25 |
| Foot Angle               | $\phi$ | 0°          | 4°   | 8°   |
| Lead Width               | b      | 0.19        | -    | 0.30 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

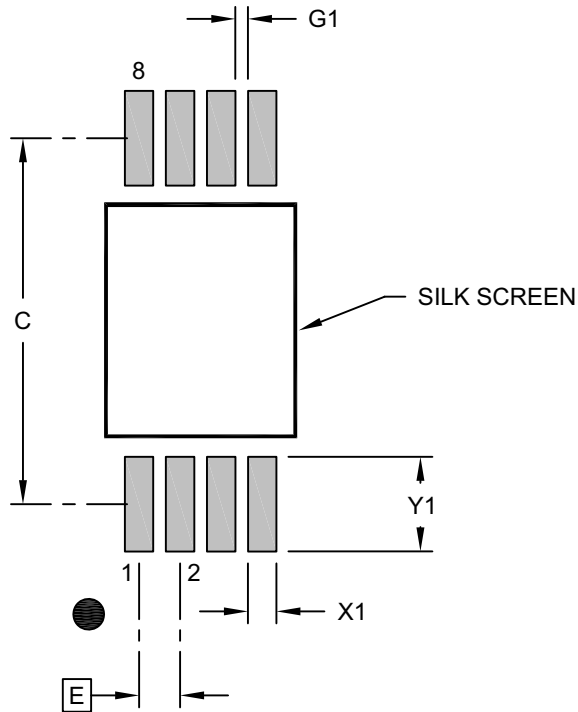
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

| Dimension Limits               | Units | MILLIMETERS |      |      |
|--------------------------------|-------|-------------|------|------|
|                                |       | MIN         | NOM  | MAX  |
| Contact Pitch                  | E     | 0.65 BSC    |      |      |
| Contact Pad Spacing            | C     |             | 5.80 |      |
| Contact Pad Width (X8)         | X1    |             |      | 0.45 |
| Contact Pad Length (X8)        | Y1    |             |      | 1.50 |
| Contact Pad to Center Pad (X6) | G1    | 0.20        |      |      |

#### Notes:

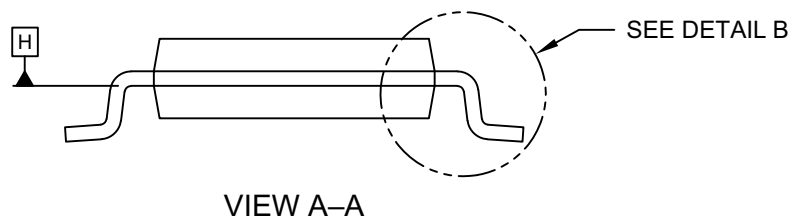
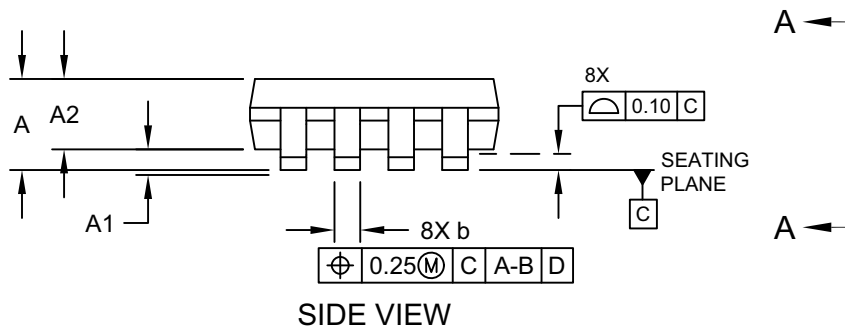
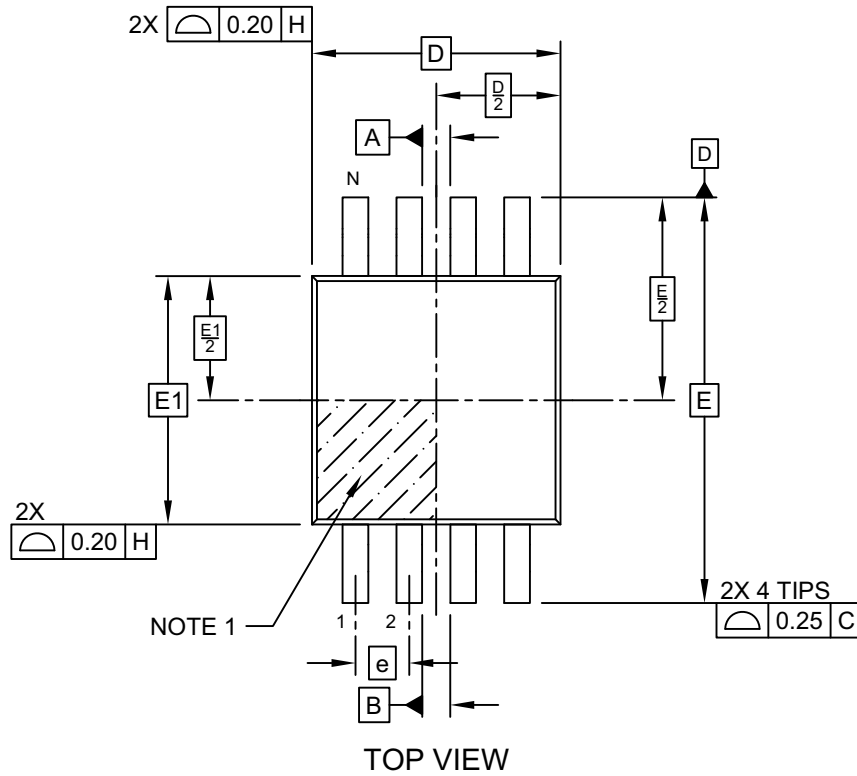
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

# 24AA024H/24LC024H

## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



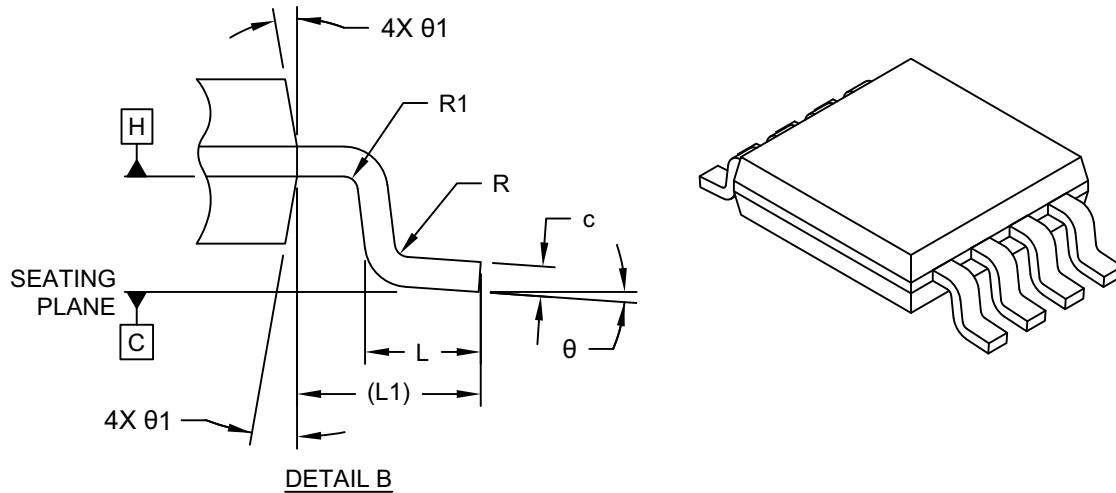
Microchip Technology Drawing C04-111-MS Rev D Sheet 1 of 2



# 24AA024H/24LC024H

## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units | MILLIMETERS |      |      |
|--------------------------|-------|-------------|------|------|
|                          |       | MIN         | NOM  | MAX  |
| Number of Terminals      | N     | 8           |      |      |
| Pitch                    | e     | 0.65 BSC    |      |      |
| Overall Height           | A     | –           | –    | 1.10 |
| Standoff                 | A1    | 0.00        | –    | 0.15 |
| Molded Package Thickness | A2    | 0.75        | 0.85 | 0.95 |
| Overall Length           | D     | 3.00 BSC    |      |      |
| Overall Width            | E     | 4.90 BSC    |      |      |
| Molded Package Width     | E1    | 3.00 BSC    |      |      |
| Terminal Width           | b     | 0.22        | –    | 0.40 |
| Terminal Thickness       | c     | 0.08        | –    | 0.23 |
| Terminal Length          | L     | 0.40        | 0.60 | 0.80 |
| Footprint                | L1    | 0.95 REF    |      |      |
| Lead Bend Radius         | R     | 0.07        | –    | –    |
| Lead Bend Radius         | R1    | 0.07        | –    | –    |
| Foot Angle               | θ     | 0°          | –    | 8°   |
| Mold Draft Angle         | θ1    | 5°          | –    | 15°  |

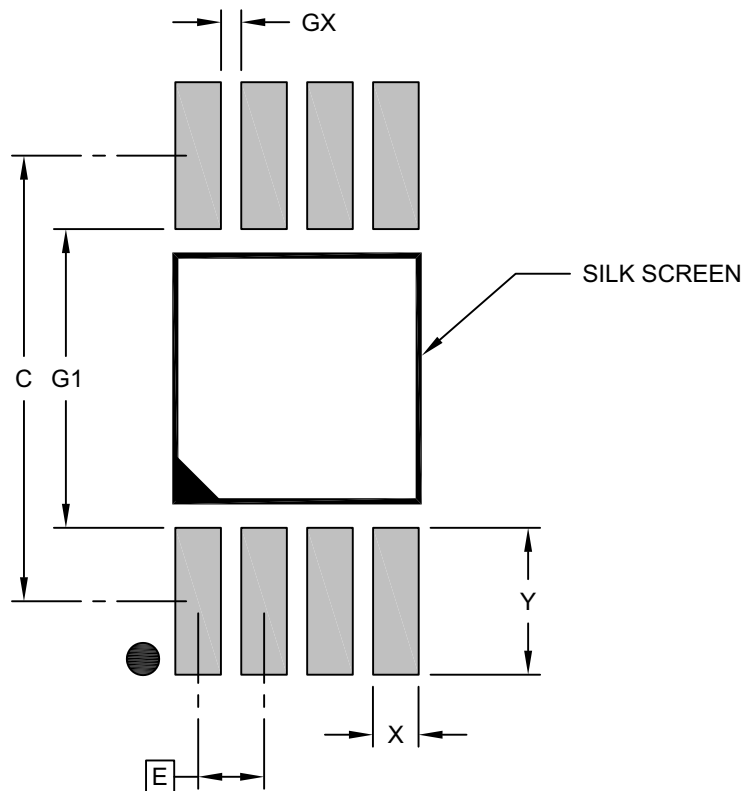
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

# 24AA024H/24LC024H

## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

| Dimension Limits                | Units | MILLIMETERS |      |      |
|---------------------------------|-------|-------------|------|------|
|                                 |       | MIN         | NOM  | MAX  |
| Contact Pitch                   | E     | 0.65 BSC    |      |      |
| Contact Pad Spacing             | C     |             | 4.40 |      |
| Contact Pad Width (X8)          | X     |             |      | 0.45 |
| Contact Pad Length (X8)         | Y     |             |      | 1.45 |
| Contact Pad to Contact Pad (X4) | G1    | 2.95        |      |      |
| Contact Pad to Contact Pad (X6) | GX    | 0.20        |      |      |

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

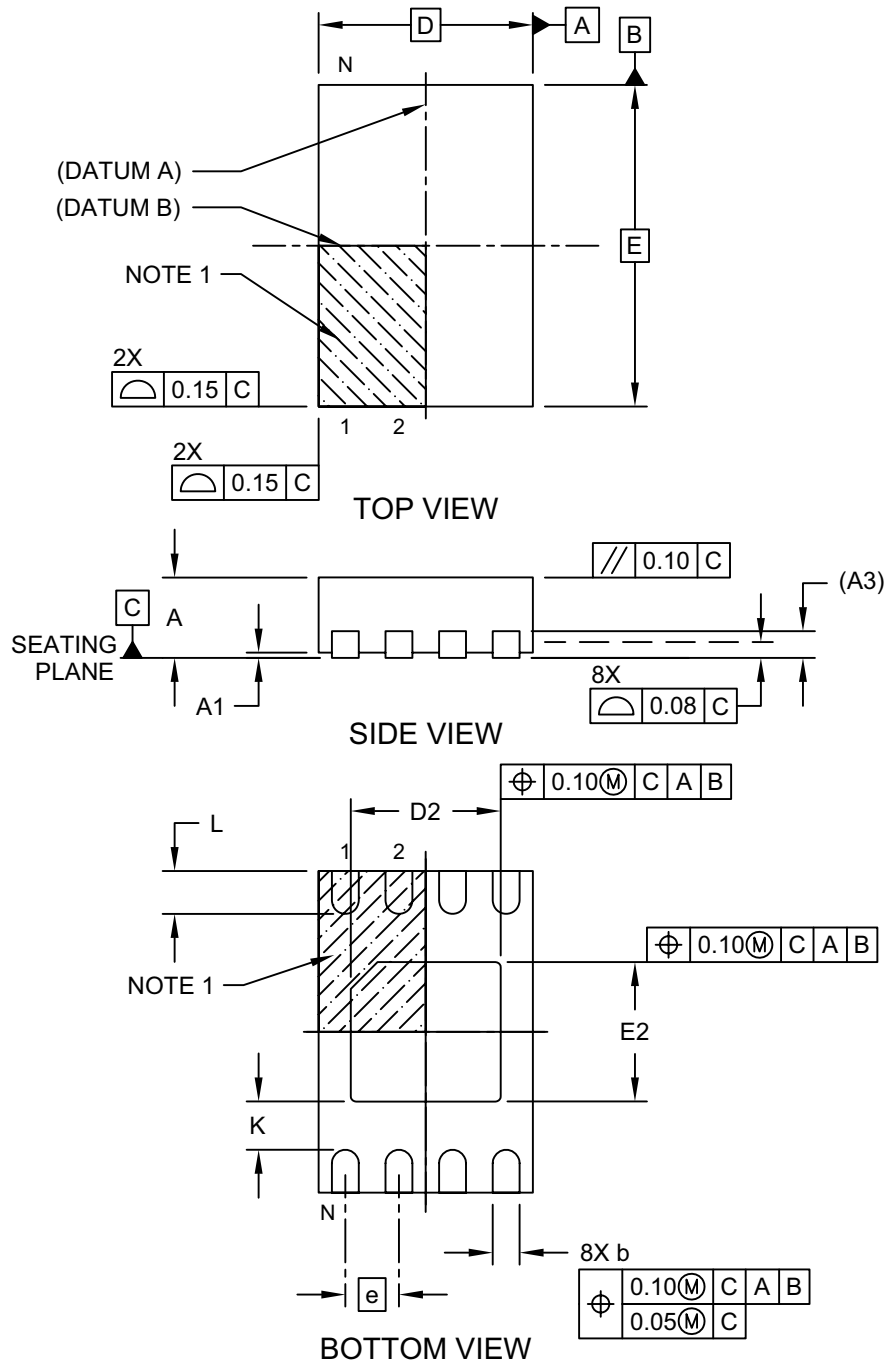
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev D

# 24AA024H/24LC024H

## 8-Lead Plastic Dual Flat, No Lead Package (MNY) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

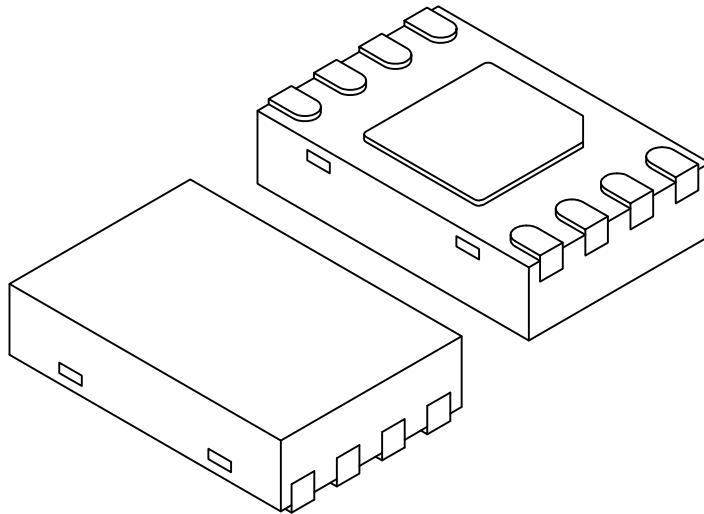


Microchip Technology Drawing No. C04-129-MNY Rev E Sheet 1 of 2

# 24AA024H/24LC024H

## 8-Lead Plastic Dual Flat, No Lead Package (MNY) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                  |    | MILLIMETERS |      |      |
|------------------------|----|-------------|------|------|
| Dimension Limits       |    | MIN         | NOM  | MAX  |
| Number of Pins         | N  | 8           |      |      |
| Pitch                  | e  | 0.50 BSC    |      |      |
| Overall Height         | A  | 0.70        | 0.75 | 0.80 |
| Standoff               | A1 | 0.00        | 0.02 | 0.05 |
| Contact Thickness      | A3 | 0.20 REF    |      |      |
| Overall Length         | D  | 2.00 BSC    |      |      |
| Overall Width          | E  | 3.00 BSC    |      |      |
| Exposed Pad Length     | D2 | 1.35        | 1.40 | 1.45 |
| Exposed Pad Width      | E2 | 1.25        | 1.30 | 1.35 |
| Contact Width          | b  | 0.20        | 0.25 | 0.30 |
| Contact Length         | L  | 0.25        | 0.30 | 0.45 |
| Contact-to-Exposed Pad | K  | 0.20        | -    | -    |

### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

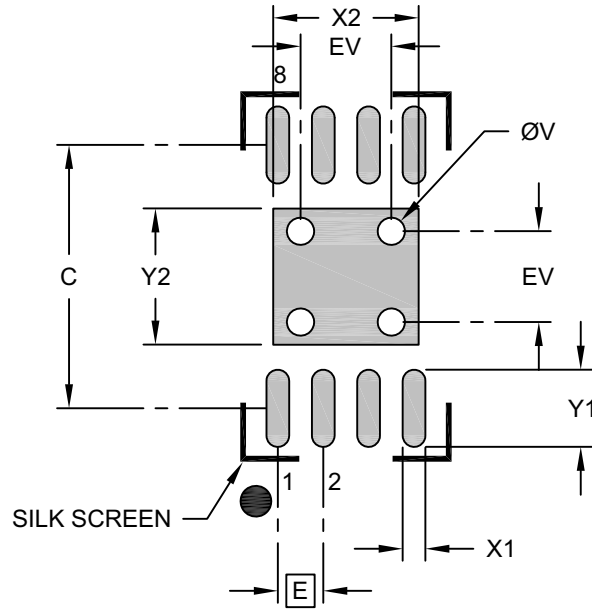
REF: Reference Dimension, usually without tolerance, for information purposes only.

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# 24AA024H/24LC024H

## 8-Lead Plastic Dual Flat, No Lead Package (MNY) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

| Dimension Limits           | Units | MILLIMETERS |      |      |
|----------------------------|-------|-------------|------|------|
|                            |       | MIN         | NOM  | MAX  |
| Contact Pitch              | E     | 0.50 BSC    |      |      |
| Optional Center Pad Width  | X2    |             |      | 1.60 |
| Optional Center Pad Length | Y2    |             |      | 1.50 |
| Contact Pad Spacing        | C     |             | 2.90 |      |
| Contact Pad Width (X8)     | X1    |             |      | 0.25 |
| Contact Pad Length (X8)    | Y1    |             |      | 0.85 |
| Thermal Via Diameter       | V     |             | 0.30 |      |
| Thermal Via Pitch          | EV    |             | 1.00 |      |

#### Notes:

- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MNY Rev. B

# 24AA024H/24LC024H

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## APPENDIX A: HISTORY

### Revision B (08/2022)

Updated formatting to current template; Replaced terminology "Master" and "Slave" with "Host" and "Client" respectively; Updated MSOP, PDIP, SOIC, TDFN and TSSOP package drawings.

### Revision A (08/2008)

Original release.

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# 24AA024H/24LC024H

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u>   | <u>IXI</u> <sup>(1)</sup> | <u>-X</u>         | <u>IXX</u> |
|---|---------------------------|-------------------|------------|
| Device  | Tape and Reel Option      | Temperature Range | Package    |
| <p><b>Device:</b> 24AA024H = 1.7V, 2-Kbit Addressable Serial EEPROM<br/>24LC024H = 2.5V, 2-Kbit Addressable Serial EEPROM</p>   |                           |                   |            |
| <p><b>Tape and Reel Option:</b> Blank = Standard packaging (tube or tray)<br/>T = Tape and Reel<sup>(1)</sup></p>   |                           |                   |            |
| <p><b>Temperature Range:</b> I = -40°C to +85°C (Industrial)<br/>E = -40°C to +125°C (Extended)</p>   |                           |                   |            |
| <p><b>Package:</b> P = Plastic Dual In-Line – 300 mil Body, 8-Lead (PDIP)<br/>SN = Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC)<br/>ST = Plastic Thin Shrink Small Outline – 4.4 mm, 8-Lead (TSSOP)<br/>MS = Plastic Micro Small Outline Package, 8-Lead (MSOP)<br/>MNY<sup>(2)</sup> = Plastic Dual Flat, No Lead Package - 2x3x0.75mm Body, 8-Lead (TDFN) (Tape and Reel only)</p> |                           |                   |            |

**Examples:**

- a) 24AA024H-I/P: Industrial Temperature, 1.7V, PDIP package.
- b) 24AA024H-I/SN: Industrial Temperature, 1.7V, SOIC package.
- c) 24AA024HT-I/ST: Tape and Reel, Industrial Temperature, 1.7V, TSSOP package.
- d) 24LC024H-I/P: Industrial Temperature, 2.5V, PDIP package.
- e) 24LC024HT-E/SN: Tape and Reel, Extended Temperature, 2.5V, SOIC package.
- f) 24LC024HT-I/MS: Tape and Reel, Industrial Temperature, 2.5V, MSOP package.

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** “Y” indicates a Nickel Palladium Gold (NiPdAu) finish.



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