AT34C02D

I²C-Compatible (Two-Wire) Serial Presence Detect (SPD) EEPROM with Permanent and Reversible Software Write Protection 2-Kbit (256 X 8)

Features

- Low-Voltage Operation:
  - V_{CC} = 1.7V to 5.5V
- Internally Organized as 256 x 8 (2K)
- JEDEC EE1002 and EE1002A Serial Presence Detect (SPD) Compliant
  - EEPROM Specification for use in DDR, DDR2, and DDR3 DIMM Modules
- Industrial Temperature Range: -40°C to +85°C
- I²C-Compatible (Two-Wire) Serial Interface:
  - 100 kHz Standard Mode, 1.7V to 5.5V
  - 400 kHz Fast Mode, 1.7V to 5.5V
  - 1 MHz Fast Mode Plus (FM+), 3.6 to 5.5V
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Write-Protect Pin for Full Array Hardware Data Protection
- Ultra Low Active Current (3 mA maximum) and Standby Current (6 µA maximum)
- 16-Byte Page Write Mode:
  - Partial page writes allowed
- Random and Sequential Read Modes
- Self-Timed Write Cycle within 5 ms Maximum
- ESD Protection > 4,000V
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Green Package Options (Lead-free/Halide-free/RoHS compliant)
- Die Sale Options: Wafer Form

Packages

- 8-Lead SOIC, 8-Lead TSSOP, 8-Pad UDFN and 8-Ball VFBGA

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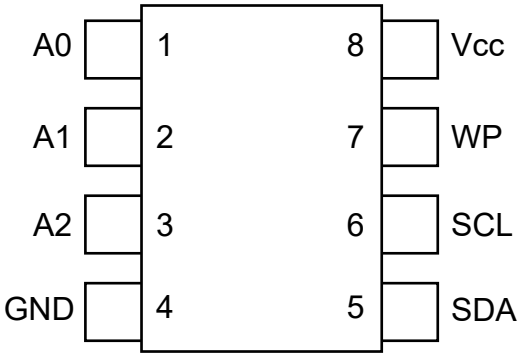
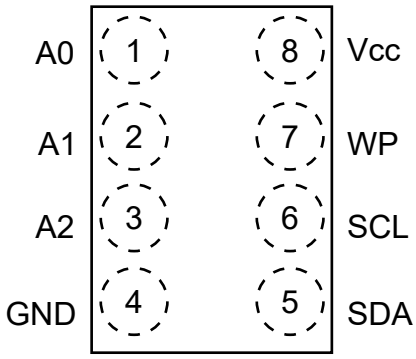
1. Package Types (not to scale)

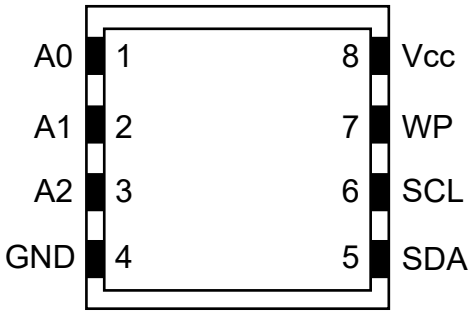
8-lead SOIC/TSSOP
(Top View)



8-Ball VFBGA
(Top View)



8-pad UDFN
(Top View)



2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	8-Lead SOIC	8-Lead TSSOP	8-Pad UDFN[1]	8-Ball VFBA	Function
A0[2]	1	1	1	1	Device Address Input
A1[2]	2	2	2	2	Device Address Input
A2[2]	3	3	3	3	Device Address Input
GND	4	4	4	4	Ground
SDA	5	5	5	5	Serial Data
SCL	6	6	6	6	Serial Clock
WP[2]	7	7	7	7	Write-Protect
V_{CC}	8	8	8	8	Device Power Supply

Notes:

1. The exposed pad on this package can be connected to GND or left floating.
2. If the A0, A1, A2 or WP pins are not driven, they are internally pulled down to GND. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Microchip recommends connecting these pins to a known state whenever possible.

2.1 Device Address Inputs (A0, A1, A2)

The A0, A1 and A2 pins are device address inputs that are hard-wired (directly to GND or to V_{CC}) for compatibility with other two-wire Serial EEPROM devices. When the pins are hard-wired, as many as eight devices may be addressed on a single bus system. A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A0, A1 and A2 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, Microchip recommends always connecting the address pins to a known state. When using a pull-up resistor, Microchip recommends using 10 kΩ or less.

2.2 Ground

The ground reference for the power supply. GND should be connected to the system ground.

2.3 Serial Data (SDA)

The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled high using an external pull-up resistor (not to exceed 10 kΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

2.4 Serial Clock (SCL)

The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled high using an external pull-up resistor.

2.5 Write-Protect (WP)

The write-protect input, when connected to GND, allows normal write operations. When the WP pin is connected directly to V_{CC}, all write operations to the protected memory are inhibited.

If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, Microchip recommends always connecting the WP pin to a known state. When using a pull-up resistor, Microchip recommends using 10 kΩ or less.

Table 2-2. Write-Protect

WP Pin Status	Part of the Array Protected
At V_{CC}	Full Array
At GND	Normal Write Operations

2.6 Device Power Supply (V_{CC})

The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

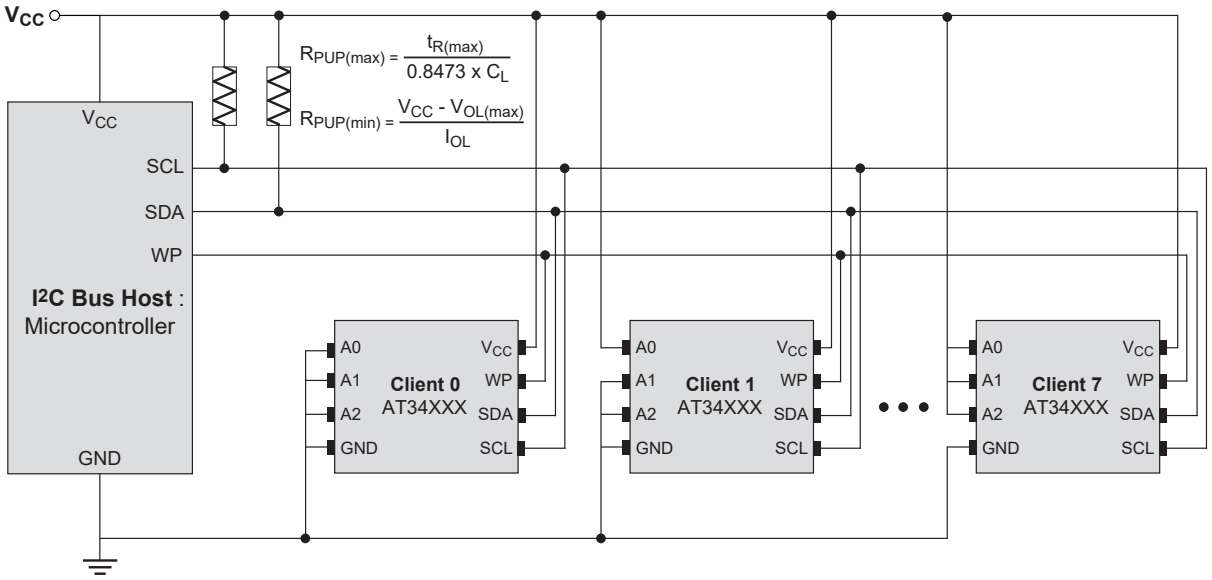
3. Description

The AT34C02D is designed to support the JEDEC EE1002 and EE1002A Serial Presence Detect (SPD) function used in DDR, DDR2 and DDR3 Dual Inline Memory Modules (DIMM). The AT34C02D provides 2,048 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 256 words of 8 bits each. The device's cascading feature allows up to eight devices to share a common two-wire bus.

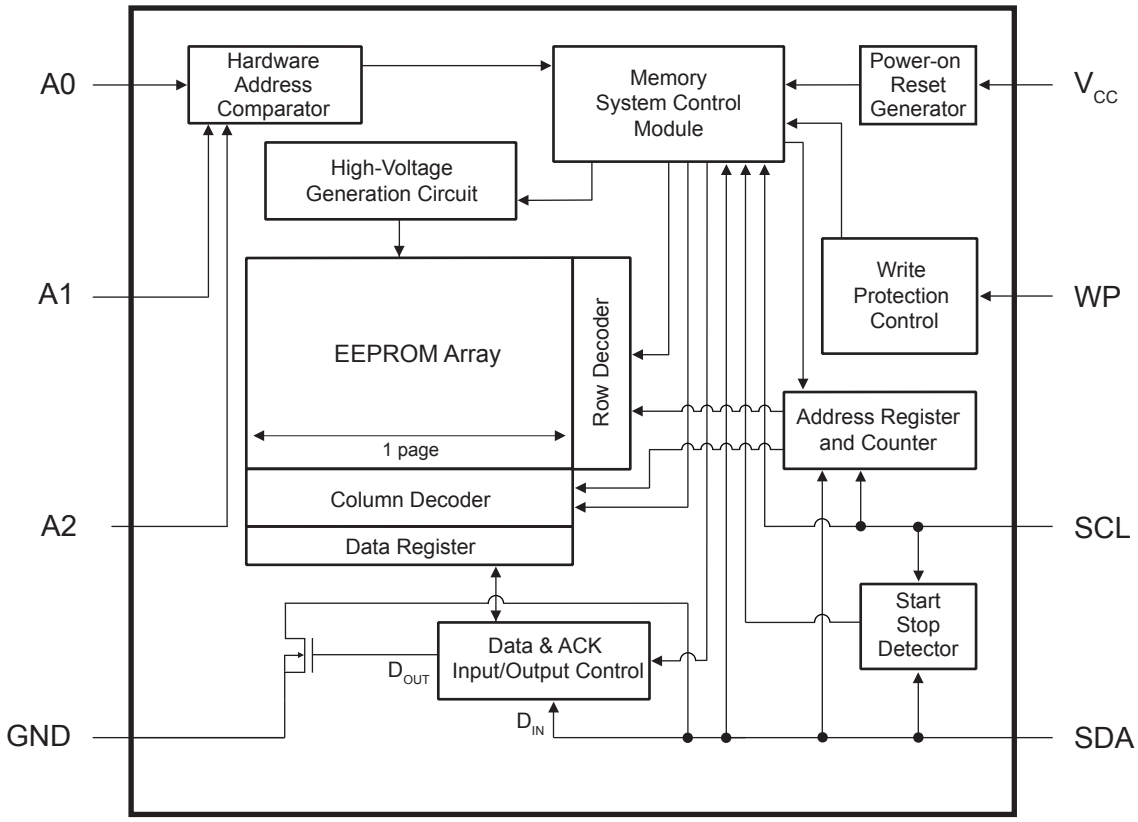
The first-half of the AT34C02D incorporates a permanent and a reversible software write protection feature while a hardware write-protect feature for the entire array is available via an external pin. The permanent software write protection is enabled by sending a special command to the device. This protection cannot be reversed once executed. However, the reversible software write protection can be reversed by sending and executing a special command. The hardware write protection is controlled by the WP pin state and can be used to protect the entire array, regardless of whether or not the software write protection has been enabled. The software and hardware write protection features allow the user the flexibility to protect no portion of the memory, the first-half of the memory, or the entire memory array depending on the specific needs of the application.

The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The device is available in space-saving 8- lead SOIC, 8-lead TSSOP, 8-pad UDFN and 8-ball VFBGA packages. All packages operate from 1.7V to 5.5V.

3.1 System Configuration Using Two-Wire Serial EEPROMs



3.2 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
V_{CC}	6.25V
Voltage on any pin with respect to ground	-1.0V to +7.0V
DC output current	5.0 mA
ESD protection	>4 kV

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

AT34C02D		
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low-Voltage Grade	1.7V to 5.5V

4.3 DC Characteristics

Table 4-2. DC Characteristics

Parameter	Symbol	Minimum	Typical(1)	Maximum	Units	Test Conditions
Supply Voltage	V_{CC}	1.7	—	5.5	V	
Supply Current	I_{CC1}	—	1.0	2.0	mA	V_{CC} = 5.0V, Read at 400 kHz
Supply Current	I_{CC2}	—	2.0	3.0	mA	V_{CC} = 5.0V, Write at 400 kHz
Standby Current	I_{SB}	—	—	1.0	µA	V_{CC} = 1.7V, V_{IN} = V_{CC} or GND
		—	—	3.0	µA	V_{CC} = 3.6V, V_{IN} = V_{CC} or GND
		—	—	6.0	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, A0 = GND
Input Leakage Current	I_{LI}	—	0.10	3.0	µA	V_{IN} = V_{CC} or GND
Output Leakage Current	I_{LO}	—	0.05	3.0	µA	V_{OUT} = V_{CC} or GND
Input Low Level	V_{IL}	-0.6	—	V_{CC} x 0.3	V	Note 2
Input High Level	V_{IH}	V_{CC} x 0.7	—	V_{CC} + 0.5	V	Note 2
Output Low Level	V_{OL1}	—	—	0.2	V	V_{CC} = 1.7V, I_{OL} = 0.15 mA
Output Low Level	V_{OL2}	—	—	0.4	V	V_{CC} = 3.0V, I_{OL} = 2.1 mA

Notes:

1. Typical values characterized at T_A = +25°C unless otherwise noted.
2. This parameter is characterized but is not 100% tested in production.

4.4 AC Characteristics

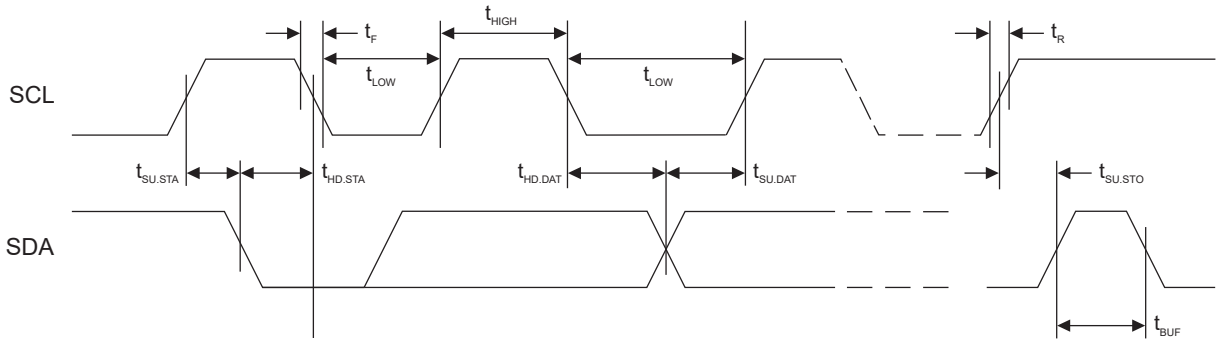
Table 4-3. AC Characteristics[1]

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Units
		V_{CC} = 1.7V to 3.6V		V_{CC} = 1.7V to 3.6V		V_{CC} = 3.6V to 5.5V		
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency, SCL	f_{SCL}	—	100	—	400	—	1000	kHz
Clock Pulse Width Low	t_{LOW}	4,700	—	1,300	—	400	—	ns
Clock Pulse Width High	t_{HIGH}	4,000	—	600	—	400	—	ns
Input Filter Spike Suppression	t_I	—	100	—	100	—	50	ns
Bus Free Time between Stop and Start	t_{BUF}	4,700	—	1,300	—	500	—	ns
Start Hold Time	$t_{HD.STA}$	4,000	—	600	—	250	—	ns
Start Set-Up Time	$t_{SU.STA}$	4,700	—	600	—	250	—	ns
Data In Hold Time	$t_{HD.DI}$	0	—	0	—	0	—	ns
Data In Set-up Time	$t_{SU.DAT}$	250	—	100	—	100	—	ns
Inputs Rise Time[2]	t_R	1,000	—	—	300	—	100	ns
Inputs Fall Time[2]	t_F	300	—	—	300	—	100	ns
Stop Set-Up Time	$t_{SU.STO}$	4,000	—	600	—	250	—	ns
Data Out Hold Time	$t_{DH.DAT}$	200	3,450	200	900	50	550	ns
Write Cycle Time	t_{WR}	—	5	—	5	—	5	ms

Notes:

1. AC measurement conditions:
   - C_L: 100 pF
   - R_{PUP} (SDA bus line pull-up resistor to V_{CC}): 1.3 kΩ (1000 kHz), 4 kΩ (400 kHz), 10 kΩ (100 kHz)
   - Input pulse voltages: 0.3 x V_{CC} to 0.7 x V_{CC}
   - Input rise and fall times: ≤50 ns
   - Input and output timing reference voltages: 0.5 x V_{CC}
2. These parameters are determined through product characterization and are not 100% tested in production.

Figure 4-1. Bus Timing



4.5 Electrical Specifications

4.5.1 Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT34C02D should monotonically rise from GND to the minimum V_{CC} level (as specified in Table 4-1), with a slew rate no faster than 0.1 V/µs.

4.5.1.1 Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT34C02D includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once the V_{CC} is greater than or equal to the minimum V_{CC} level, the bus host must wait at least t_{PUP} before sending the first command to the device. See Table 4-4 for the values associated with these power-up parameters.

Table 4-4. Power-up Conditions(1)

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept commands	100	—	µs
V_{POR}	Power-on Reset Threshold Voltage	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles	500	—	ms

Note:

1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT34C02D drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed. First, drive the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time, and then perform a new power-up sequence in compliance with the requirements defined in this section.

4.5.2 Pin Capacitance

Table 4-5. Pin Capacitance(1)

Symbol	Test Condition	Max.	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A0, A1, A2 and SCL)	6	pF	V_{IN} = 0V

Note:

1. This parameter is characterized but is not 100% tested in production.

4.5.3 EEPROM Cell Performance Characteristics

Table 4-6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance(1)	T_A = 25°C, V_{CC} = 3.3V, Page Write mode	1,000,000	—	Write Cycles
Data Retention(1)	T_A = 55°C	100	—	Years

Note:

1. Performance is determined through characterization and the qualification process.

5. Device Operation and Communication

The AT34C02D operates as a client device and utilizes a simple I^2C-compatible two-wire digital serial interface to communicate with a host controller, commonly referred to as the bus host. The host initiates and controls all read and write operations to the client devices on the serial bus, and both the host and the client devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the host, while the bidirectional SDA pin is used to receive command and data information from the host as well as to send data back to the host. Data is always latched into the AT34C02D on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pins incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant bit (MSb) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an Acknowledge (ACK) or a No-Acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the host. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any read or write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the host and the client devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the host. In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic high state at the same time.

5.1 Clock and Data Transition Requirements

The SDA pin is an open-drain terminal and therefore must be pulled high with an external pull-up resistor. SCL is an input pin that can either be driven high or pulled high using an external pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below. The relationship of the AC timing parameters with respect to SCL and SDA for the AT34C02D are shown in the timing waveform in Figure 4-1. The AC timing characteristics and specifications are outlined in AC Characteristics.

5.2 Start and Stop Conditions

5.2.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable logic '1' state and will bring the device out of Standby mode. The host uses a Start condition to initiate any data transfer sequence; therefore, every command must begin with a Start condition. The device will continuously monitor the SDA and SCL pins for a Start condition but will not respond unless one is detected. Refer to Figure 5-1 for more details.

5.2.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the logic '1' state.

The host can use the Stop condition to end a data transfer sequence with the AT34C02D, which will subsequently return to Standby mode. The host can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the host will perform another operation. Refer to Figure 5-1 for more details.

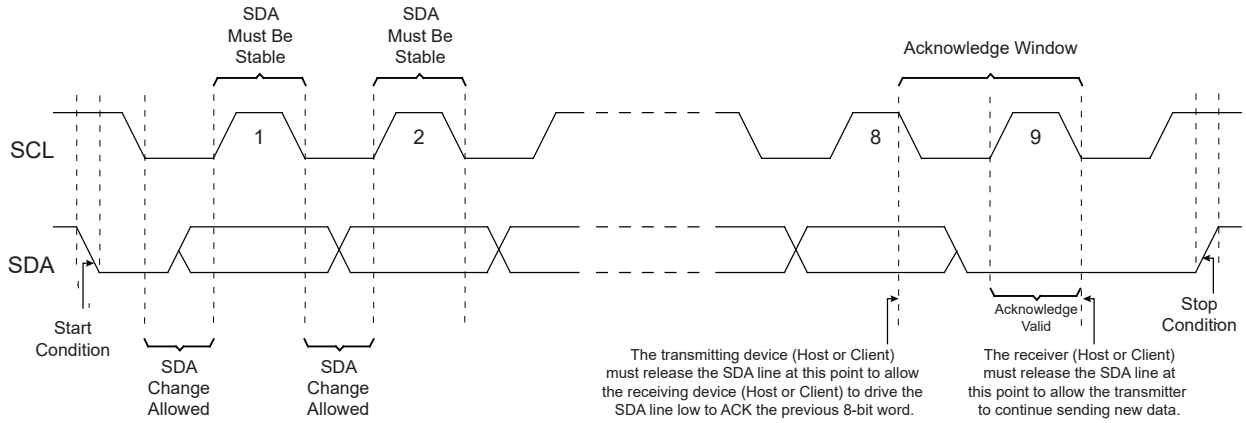
5.3 Acknowledge and No-Acknowledge

After every byte of data is received, the receiving device must confirm to the transmitting device that it has successfully received the data byte by responding with what is known as an Acknowledge (ACK). An ACK is accomplished by the transmitting device first releasing the SDA line at the falling edge of the eighth clock cycle followed by the receiving device responding with a logic '0' during the entire high period of the ninth clock cycle.

When the AT34C02D is transmitting data to the host, the host can indicate that it is done receiving data and wants to end the operation by sending a logic '1' response to the AT34C02D instead of an ACK response during the ninth clock cycle. This is known as a No-Acknowledge (NACK) and is accomplished by the host sending a logic '1' during the ninth clock cycle, at which point the AT34C02D will release the SDA line so the host can then generate a Stop condition.

The transmitting device, which can be the bus host or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle to allow the receiving device to drive the SDA line to a logic '0' to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram has been provided in Figure 5-1 to better illustrate these requirements.

Figure 5-1. Start Condition, Data Transitions, Stop Condition and Acknowledge



5.4 Standby Mode

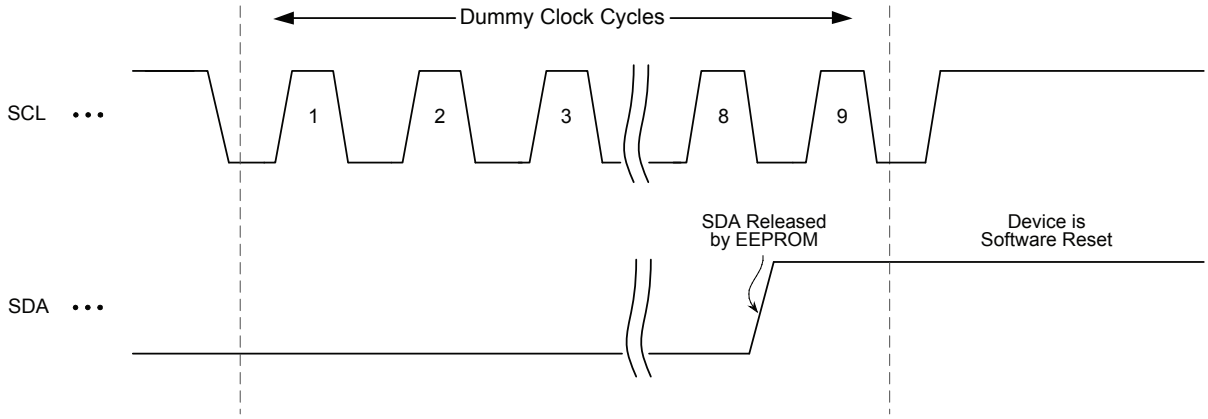
The AT34C02D features a low-power Standby mode that is enabled when any one of the following occurs:

- A valid power-up sequence is performed (see Power-Up Requirements and Reset Behavior).
- A Stop condition is received by the device unless it initiates an internal write cycle (see Write Operations).
- At the completion of an internal write cycle (see Write Operations).

5.5 Software Reset

After an interruption in protocol, power loss or system Reset, any two-wire device can be protocol reset by clocking SCL until SDA is released by the EEPROM and goes high. The number of clock cycles until SDA is released by the EEPROM will vary. The software Reset sequence should not take more than nine dummy clock cycles. Once the software Reset sequence is complete, new protocol can be sent to the device by sending a Start condition followed by the protocol. Refer to Figure 5-2 for an illustration.

Figure 5-2. Software Reset



In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device (see Power-Up Requirements and Reset Behavior).

6. Memory Organization

The AT34C02D is internally organized as 16 pages of 16 bytes each.

6.1 Device Addressing

Accessing the device requires an 8-bit device address byte following a Start condition to enable the device for a read or write operation. Since multiple client devices can reside on the serial bus, each client device must have its own unique address so the host can access each device independently.

The Most Significant four bits of the device address byte is referred to as the device type identifier. The device type identifier '1010' (Ah) for the main EEPROM access and '0110' (6h) for the Write-Protect registers access is required in bits 7 through 4 of the device address byte (see Table 6-1).

Following the 4-bit device type identifier are the hardware client address bits, A2, A1 and A0. These bits can be used to expand the address space by allowing up to eight Serial EEPROM devices on the same bus. These hardware client address bits must correlate with the voltage level on the corresponding hardwired device address input pins A0, A1 and A2. The A0, A1 and A2 pins use an internal proprietary circuit that automatically biases the pin to a logic '0' state if the pin is allowed to float. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once the pin is biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Microchip recommends connecting the A0, A1 and A2 pins to a known state whenever possible.

The eighth bit (bit 0) of the device address byte is the Read/Write Select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon the successful comparison of the device address byte, the AT34C02D will return an ACK. If a valid comparison is not made, the device will NACK. The device will NACK if the Write-Protect register has been programmed and the device type identifier is '0110' (6h).

Table 6-1. Device Address Byte

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Write-Protect Registers	0	1	1	0	A2	A1	A0	R/$\overline{W}$

For all operations except the current address read, a word address byte must be transmitted to the device immediately following the device address byte. The word address byte contains a 8-bit memory array word address, and is used to specify which byte location in the EEPROM to start reading or writing. Refer to Table 6-2 to review these bit positions.

Table 6-2. Word Address Byte

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	A7	A6	A5	A4	A3	A2	A1	A0
Write-Protect Registers	X	X	X	X	X	X	X	X

Note: X indicates a "don't care" bit.

7. Write Operations

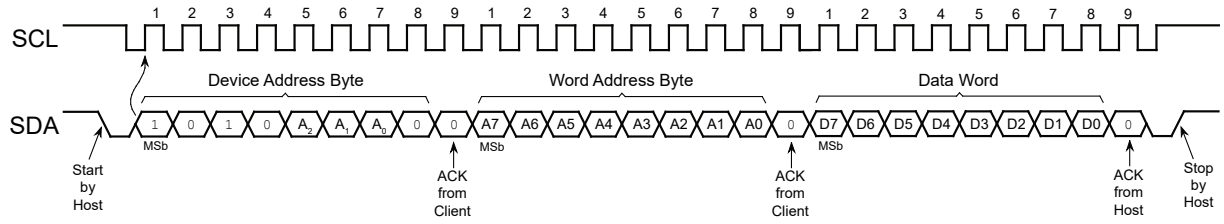
All write operations for the AT34C02D begin with the host sending a Start condition, followed by a device address byte with the R/$\overline{W}$ bit set to logic '0', and then by the word address byte. The data value(s) to be written to the device immediately follow the word address byte.

7.1 Byte Write

The AT34C02D supports the writing of a single 8-bit byte. Selecting a data word in the AT34C02D requires a 7-bit word address.

Upon receipt of the proper device address and the word address bytes, the EEPROM will send an Acknowledge. The device will then be ready to receive the 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will respond with an ACK. The addressing device, such as a bus host, must then terminate the write operation with a Stop condition. At that time, the EEPROM will enter an internally self-timed write cycle, which will be completed within t_{WR}, while the data word is being programmed into the nonvolatile EEPROM. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.

Figure 7-1. Byte Write



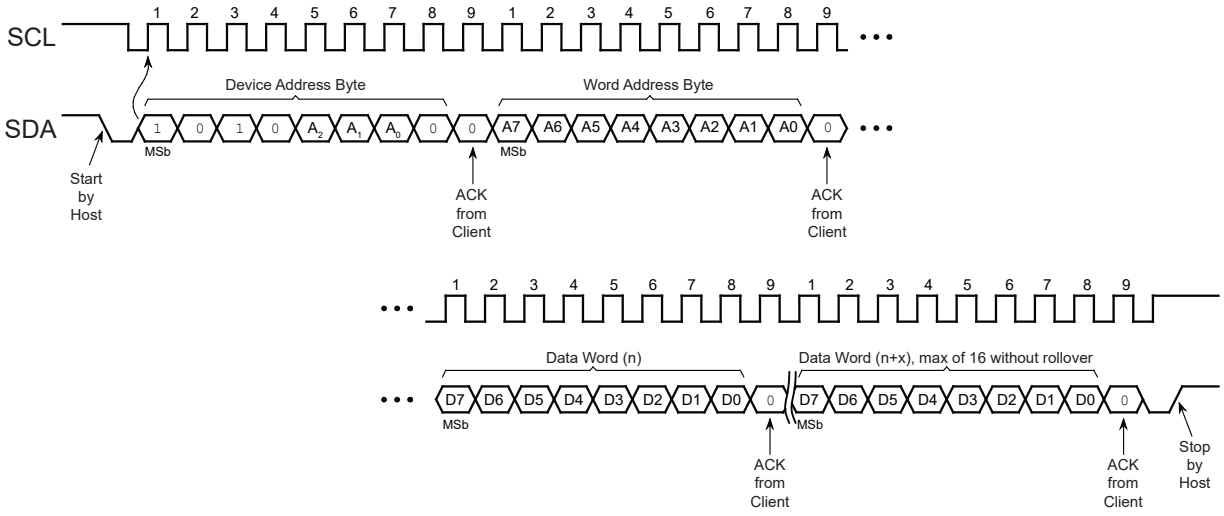
7.2 Page Write

A page write operation allows up to 16 bytes to be written in the same write cycle, provided all bytes are in the same row of the memory array (where address bits A7 to A4 are the same). Partial page writes of less than 16 bytes are also allowed.

A page write is initiated the same way as a byte write, but the bus host does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the bus host can transmit up to fifteen additional data words. The EEPROM will respond with an ACK after each data word is received. Once all data to be written has been sent to the device, the bus host must issue a Stop condition (see Figure 7-2) at which time the internally self-timed write cycle will begin.

The lower four bits of the word address are internally incremented following the receipt of each data word. The higher order address bits are not incremented and retain the memory page row location. Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. When the incremented word address reaches the page boundary, the address counter will rollover to the beginning of the same page. Nevertheless, creating a rollover event should be avoided as previously loaded data in the page could become unintentionally altered.

Figure 7-2. Page Write

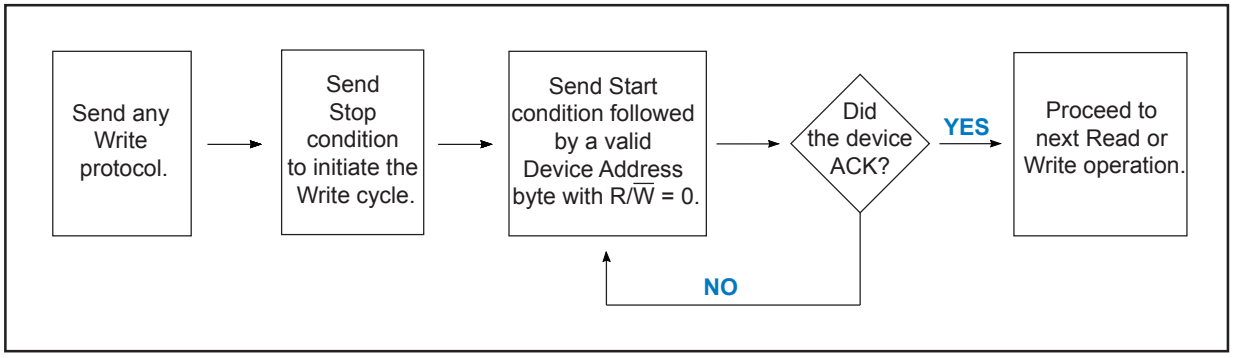


7.3 Acknowledge Polling

An Acknowledge Polling routine can be implemented to optimize time-sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}). This method allows the application to know immediately when the Serial EEPROM write cycle has completed, so a subsequent operation can be started.

Once the internally self-timed write cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid device address byte with the R/$\overline{W}$ bit set at logic '0'. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write cycle has completed, the EEPROM will respond with an ACK, allowing a new read or write operation to be immediately initiated. A flowchart has been included below in Figure 7-3 to better illustrate this technique.

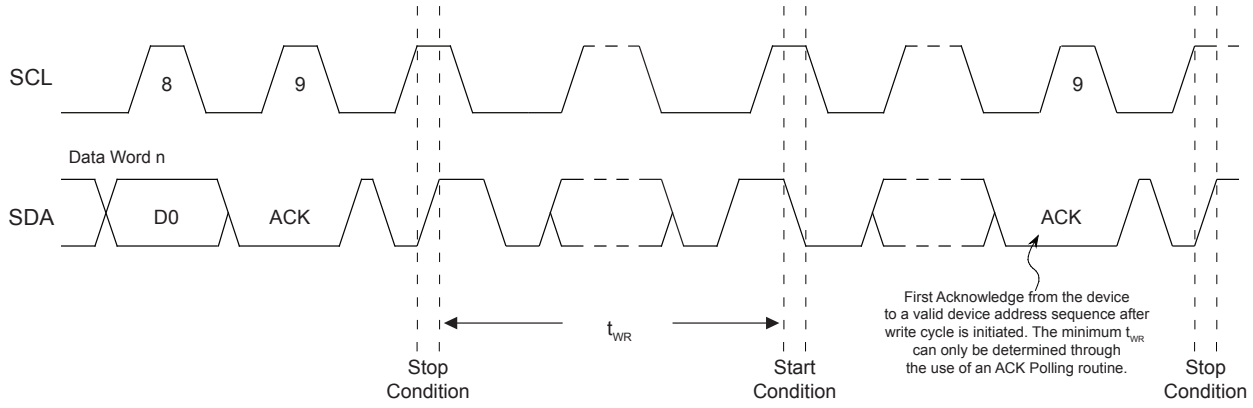
Figure 7-3. Acknowledge Polling Flowchart



7.4 Write Cycle Timing

The length of the self-timed write cycle (t_{WR}) is defined as the amount of time from the Stop condition that begins the internal write cycle to the Start condition of the first device address byte sent to the AT34C02D that it subsequently responds to with an ACK. Figure 7-4 has been included to show this measurement. During the internally self-timed write cycle, any attempts to read from or write to the memory array will not be processed.

Figure 7-4. Write Cycle Timing



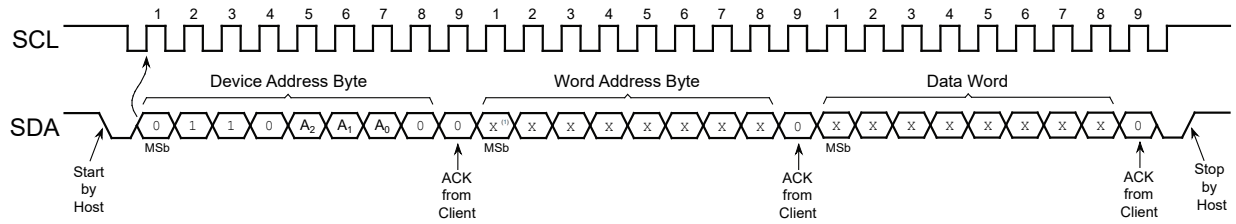
7.5 Write Protection

Once enabled, the Software Write Protection write protects only the first-half of the array (00h - 7Fh) while the hardware write protection, via the WP pin, is used to protect the entire array (see Hardware Write Protection).

7.5.1 Permanent Software Write Protection (PSWP)

The Permanent Software Write Protection (PSWP) is enabled by sending a command to the device, similar to a normal write operation, which programs the Permanent Write-Protect register. This must be done with the WP pin low. The Write-Protect register is programmed by sending a write command with the device type identifier of '0110' (6h) instead of '1010' (Ah) with the address and data bit(s) being don't cares. The write cycle time must be observed. Once the PSWP has been enabled, the device will no longer acknowledge the '0110' (6h) device type identifier and cannot be reversed even if the device is powered down.

Figure 7-5. Setting Permanent Write-Protect Register (PSWP)



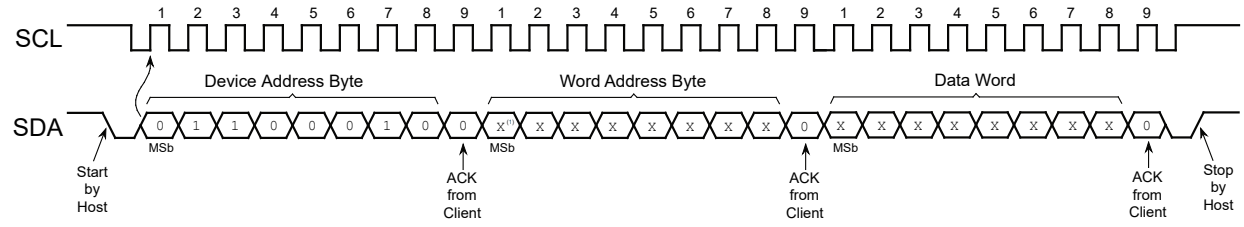
Note:

1. X is a "don't care" bit.

7.5.2 Reversible Software Write Protection (RSWP)

The Reversible Software Write Protection (RSWP) is enabled by sending a command to the device, similar to a normal write operation, which programs the Reversible Write-Protect register. This must be done with the WP pin low. The RSWP is programmed by sending a write command '01100010'(62h) with pins A2 and A1 tied to ground or not connected and the A0 pin connected to V_{HV} (see Figure 7-6 and Table 7-1). The RSWP or write protection can be reversed by sending a command '01100110' (66h) with the A2 pin tied to ground or no connect, the A1 pin tied to V_{CC} and the A0 pin tied to V_{HV} (see Figure 7-7 and Table 7-1).

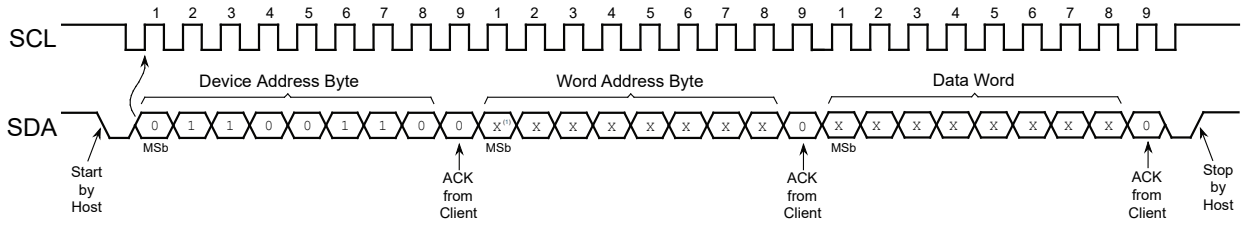
Figure 7-6. Setting Reversible Write-Protect Register (RSWP)



Note:

1. X is a “don’t care” bit.

Figure 7-7. Clearing Reversible Write-Protect Register (RSWP)



Note:

1. X is a “don’t care” bit.

Table 7-1. V_{HV}

	Min.	Max.	Units
V_{HV}	7	10	V

Note: $V_{HV} - V_{CC} > 4.8V$

7.5.3 Hardware Write Protection

The WP pin can be connected to V_{CC}, GND, or left floating. Connecting the WP pin to V_{CC} will write-protect the entire array regardless of whether or not the Software Write Protection has been enabled or invoked (see Table 7-3 and Table 7-4). The Software Write Protection register cannot be programmed when the WP pin is connected to V_{CC}. If the WP pin is connected to GND or left floating, the write protection mode is determined by the status of the Software Write-Protect register.

Table 7-2. Write Protection

Command	Pin			Preamble							R/$\overline{W}$
	A2	A1	A0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set PSWP	A2	A1	A0	0	1	1	0	A2	A1	A0	0
Set RSWP	0	0	V_{HV}	0	1	1	0	0	0	1	0
Clear RSWP	0	V_{CC}	V_{HV}	0	1	1	0	0	1	1	0

Table 7-3. WP Connected to GND or Floating

WP Connected to GND or Floating					
Command	**R/$\overline{W}$ Bit**	**Permanent Write-Protect Register PSWP**	**Reversible Write-Protect Register RSWP**	**Response from Device**	**Action from Device**
1010	R	X	X	ACK	Read Array.
1010	W	Programmed	X	ACK	Can write to second-half (80h - FFh) only.
1010	W	X	Programmed	ACK	Can write to second-half (80h - FFh) only.
1010	W	Not Programmed	Not Programmed	ACK	Can write to full array.
Read PSWP	R	Programmed	X	NACK	STOP – Indicates Permanent Write-Protect register is programmed.
Read PSWP	R	Not Programmed	X	ACK	Data read out is undefined. Indicates PSWP register is not programmed.
Set PSWP	W	Programmed	X	NACK	STOP – Indicates Permanent Write-Protect register is programmed.
Set PSWP	W	Not Programmed	X	ACK	Program Permanent Write-Protect register (irreversible).
Read RSWP	R	X	Programmed	NACK	STOP – Indicates Permanent Write-Protect register is programmed.
Read RSWP	R	X	Not Programmed	ACK	Data read out is undefined. Indicates RSWP register is not programmed.
Set RSWP	W	X	Programmed	NACK	STOP – Indicates Reversible Write-Protect register is programmed.
Set RSWP	W	X	Not Programmed	ACK	Program Reversible Write-Protect register (reversible).
Clear RSWP	W	Programmed	X	NACK	STOP – Indicates Permanent Write-Protect register is programmed.
Clear RSWP	W	Not Programmed	X	ACK	Clear (unprogram) Reversible Write-Protect register (reversible).

Table 7-4. WP Connected to V_{CC}

WP Connected to V_{CC}					
Command	**R/$\overline{W}$ Bit**	**Permanent Write-Protect Register PSWP**	**Reversible Write-Protect Register RSWP**	**Response from Device**	**Action from Device**
1010	R	X	X	ACK	Read array.
1010	W	X	X	ACK	Device is write protected.
Read PSWP	R	Programmed	X	NACK	STOP – Indicates Permanent Write-Protect register is programmed.
Read PSWP	R	Not Programmed	X	ACK	Data read out is undefined. Indicates PSWP register is not programmed.

.....continued

WP Connected to V_{CC}					
Command	**R/$\overline{W}$ Bit**	**Permanent Write-Protect Register PSWP**	**Reversible Write-Protect Register RSWP**	**Response from Device**	**Action from Device**
Set PSWP	W	Programmed	X	NACK	STOP – Indicates Permanent Write-Protect register is programmed.
Set PSWP	W	Not Programmed	X	ACK	Cannot program write-protect registers.
Read RSWP	R	X	Programmed	NACK	STOP – Indicates Reversible Write-Protect register is programmed.
Read RSWP	R	X	Not Programmed	ACK	Data read out is undefined. Indicates RSWP register is not programmed.
Set RSWP	W	X	Programmed	NACK	STOP – Indicates Reversible Write-Protect register is programmed.
Set RSWP	W	X	Not Programmed	ACK	Cannot program write-protect registers.
Clear RSWP	W	Programmed	X	NACK	STOP – Indicates Permanent Write-Protect register is programmed.
Clear RSWP	W	Not Programmed	X	ACK	Cannot write to Write-Protect registers.

8. Read Operations

Read operations are initiated the same way as write operations with the exception that the Read/Write Select bit in the device address byte must be a logic '1'. There are three read operations:

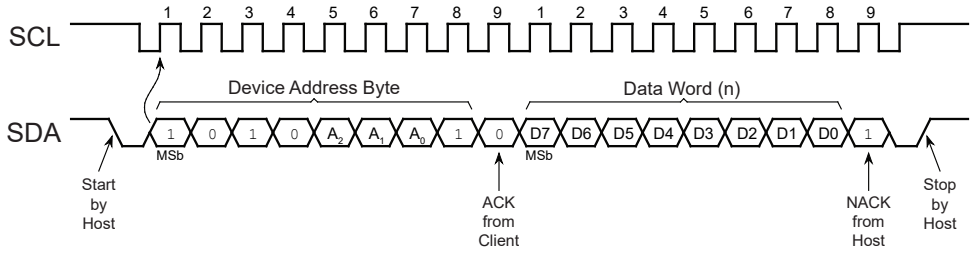
- Current Address Read
- Random Address Read
- Sequential Read

8.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the V_{CC} is maintained to the part. The address rollover during a read is from the last byte of the last page to the first byte of the first page of the memory.

A current address read operation will output data according to the location of the internal data word address counter. This is initiated with a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. The device will ACK this sequence and the current address data word is serially clocked out on the SDA line. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol or it can send a Start condition to begin the next sequence.

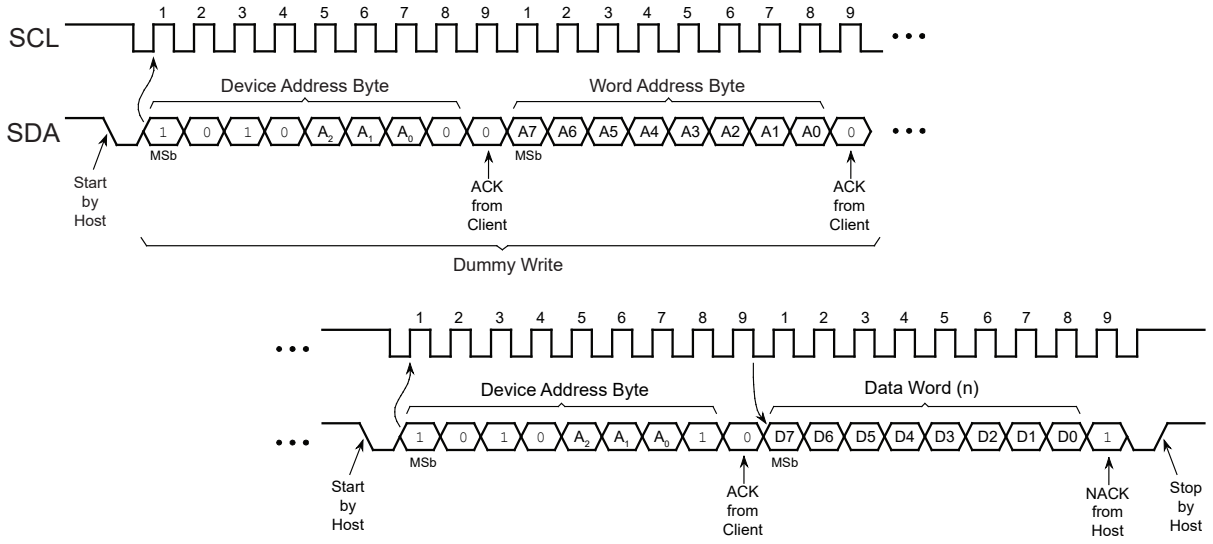
Figure 8-1. Current Address Read



8.2 Random Read

A random read begins in the same way as a byte write operation does to load in a new data word address. This is known as a "dummy write" sequence; however, the data byte and the Stop condition of the byte write must be omitted to prevent the part from entering an internal write cycle. Once the device address and word address are clocked in and acknowledged by the EEPROM, the bus host must generate another Start condition. The bus host now initiates a current address read by sending a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. The EEPROM will ACK the device address and serially clock out the data word on the SDA line. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

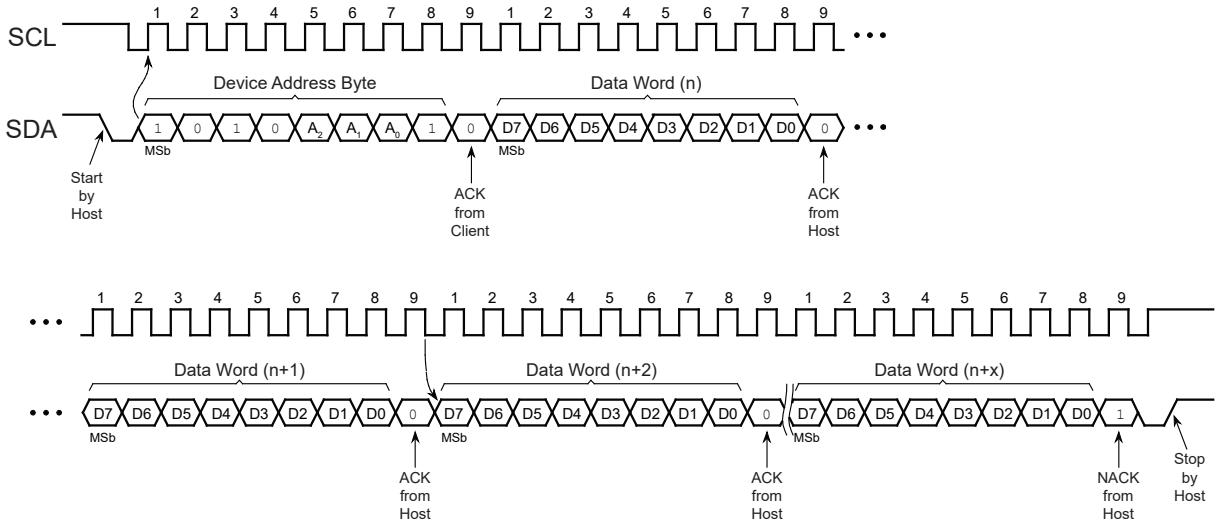
Figure 8-2. Random Read



8.3 Sequential Read

Sequential reads are initiated by either a current address read or a random read. After the bus host receives a data word, it responds with an Acknowledge. As long as the EEPROM receives an ACK, it will continue to increment the word address and serially clock out sequential data words. When the maximum memory address is reached, the data word address will rollover and the sequential read will continue from the beginning of the memory array. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol or it can send a Start condition to begin the next sequence.

Figure 8-3. Sequential Read



8.4 Checking the Write-Protect Registers Status

8.4.1 Checking the Permanent Write-Protect Register (PSWP) Status

Determining the status of the Permanent Write-Protect register can be accomplished by sending a similar command to the device as was used when programming the register, except the R/$\overline{W}$ bit must be set to one. If the device responds with an acknowledge, the Permanent Write-Protect register has not been programmed. Otherwise, it has been programmed and the first-half of the array is permanently write protected.

8.4.2 Checking the Reversible Write-Protect Register (RSWP) Status

Determining the status of the Reversible Write-Protect register can be accomplished by sending a similar command to the device as was used when programming the register, except the R/$\overline{W}$ bit must be set to one. If the device returns an acknowledge, the Reversible Write-Protect register has not been programmed. Otherwise, it has been programmed and the first-half of the array is write protected, but remains reversible.

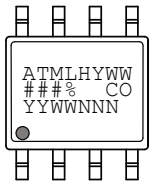
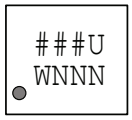
Table 8-1. PSWP and RSWP Status

Command	Pin			Preamble							R/$\overline{W}$
	A2	A1	A0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read PSWP	A2	A1	A0	0	1	1	0	A2	A1	A0	1
Read RSWP	0	0	A0	0	1	1	0	0	0	1	1

9. Packaging Information

9.1 Package Marking Information

AT34C02D: Package Marking Information

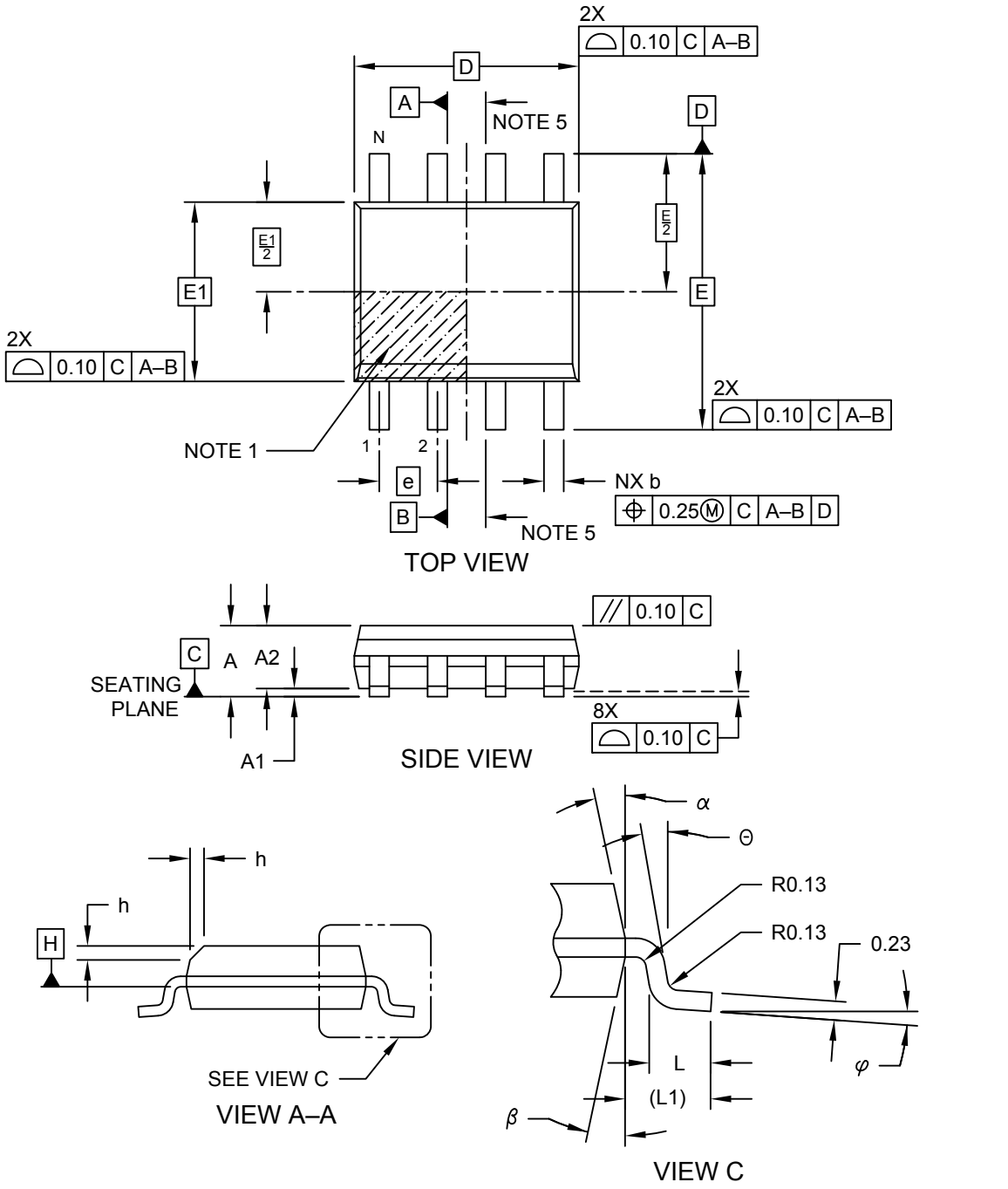
8-lead SOIC	8-lead TSSOP
	
8-pad UDFN	**8-ball VFBGA**
2.0 x 3.0 mm Body 	1.5 x 2.0 mm Body 

Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

Catalog Number Truncation					
AT34C02D			Truncation Code ##: 34D		
Date Codes					**Voltages**
YY = Year		Y = Year		WW = Work Week of Assembly	% = Minimum Voltage
16: 2016	20: 2020	6: 2016	0: 2020	02: Week 2	M: 1.7V min
17: 2017	21: 2021	7: 2017	1: 2021	04: Week 4	
18: 2018	22: 2022	8: 2018	2: 2022	...	
19: 2019	23: 2023	9: 2019	3: 2023	52: Week 52	
Country of Origin		**Device Grade**			**Atmel Truncation**
CO = Country of Origin		H or U: Industrial Grade			AT: Atmel ATM: Atmel ATML: Atmel
Trace Code					
NNN = Alphanumeric Trace Code (2 Characters for Small Packages)					

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

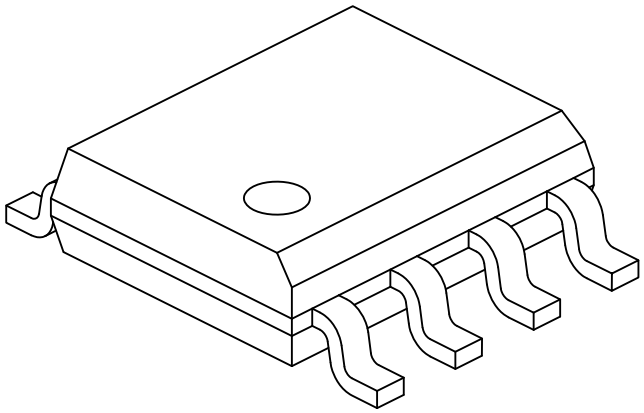
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

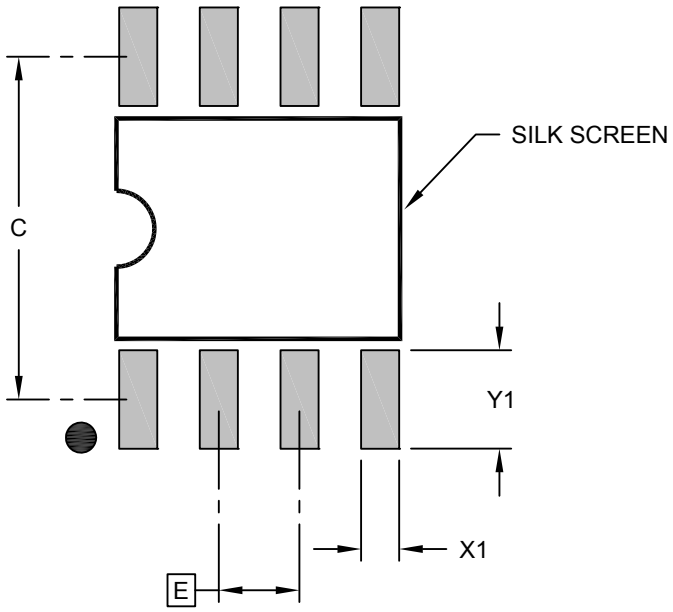
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

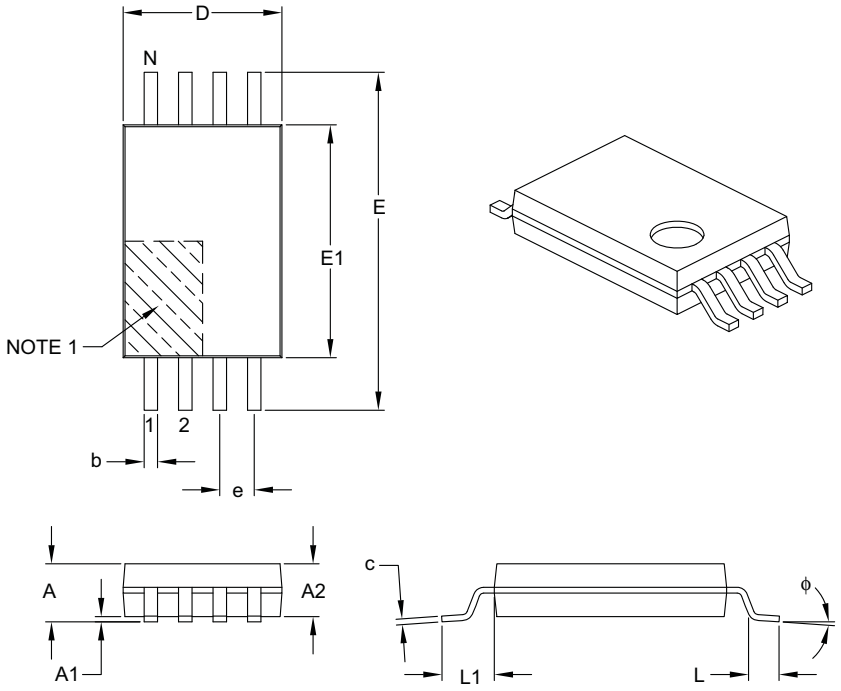
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

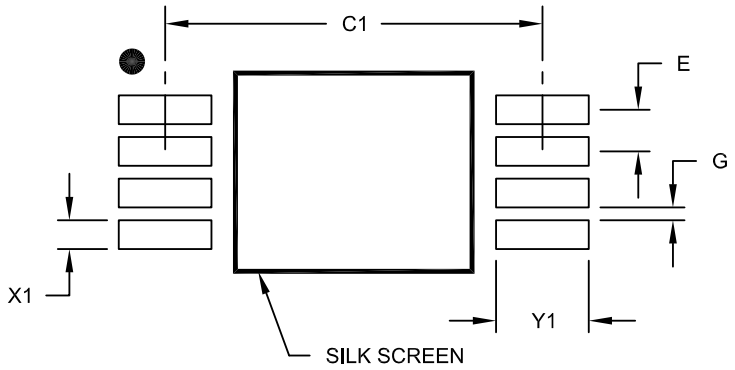
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

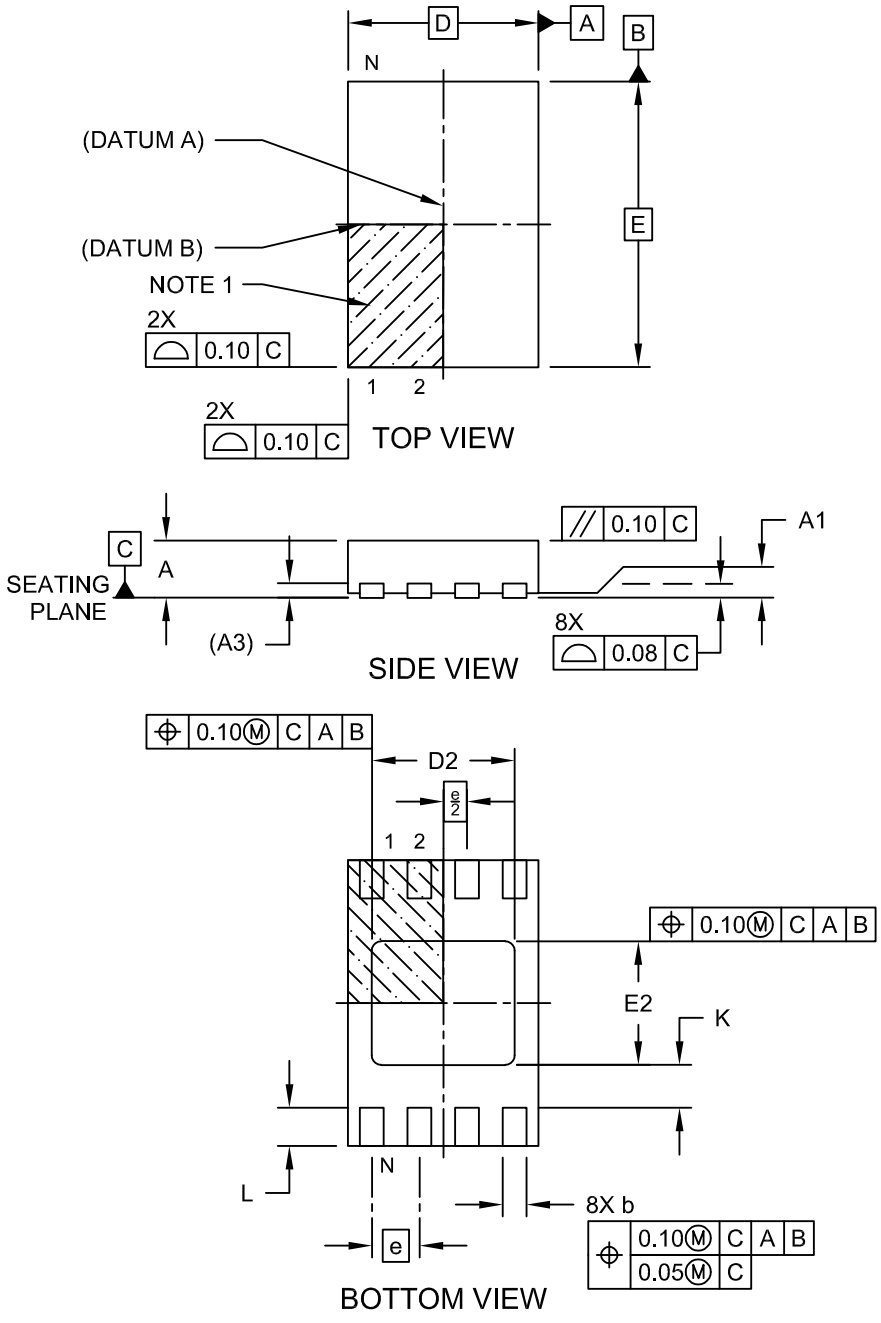
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

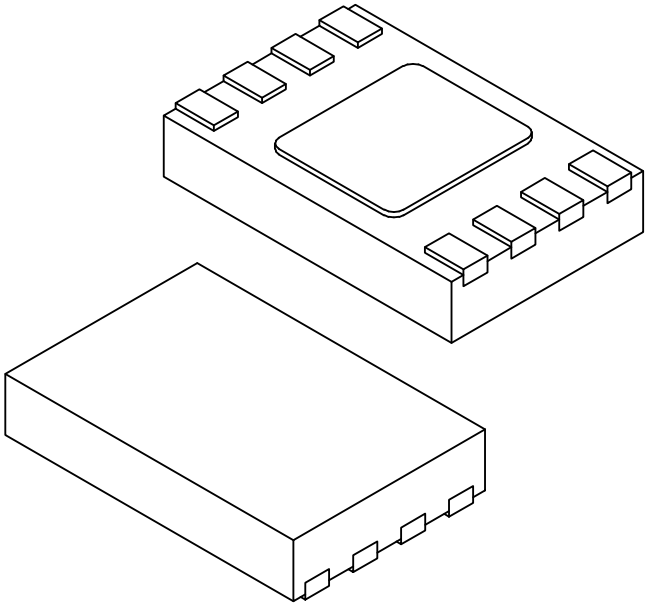
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 1 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.25	0.35	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

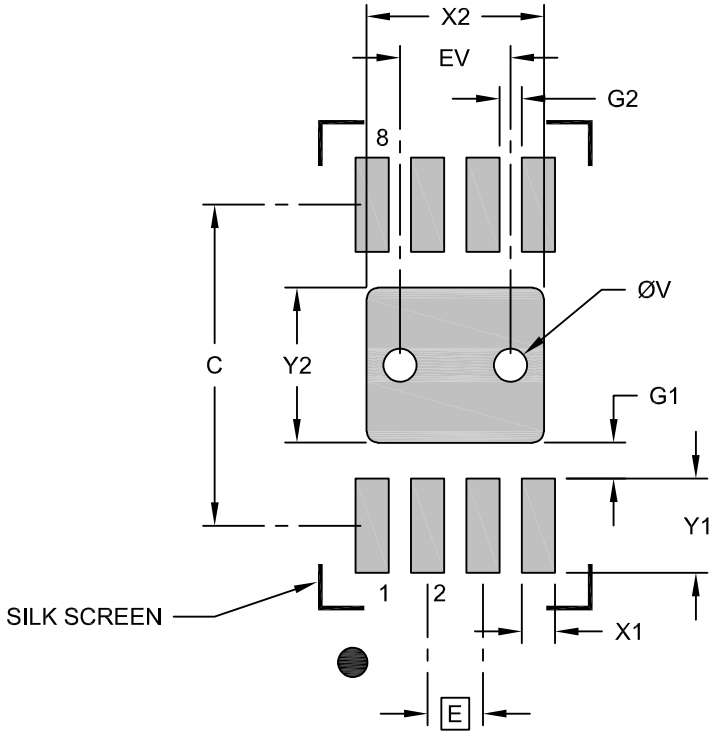
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 2 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



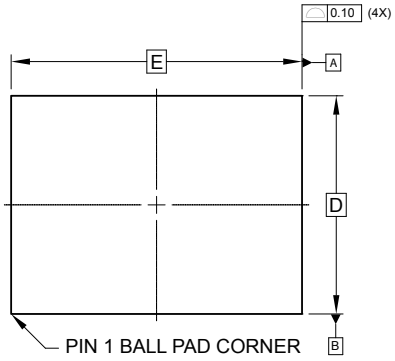
RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

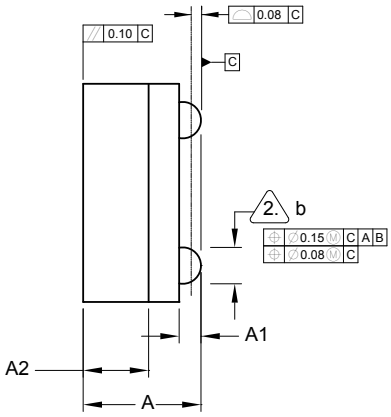
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

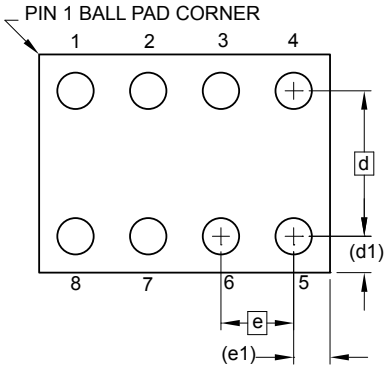
Microchip Technology Drawing C04-23355-Q4B Rev C



TOP VIEW



SIDE VIEW



BOTTOM VIEW
8 SOLDER BALLS

Notes:

1. This drawing is for general information only.
2. Dimension ‘b’ is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.0 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

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	TITLE	GPC	DRAWING NO.	REV.
	8U3-1, 8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)	GXU	8U3-1	G

Note: For the most current package drawings, please see the Microchip Packaging Specification located at www.microchip.com/packaging.

10. Revision History

Revision A (December 2020)
Updated to Microchip template. Microchip DS20006480 replaces Atmel document 8781. Updated Part Marking Information. Updated the "Software Reset" section. Added ESD rating. Removed lead finish designation. Updated trace code format in package markings. Added a figure for “System Configuration Using Two-Wire Serial EEPROMs”. Updated "Block Diagram" figure. Added POR recommendations section. Updated formatting to current template. Replaced terminology "Master" and "Slave" with "Host" and "Client" respectively. Updated the 8U3-1 VFBGA package drawing. Updated the SOIC, TSSOP and UDFN package drawings to Microchip format.

Atmel Document 8781 Revision D (January 2015)
Add the UDFN Expanded Quantity Option and update the ordering information section. Update the 8MA2 package outline drawing.

Atmel Document 8781 Revision C (July 2014)
Updated various language elements for consistency with JEDEC EE1002/1002A. Updated AC timing terminology for consistency with JEDEC EE1002/1002A. Added 100 kHz timing information for SPD applications using < 2.2V VCC supply. Miscellaneous formatting changes and text corrections. Update package drawings.

Atmel Document 8781 Revision B (June 2012)
Correct ordering code: AT34C02D-WWU11, Die Sale to AT34C02D-WWU11M, Wafer Sale. Update template.

Atmel Document 8781 Revision A (March 2012)
Initial document release.

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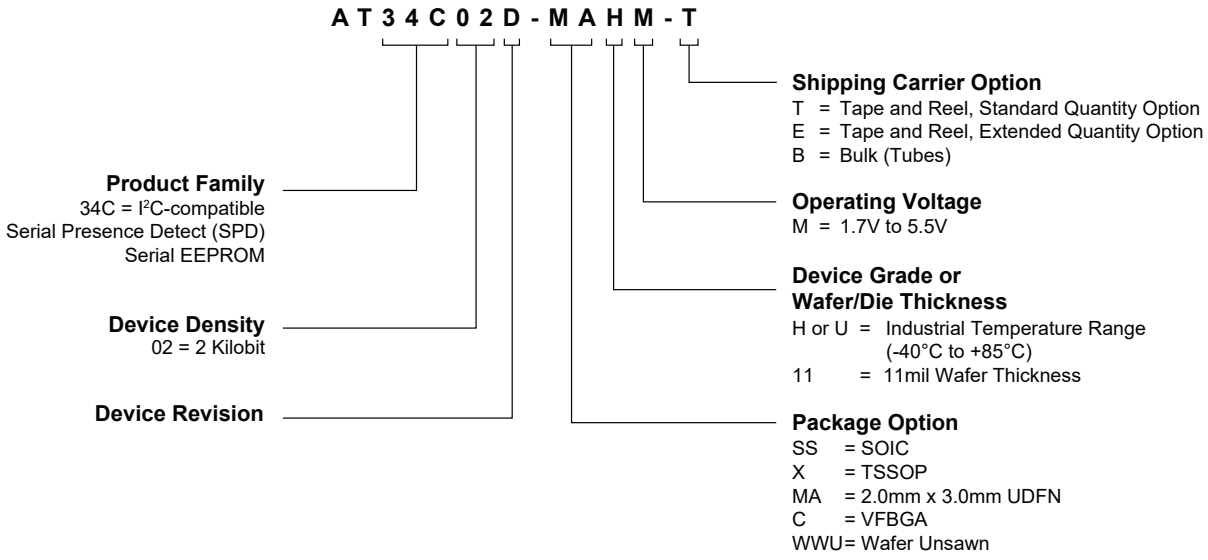

Examples

Device	Package	Package Drawing Code	Package Option	Shipping Carrier Option	Device Grade
AT34C02D-SSHM-B	SOIC	SN	SS	Bulk (Tubes)	Industrial Temperature (-40°C to 85°C)
AT34C02D-SSHM-T	SOIC	SN	SS	Tape and Reel	
AT34C02D-XHM-B	TSSOP	ST	X	Bulk (Tubes)	
AT34C02D-XHM-T	TSSOP	ST	X	Tape and Reel	
AT34C02D-MAHM-T	UDFN	Q4B	MA	Tape and Reel	
AT34C02D-MAHM-E	UDFN	Q4B	MA	Extended Qty. Tape and Reel	
AT34C02D-CUM-T	VFBGA	8U3-1	C	Tape and Reel	

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