25AA040A/25LC040A

4-Kbit SPI Bus Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25AA040A	1.8V-5.5V	16 bytes	I	MC, MS, P, OT, SN, MN, ST
25LC040A	2.5V-5.5V	16 bytes	I, E	MC, MS, P, OT, SN, MN, ST

Features

- 10 MHz Maximum Clock Speed
- Low-Power CMOS Technology:
  - Maximum Write current: 5 mA at 5.5V
  - Read current: 5 mA at 5.5V, 10 MHz
  - Standby current: 5 µA at 5.5V
- 512 x 8-bit Organization
- 16-Byte Page
- Sequential Read
- Self-Timed Erase and Write Cycles (5 ms maximum)
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-In Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- High Reliability:
  - Endurance: 1M erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4000V
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- RoHS Compliant
- Automotive AEC-Q100 Qualified

Packages

- 8-Lead DFN, 8-Lead MSOP, 8-Lead PDIP, 8-Lead SOIC, 6-Lead SOT23, 8-Lead TDFN and 8-Lead TSSOP

Pin Function Table

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write-Protect Pin
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
Vcc	Supply Voltage

Description

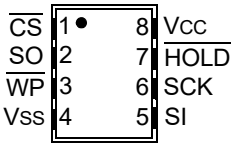
The Microchip Technology Inc. 25XX040A[(1)] is a 4-Kbit Serial Electrically Erasable PROM (EEPROM). The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

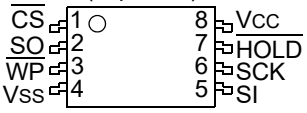
Note 1: 25XX040A is used in this document as a generic part number for the 25AA040A and 25LC040A devices.

Package Types (not to scale)

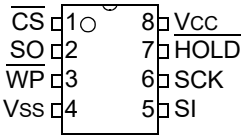
DFN/TDFN
(Top View)



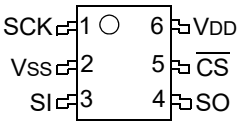
MSOP/TSSOP
(Top View)



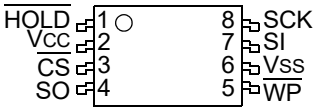
PDIP/SOIC
(Top View)



SOT-23
(Top View)



X-Rotated TSSOP
(Top View)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

V_{CC}.....6.5V

All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias .....-40°C to +125°C

ESD protection on all pins .....4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** **Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V** **Extended (E): T_A = -40°C to +125°C V_{CC} = 2.5V to 5.5V**			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	V_{IH1}	High-Level Input Voltage	0.7 V_{CC}	V_{CC} +1	V	
D002	V_{IL1}	Low-Level Input Voltage	-0.3	0.3 V_{CC}	V	$V_{CC} \geq$ 2.7V (**Note 1**)
D003	V_{IL2}		-0.3	0.2 V_{CC}	V	V_{CC} < 2.7V (**Note 1**)
D004	V_{OL}	Low-Level Output Voltage	—	0.4	V	I_{OL} = 2.1 mA
D005	V_{OL}		—	0.2	V	I_{OL} = 1.0 mA, V_{CC} = 2.5V
D006	V_{OH}	High-Level Output Voltage	V_{CC} -0.5	—	V	I_{OH} = -400 µA
D007	I_{LI}	Input Leakage Current	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
D008	I_{LO}	Output Leakage Current	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}
D009	C_{INT}	Internal Capacitance (all inputs and outputs)	—	7	pF	T_A = +25°C, CLK = 1.0 MHz, V_{CC} = 5.0V (**Note 1**)
D010	I_{CC} Read	Operating Current	—	5	mA	V_{CC} = 5.5V; F_{CLK} = 10.0 MHz; SO = Open
			—	2.5	mA	V_{CC} = 2.5V; F_{CLK} = 5.0 MHz; SO = Open
D011	I_{CC} Write		—	5	mA	V_{CC} = 5.5V
			—	3	mA	V_{CC} = 2.5V
D012	I_{CCS}	Standby Current	—	5	µA	$\overline{CS}$ = V_{CC} = 5.5V, Inputs tied to V_{CC} or V_{SS}, T_A = +125°C
			—	1	µA	$\overline{CS}$ = V_{CC} = 2.5V, Inputs tied to V_{CC} or V_{SS}, T_A = +85°C

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V Extended (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	—	10	MHz	4.5V ≤ VCC < 5.5V
			—	5	MHz	2.5V ≤ VCC < 4.5V
			—	3	MHz	1.8V ≤ VCC < 2.5V
2	TCSS	$\overline{CS}$ Setup Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			150	—	ns	1.8V ≤ VCC < 2.5V
3	TCSH	$\overline{CS}$ Hold Time	100	—	ns	4.5V ≤ VCC < 5.5V
			200	—	ns	2.5V ≤ VCC < 4.5V
			250	—	ns	1.8V ≤ VCC < 2.5V
4	TCSD	$\overline{CS}$ Disable Time	50	—	ns	
5	Tsu	Data Setup Time	10	—	ns	4.5V ≤ VCC < 5.5V
			20	—	ns	2.5V ≤ VCC < 4.5V
			30	—	ns	1.8V ≤ VCC < 2.5V
6	THD	Data Hold Time	20	—	ns	4.5V ≤ VCC < 5.5V
			40	—	ns	2.5V ≤ VCC < 4.5V
			50	—	ns	1.8V ≤ VCC < 2.5V
7	TR	CLK Rise Time	—	100	ns	**Note 1**
8	TF	CLK Fall Time	—	100	ns	**Note 1**
9	THI	Clock High Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			150	—	ns	1.8V ≤ VCC < 2.5V
10	TLO	Clock Low Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			150	—	ns	1.8V ≤ VCC < 2.5V
11	TCLD	Clock Delay Time	50	—	ns	
12	TCLE	Clock Enable Time	50	—	ns	
13	TV	Output Valid from Clock Low	—	50	ns	4.5V ≤ VCC < 5.5V
			—	100	ns	2.5V ≤ VCC < 4.5V
			—	160	ns	1.8V ≤ VCC < 2.5V
14	THO	Output Hold Time	0	—	ns	**Note 1**
15	TDIS	Output Disable Time	—	40	ns	4.5V ≤ VCC < 5.5V (**Note 1**)
			—	80	ns	2.5V ≤ VCC < 4.5V (**Note 1**)
			—	160	ns	1.8V ≤ VCC < 2.5V (**Note 1**)

Note 1: This parameter is periodically sampled and not 100% tested.

2: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V Extended (E): T_A = -40°C to +125°C V_{CC} = 2.5V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
16	T_{HS}	$\overline{HOLD}$ Setup Time	20	—	ns	4.5V ≤ V_{CC} < 5.5V
			40	—	ns	2.5V ≤ V_{CC} < 4.5V
			80	—	ns	1.8V ≤ V_{CC} < 2.5V
17	T_{HH}	$\overline{HOLD}$ Hold Time	20	—	ns	4.5V ≤ V_{CC} < 5.5V
			40	—	ns	2.5V ≤ V_{CC} < 4.5V
			80	—	ns	1.8V ≤ V_{CC} < 2.5V
18	T_{HZ}	$\overline{HOLD}$ Low to Output High-Z	—	30	ns	4.5V ≤ V_{CC} < 5.5V (**Note 1**)
			—	60	ns	2.5V ≤ V_{CC} < 4.5V (**Note 1**)
			—	160	ns	1.8V ≤ V_{CC} < 2.5V (**Note 1**)
19	T_{HV}	$\overline{HOLD}$ High to Output Valid	—	30	ns	4.5V ≤ V_{CC} < 5.5V
			—	60	ns	2.5V ≤ V_{CC} < 4.5V
			—	160	ns	1.8V ≤ V_{CC} < 2.5V
20	T_{WC}	Internal Write Cycle Time (byte or page)	—	5	ms	**Note 2**
21		Endurance	1M	—	E/W Cycles	+25°C, V_{CC} = 5.5V, Page Mode (**Note 3**)

Note 1: This parameter is periodically sampled and not 100% tested.

2: T_{WC} begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform	
V_{LO} = 0.2V	—
V_{HI} = V_{CC} - 0.2V	**Note 1**
V_{HI} = 4.0V	**Note 2**
C_L = 100 pF	—
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For V_{CC} ≤ 4.0V

2: For V_{CC} ≥ 4.0V

FIGURE 1-1: HOLD TIMING

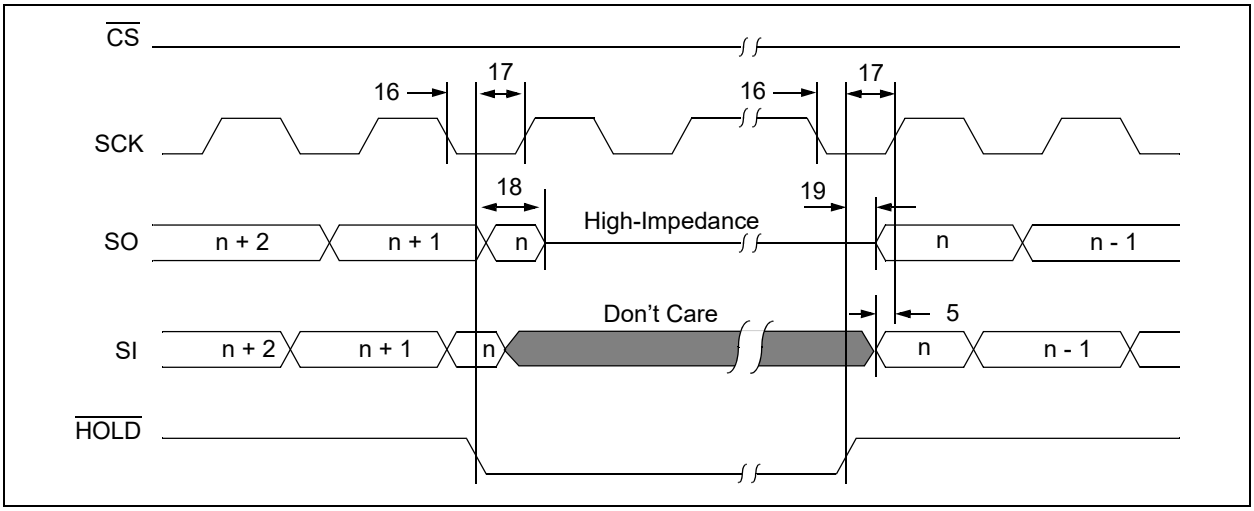


FIGURE 1-2: SERIAL INPUT TIMING

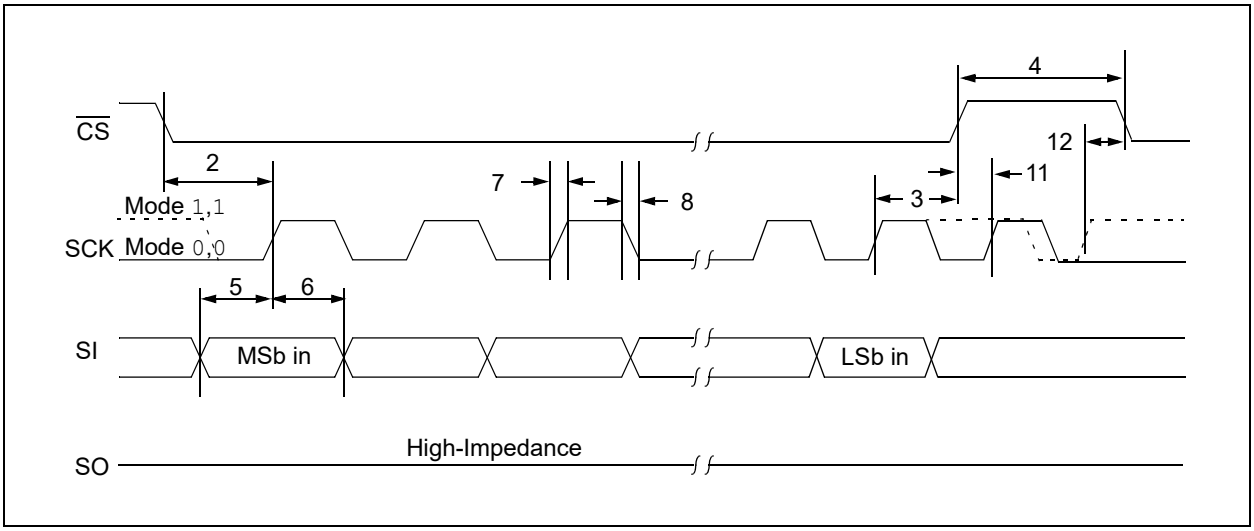
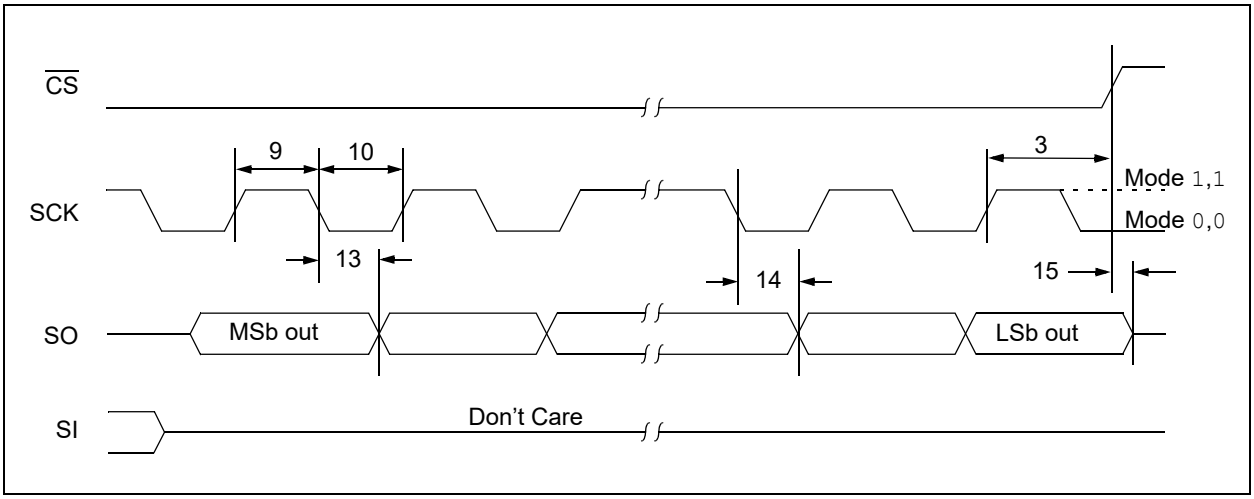


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	DFN[1]	MSOP	PDIP	SOIC	SOT-23	TDFN[1]	TSSOP	Rotated TSSOP	Function
$\overline{CS}$	1	1	1	1	5	1	1	3	Chip Select Input
SO	2	2	2	2	4	2	2	4	Serial Data Output
$\overline{WP}$	3	3	3	3	—	3	3	5	Write-Protect Pin
Vss	4	4	4	4	2	4	4	6	Ground
SI	5	5	5	5	3	5	5	7	Serial Data Input
SCK	6	6	6	6	1	6	6	8	Serial Clock Input
$\overline{HOLD}$	7	7	7	7	—	7	7	1	Hold Input
Vcc	8	8	8	8	6	8	8	2	Supply Voltage

Note 1: The exposed pad on the DFN/TDFN packages can be connected to Vss or left floating.

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus.

A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25XX040A. During a read cycle, data are shifted out on this pin after the falling edge of the serial clock.

2.3 Write-Protect ($\overline{WP}$)

The $\overline{WP}$ pin is a hardware write-protect input pin. When it is low, all writes to the array or STATUS registers are disabled, but any other operations function normally. When $\overline{WP}$ is high, all functions, including nonvolatile writes, operate normally. At any time, when $\overline{WP}$ is low, the write enable latch will be reset and programming will be inhibited. However, if a write cycle is already in progress, $\overline{WP}$ going low will not change or disable the write cycle. See Table 3-4 for the Write-Protect Functionality Matrix.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data are latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a host and the 25XX040A. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin are updated after the falling edge of the clock input.

2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25XX040A while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence.

The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25XX040A must remain selected during this sequence. The SI and SCK levels are “don’t cares” during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not be resumed until the next SCK high-to-low transition.

The SO line will tri-state immediately upon a high-to-low transition of the HOLD pin and will begin outputting again immediately upon a subsequent low-to-high transition of the HOLD pin, independent of the state of SCK.

3.0 FUNCTIONAL DESCRIPTION

3.1 Principles of Operation

The 25XX040A is a 512-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25XX040A contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred Most Significant bit (MSb) first, Least Significant bit (LSb) last.

Data (SI) are sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25XX040A in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

BLOCK DIAGRAM

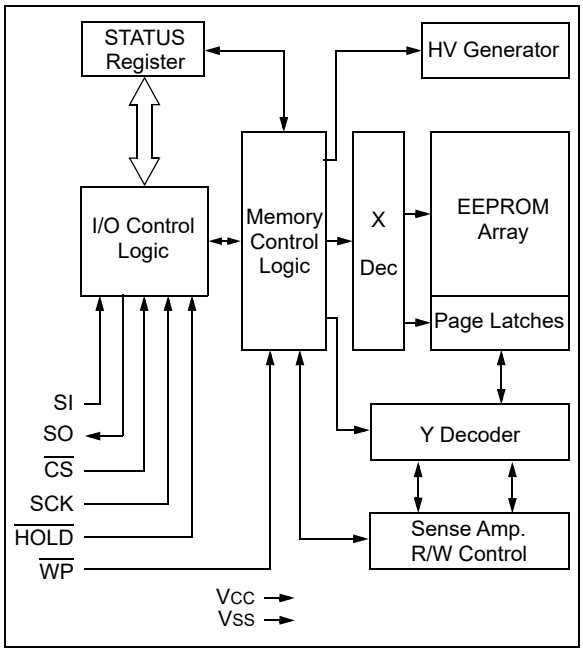


TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 $A_8$011(1)	Read data from memory array beginning at selected address
WRITE	0000 $A_8$010(1)	Write data to memory array beginning at selected address
WRDI	0000 x100(2)	Reset the write enable latch (disable write operations)
WREN	0000 x110(2)	Set the write enable latch (enable write operations)
RDSR	0000 x101(2)	Read STATUS register
WRSR	0000 x001(2)	Write STATUS register

Note 1: A_8 is the 9th address bit, which is used to address the entire 512-byte array.

2: x = don't care

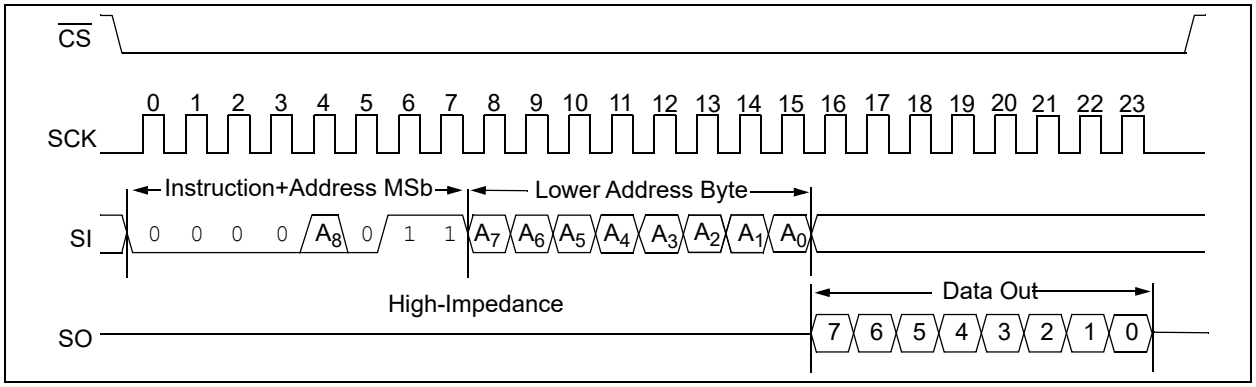
3.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit `READ` instruction is transmitted to the 25XX040A followed by a 9-bit address. The MSb (A_8) is sent to the client during the instruction sequence. See Figure 3-1 for more details.

After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address are shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the client.

The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFh), the address counter rolls over to address 000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-1).

FIGURE 3-1: READ SEQUENCE



3.3 Write Sequence

Prior to any attempt to write data to the 25XX040A, the write enable latch must be set by issuing the WREN instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25XX040A. After all eight bits of the instruction are transmitted, $\overline{CS}$ must be driven high to set the write enable latch.

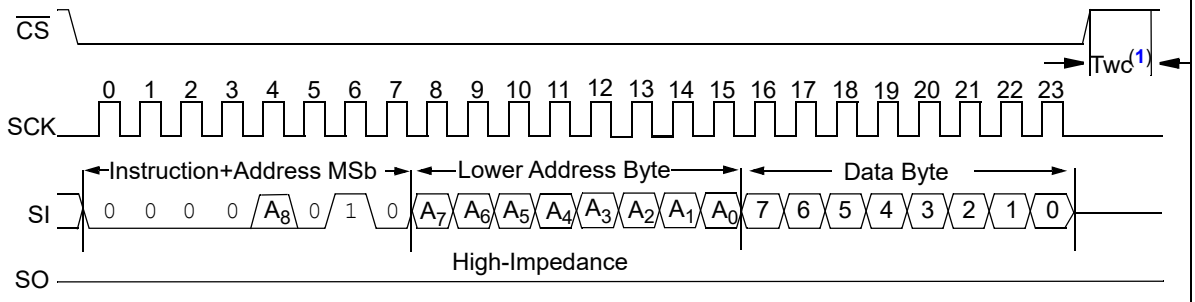
If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ driven high, data will not be written to the array since the write enable latch was not properly set.

After setting the write enable latch, the user may proceed by driving $\overline{CS}$ low, issuing a WRITE instruction, followed by the remainder of the address and then the data to be written. Keep in mind that the Most Significant address bit (A_8) is included in the instruction byte for the 25XX040A. Up to 16 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally, a page address begins with XXXX 0000 and ends with XXXX 1111. If the internal address counter reaches XXXX 1111 and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and overwrite any data that previously existed in those locations.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

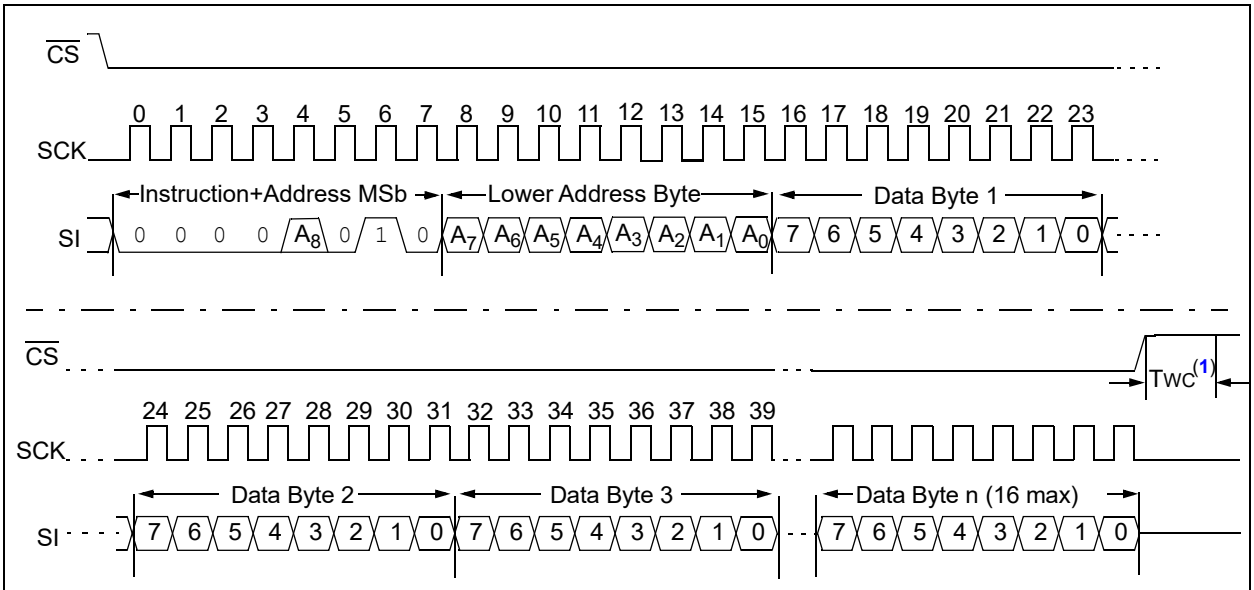
For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is driven high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 3-6). Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the write cycle is completed, the write enable latch is reset.

FIGURE 3-2: BYTE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

FIGURE 3-3: PAGE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX040A contains a write enable latch. See Table 3-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- $\overline{WP}$ pin is brought low

FIGURE 3-4: WRITE ENABLE SEQUENCE (WREN)

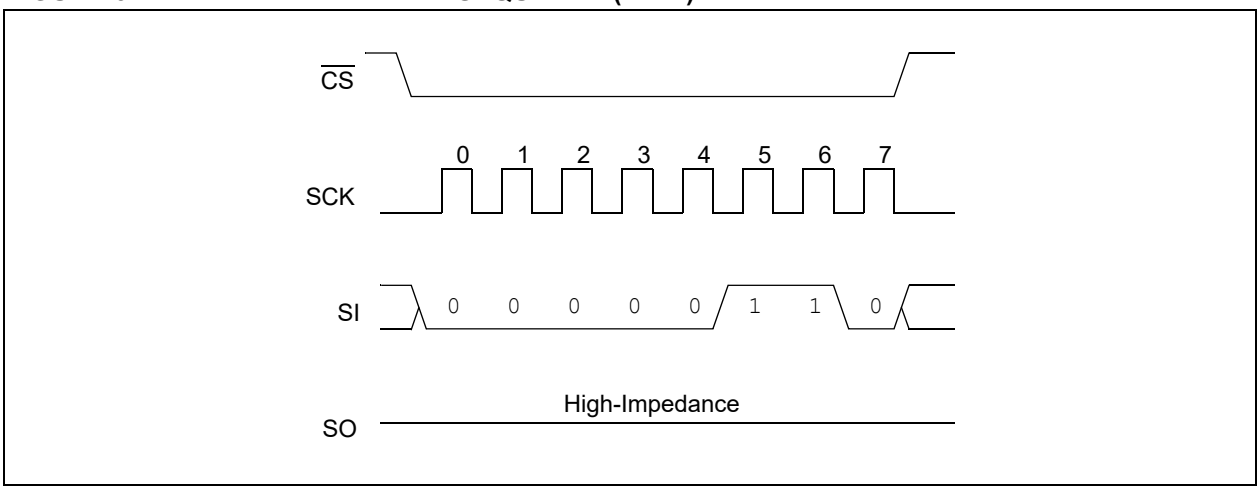
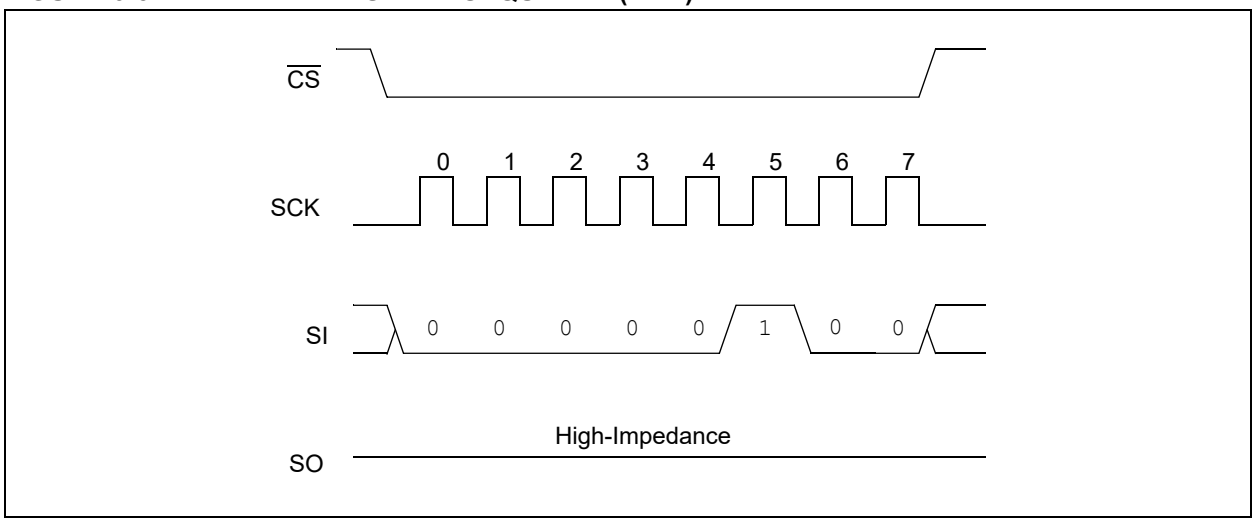


FIGURE 3-5: WRITE DISABLE SEQUENCE (WRDI)



3.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. See Figure 3-6 for the RDSR timing sequence. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 3-2: STATUS REGISTER

7	6	5	4	3	2	1	0
–	–	–	–	W/R	W/R	R	R
X	X	X	X	BP1	BP0	WEL	WIP

Note 1: W/R = writable/readable. R = read-only.

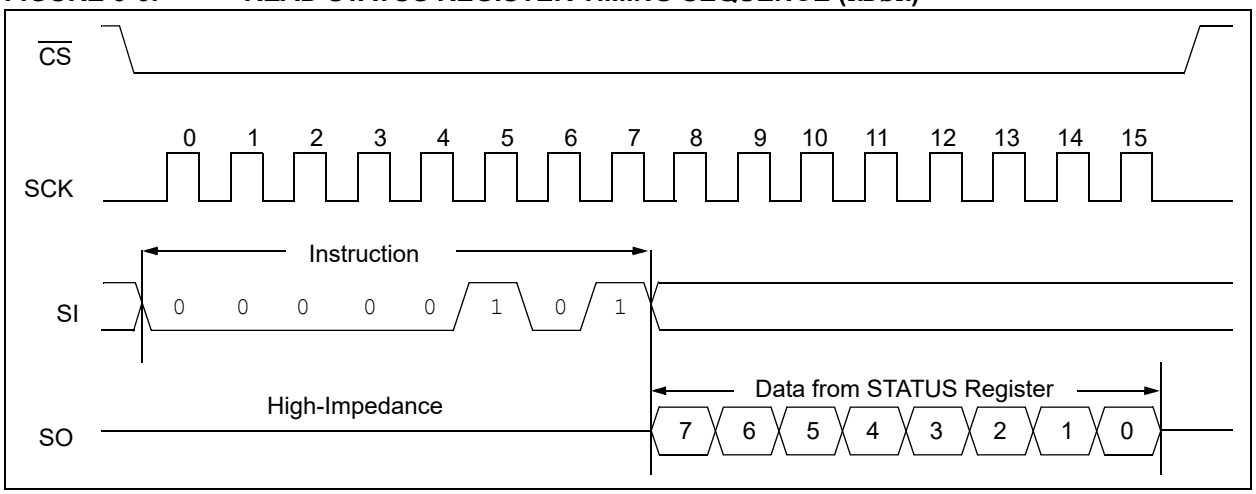
The **Write-In-Process (WIP)** bit indicates whether the 25XX040A is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 3-4 and Figure 3-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction (see Figure 3-7). These bits are nonvolatile and are described in more detail in Table 3-3.

See Figure 3-6 for the RDSR timing sequence.

FIGURE 3-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



3.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 3-2. Four levels of protection for the array are selectable by writing to the appropriate bits in the STATUS register. The user has the ability to write-protect none, one, two or all four of the segments of the array as shown in Table 3-3. See Figure 3-7 for the WRSR timing sequence.

TABLE 3-3: ARRAY PROTECTION

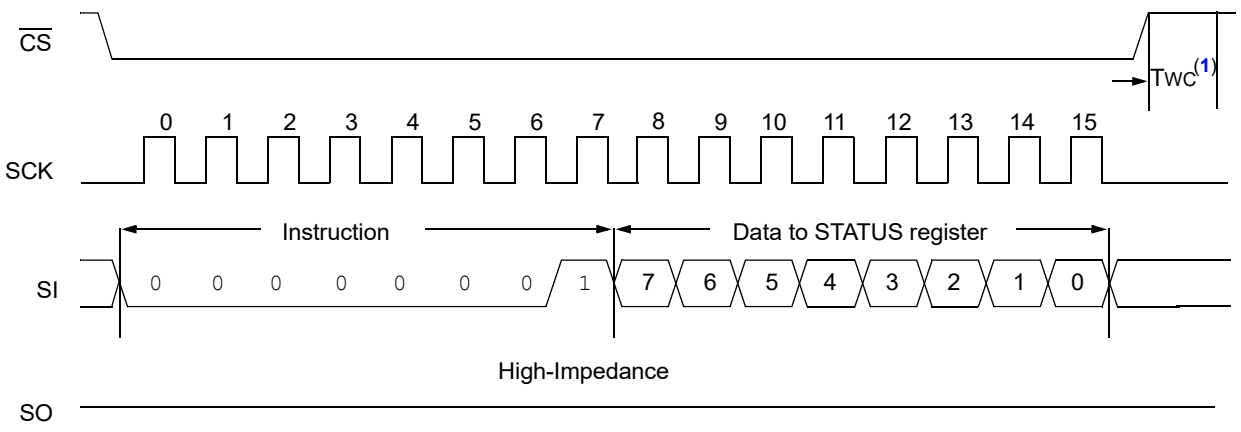
BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (180h-1FFh)
1	0	upper 1/2 (100h-1FFh)
1	1	all (000h-1FFh)

TABLE 3-4: WRITE-PROTECT FUNCTIONALITY MATRIX

$\overline{WP}$ (pin 3)	WEL (SR bit 1)	Protected Blocks	Unprotected Blocks	STATUS Register
0 (low)	x	Protected	Protected	Protected
1 (high)	0	Protected	Protected	Protected
1 (high)	1	Protected	Writable	Writable

Note 1: x = don't care

FIGURE 3-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

4.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

5.0 POWER-ON STATE

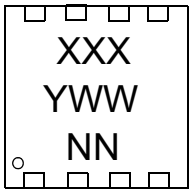
The 25XX040A powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{CS}$ is required to enter active state

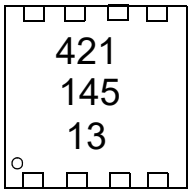
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

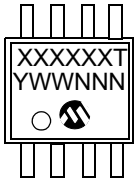
8-Lead 2X3 DFN



Example

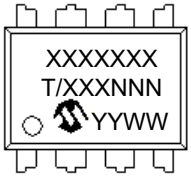


8-Lead MSOP (150 mil)

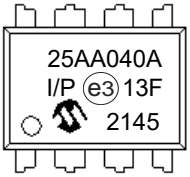


Example

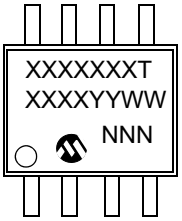
8-Lead PDIP (300 mil)



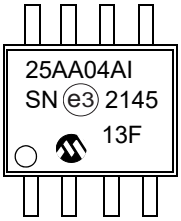
Example



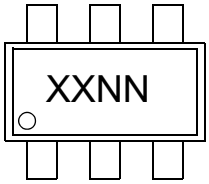
8-Lead SOIC



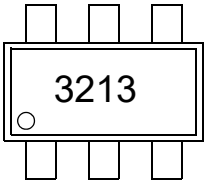
Example



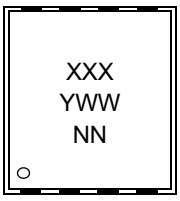
6-Lead SOT-23



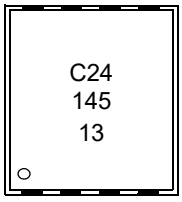
Example



8-Lead 2x3 TDFN

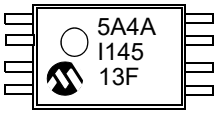


Example



8-Lead TSSOP

Example



Part Number	1st Line Marking Codes								
	DFN		MSOP	SOT-23		TDFN		TSSOP	
	I-Temp.	E-Temp.		I-Temp.	E-Temp.	I-Temp.	E-Temp.	Standard	Rotated
25AA040A	421	—	5A4AT	32NN	—	C21	—	5A4A	A4AX
25LC040A	424	425	5L4AT	35NN	36NN	C24	C25	5L4A	L4AX

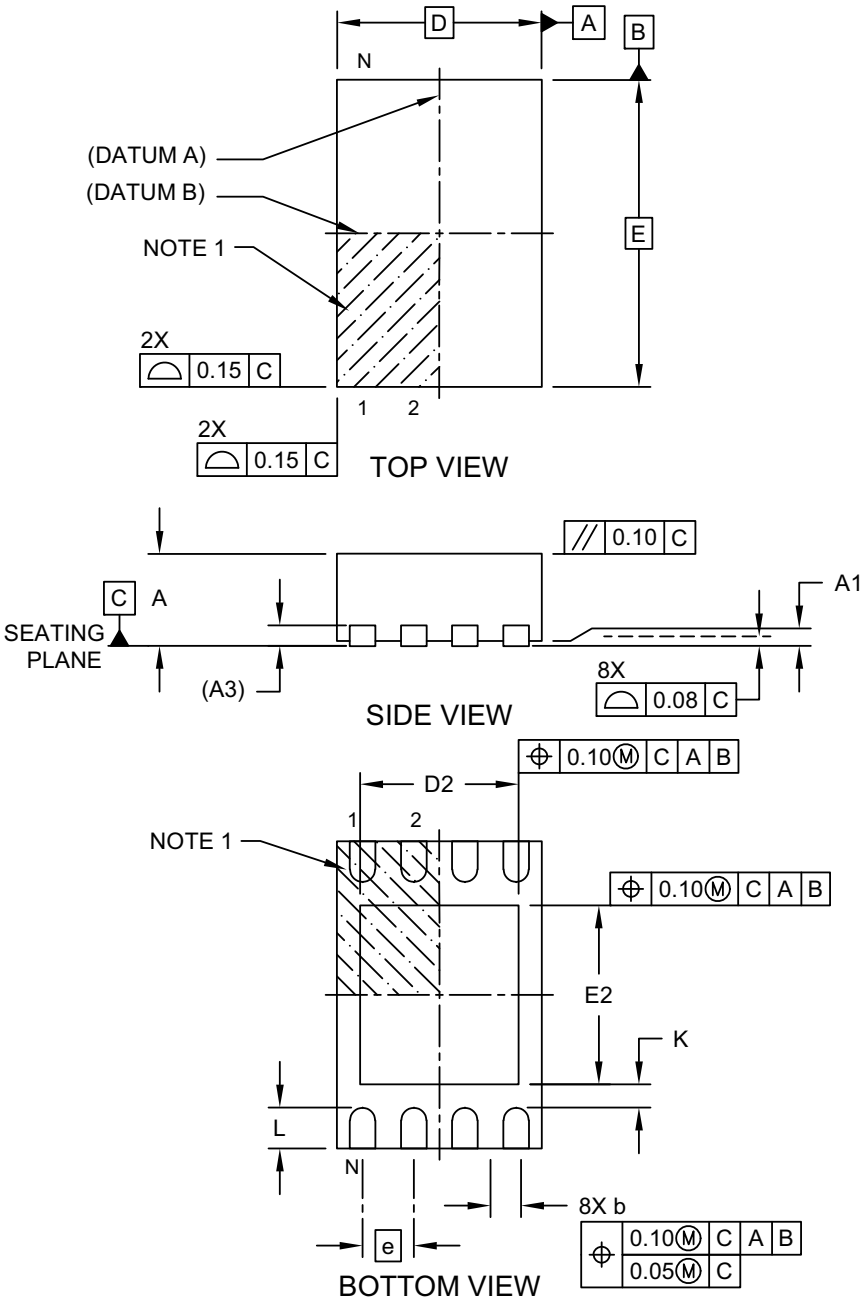
Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	RoHS-compliant JEDEC® designator for Matte Tin (Sn)

Note: For very small packages with no room for the RoHS-compliant JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

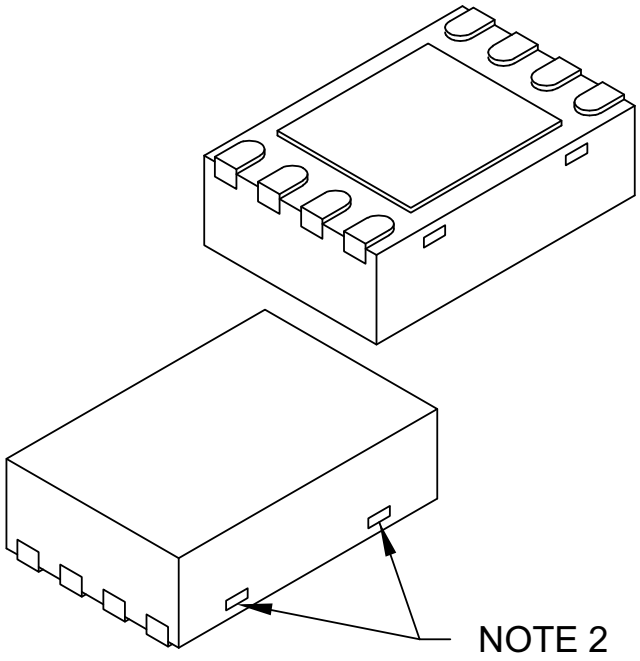
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-123 Rev E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.30	-	1.55
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	-	1.75
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

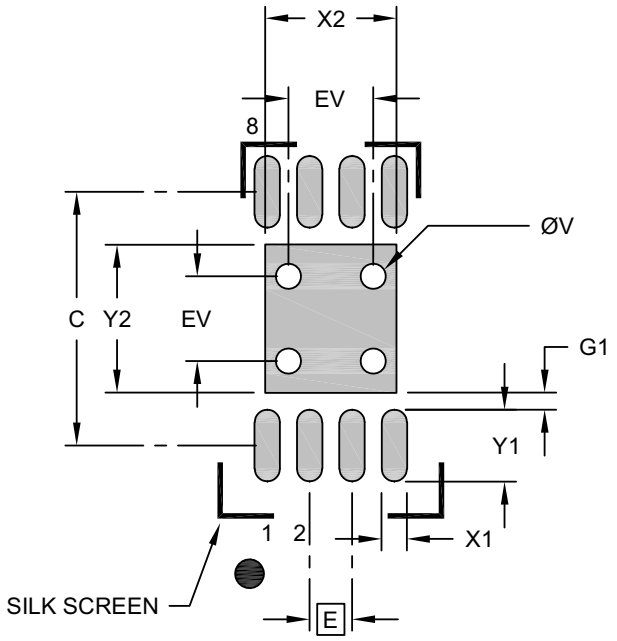
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123 Rev E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.55
Optional Center Pad Length	Y2			1.75
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

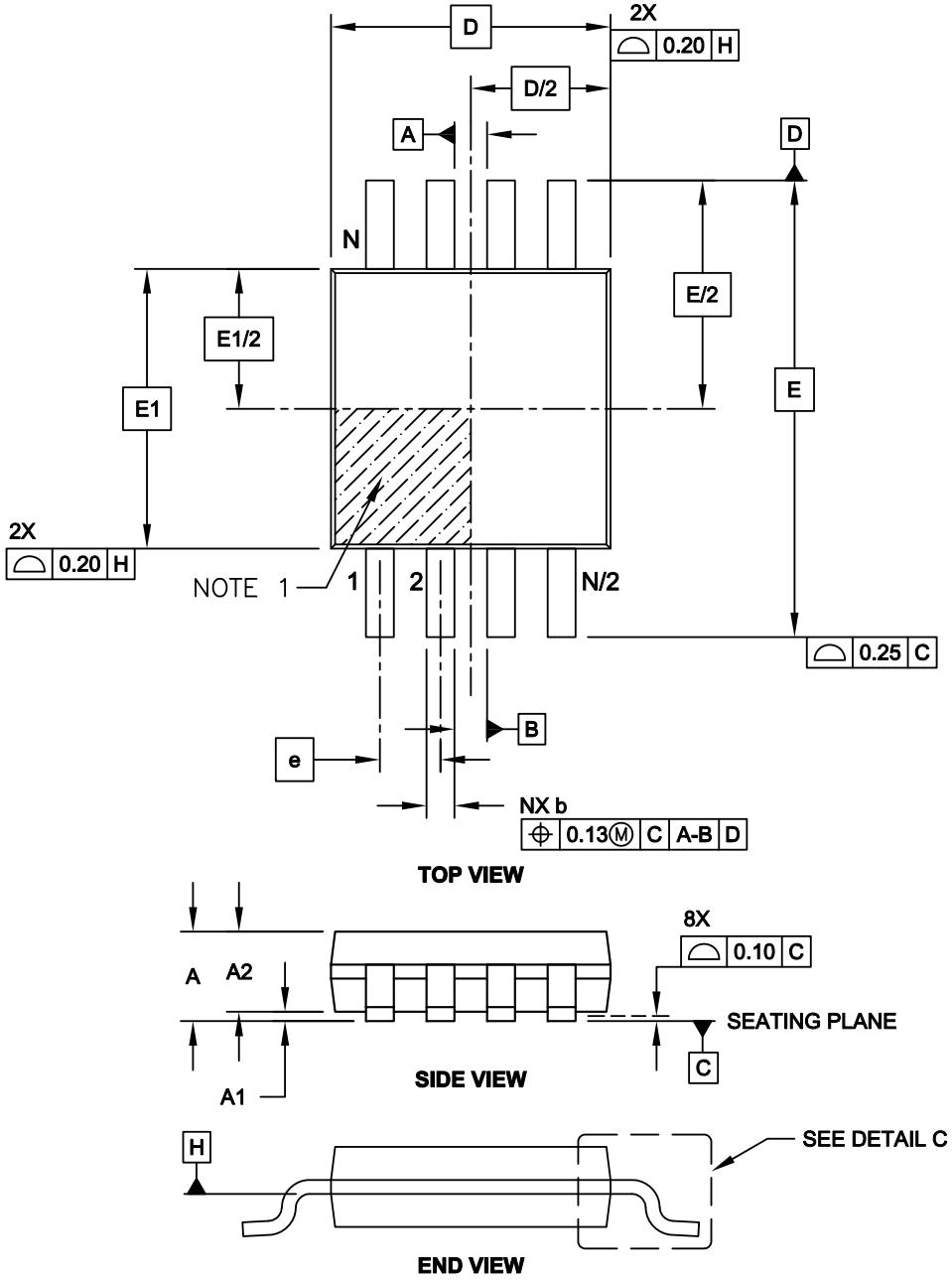
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2123 Rev E

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

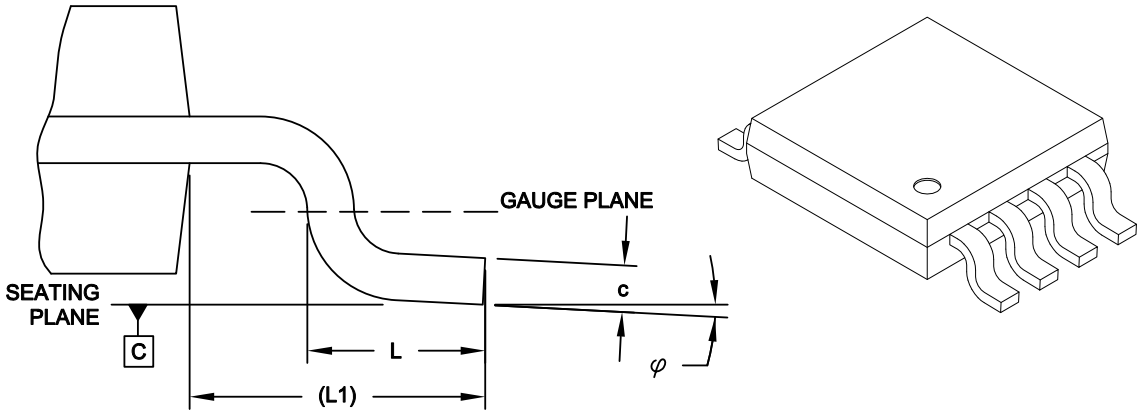
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

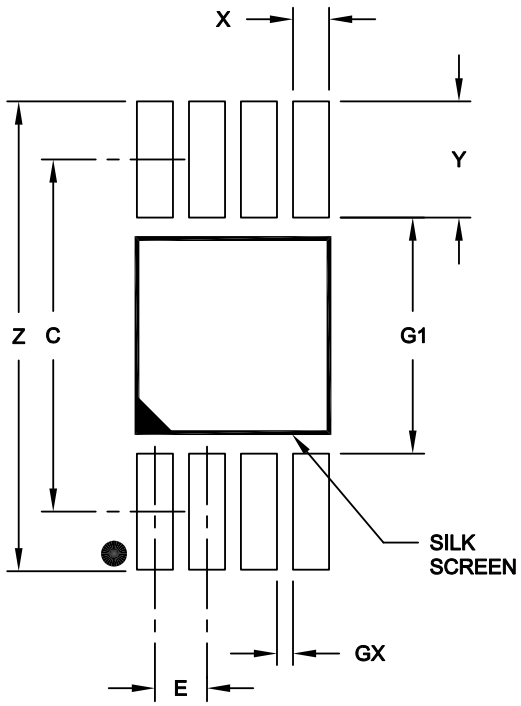
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

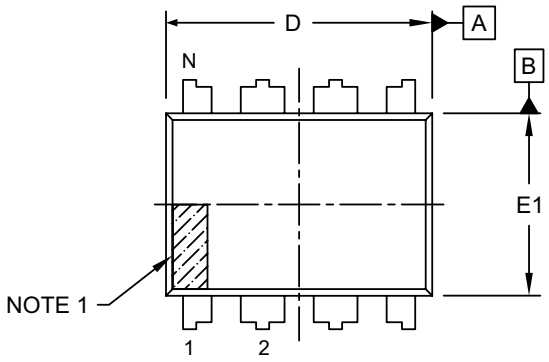
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

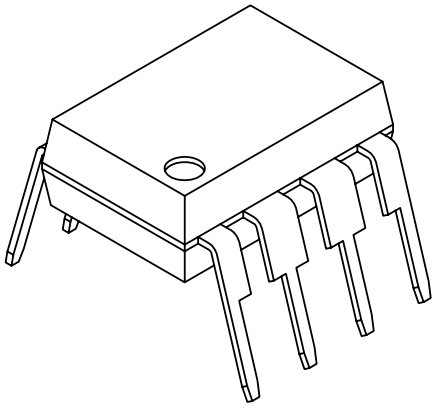
Microchip Technology Drawing No. C04-2111A

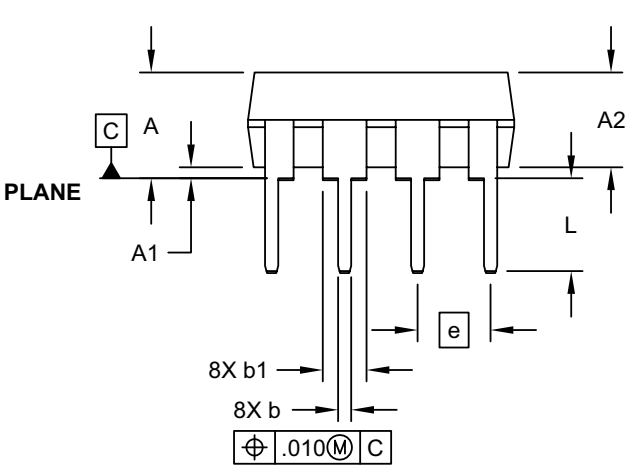
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

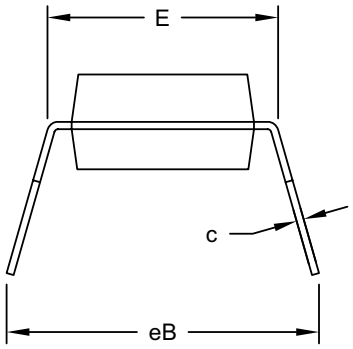


TOP VIEW





SIDE VIEW

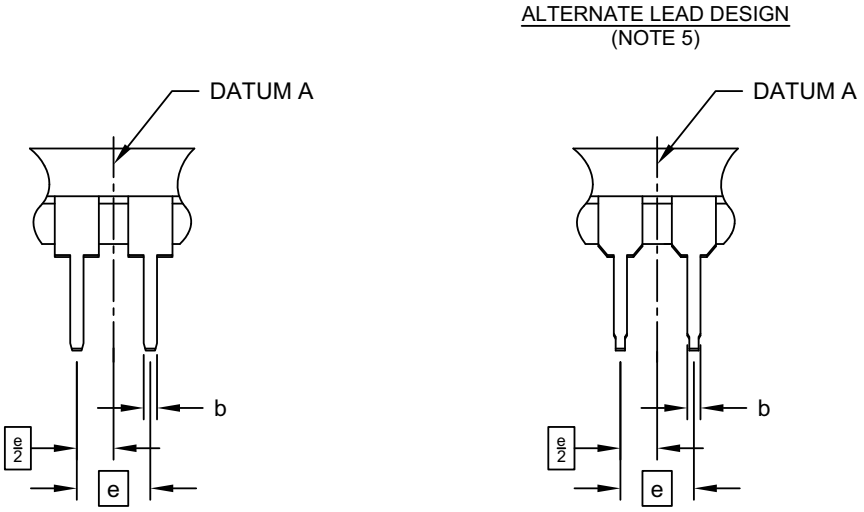


END VIEW

Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

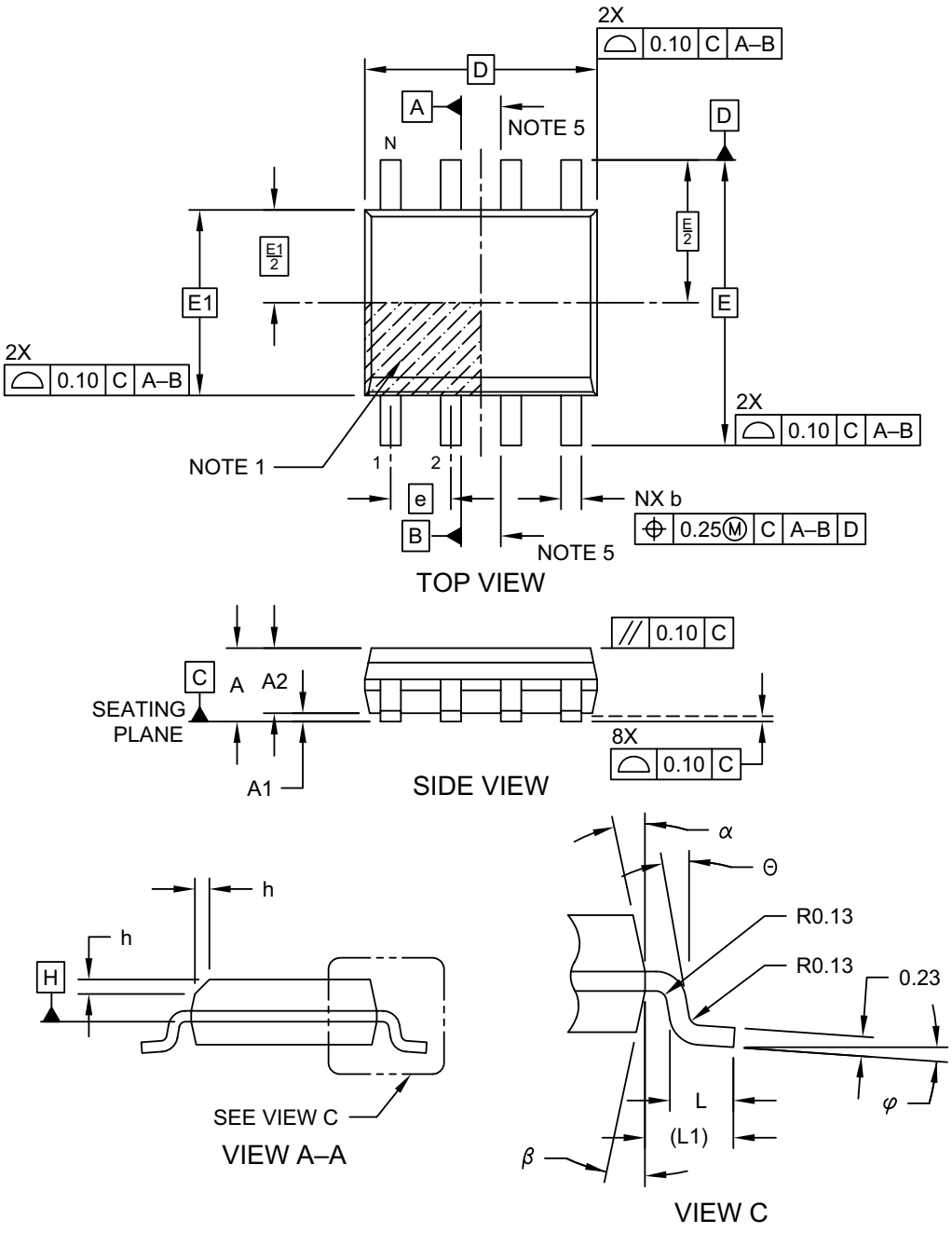
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

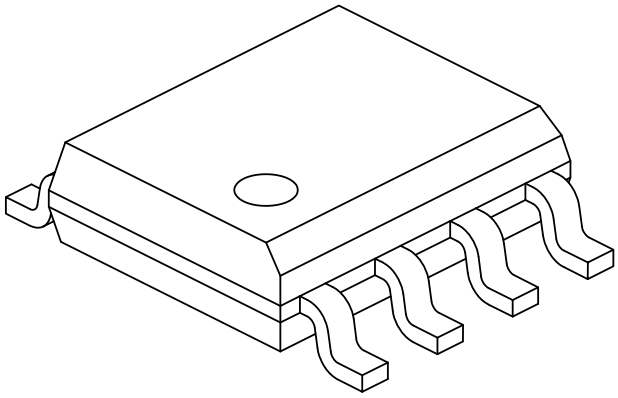
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

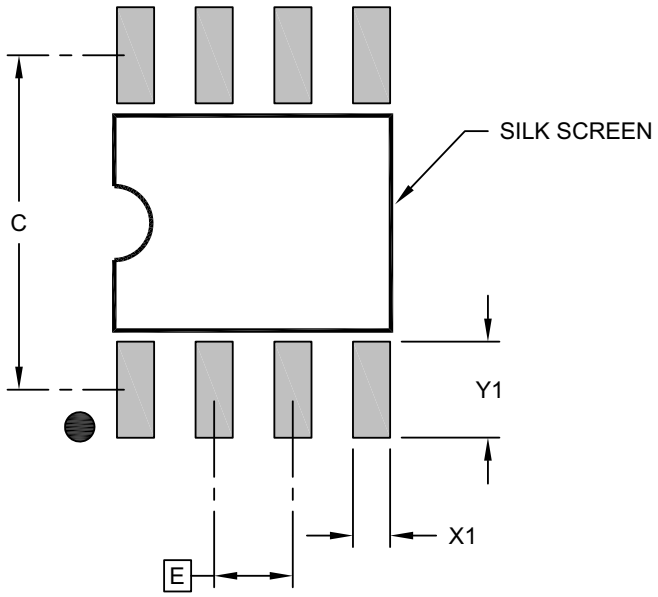
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

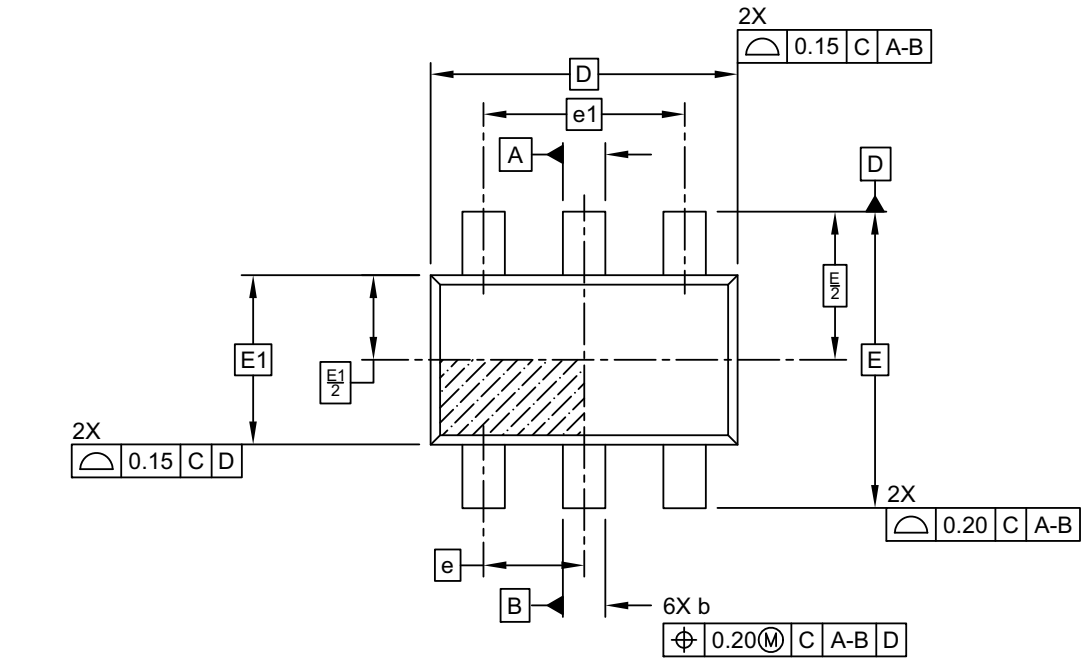
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

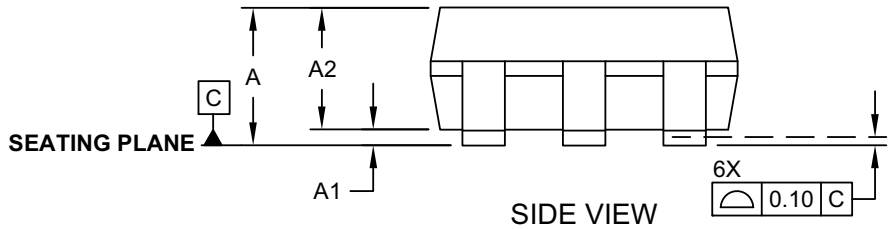
Microchip Technology Drawing C04-2057-SN Rev F

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

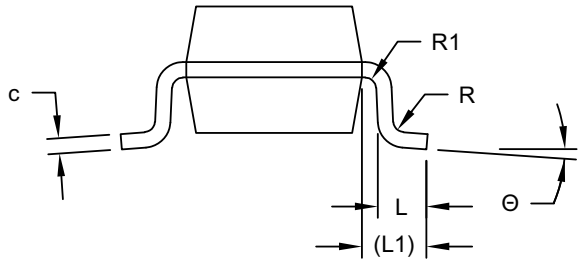
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

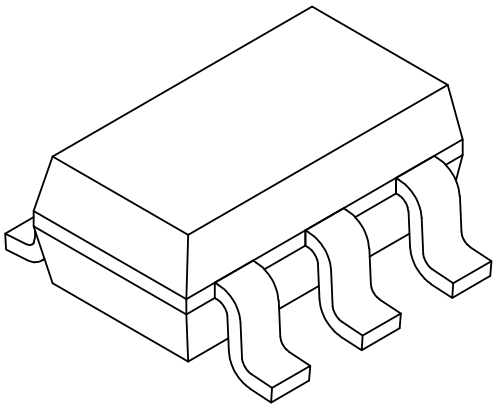


END VIEW

Microchip Technology Drawing C04-028D (OT) Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

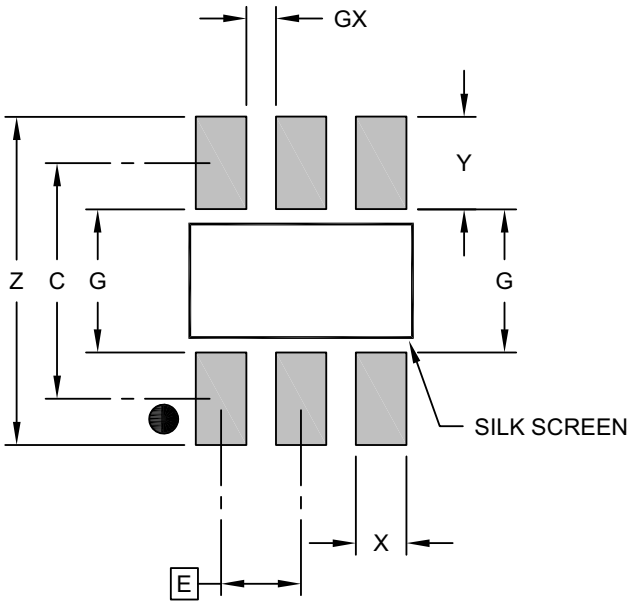
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028D (OT) Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

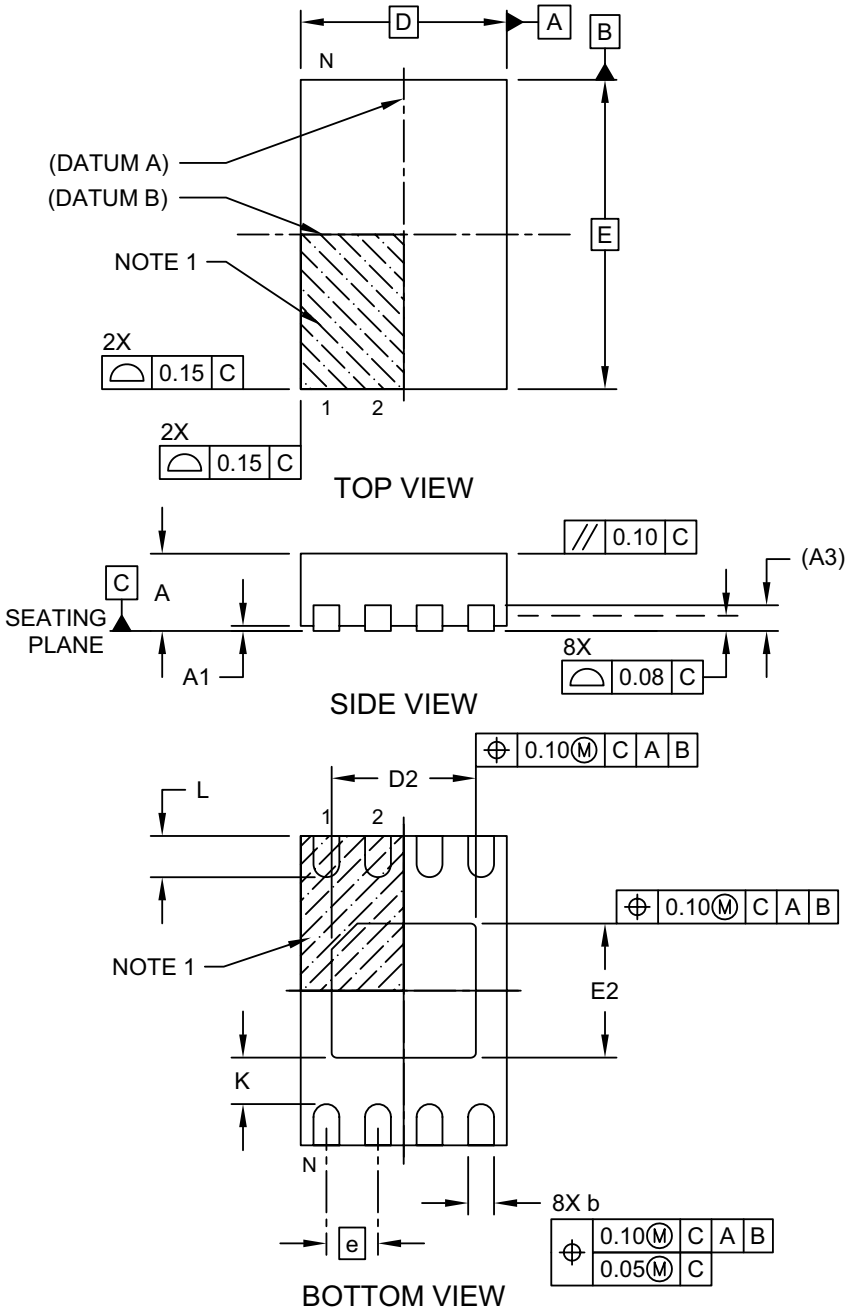
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028D (OT)

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]
With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

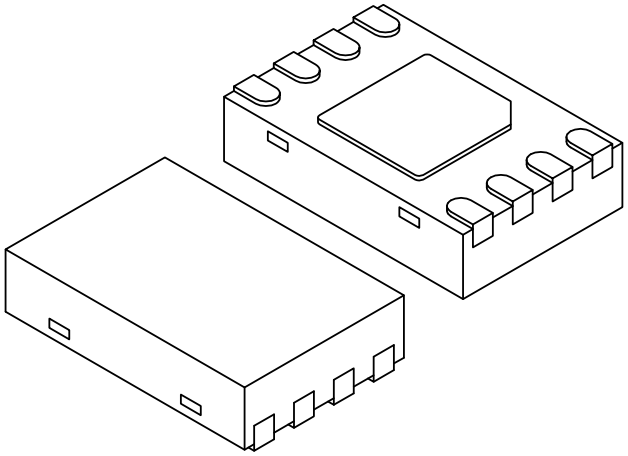
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Exposed Pad Width	E2	1.25	1.30	1.35
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

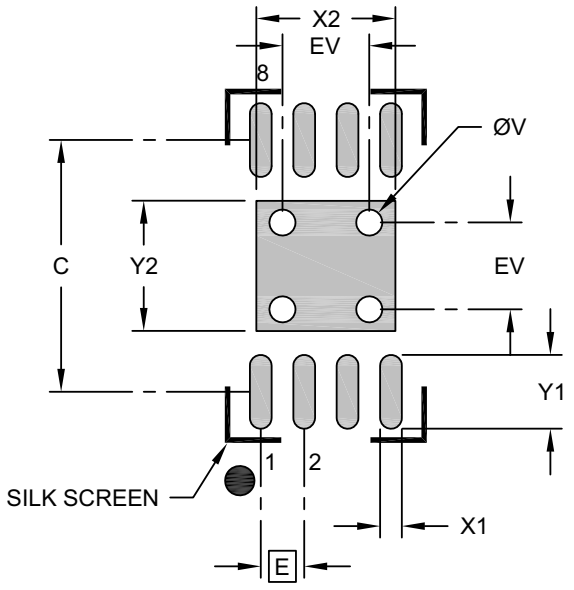
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]
With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.50
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.25
Contact Pad Length (X8)	Y1			0.85
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

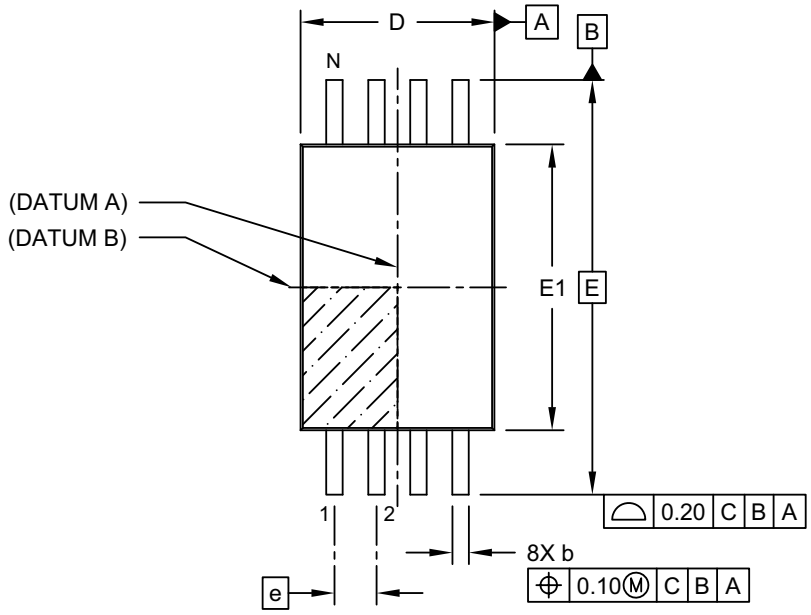
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

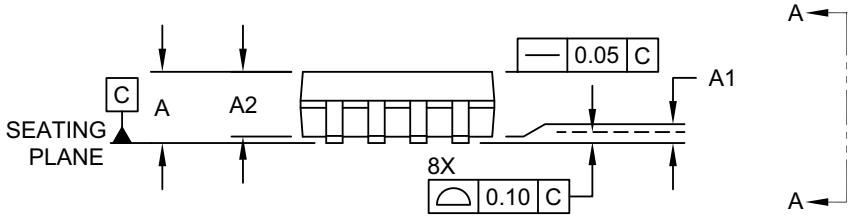
Microchip Technology Drawing No. C04-129-MN Rev. B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

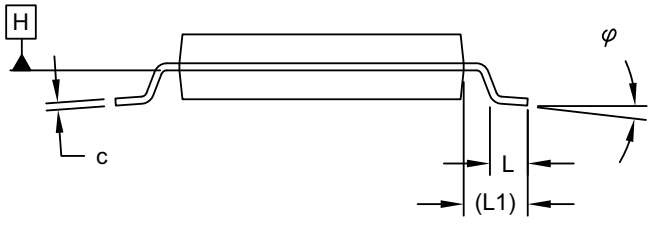
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

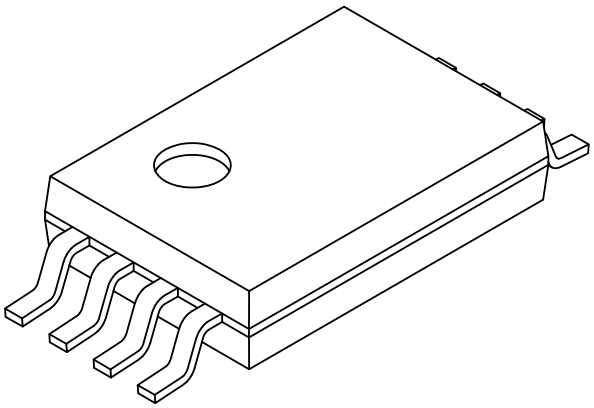


VIEW A-A

Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	-
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

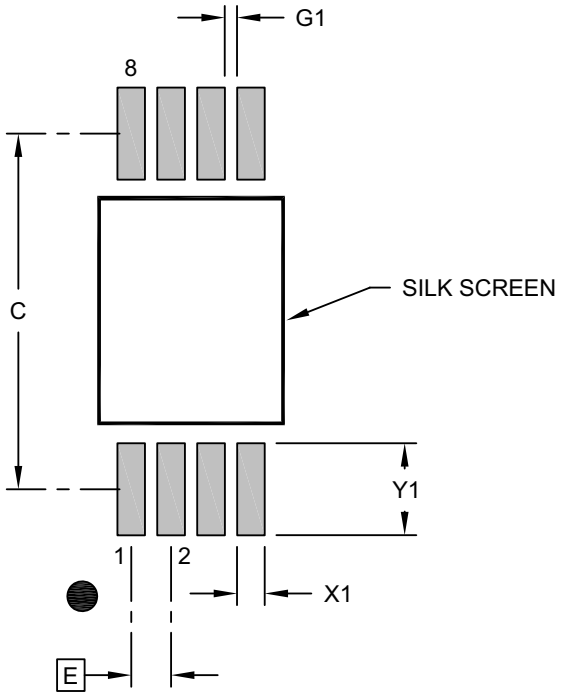
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

APPENDIX A: REVISION HISTORY

Revision J (12/2021)

Added Product Identification System section for Automotive; Updated DFN, PDIP, SOIC, SOT23, TDFN and TSSOP package drawings; Replaced terminology “Master” and “Slave” with “Host” and “Client”, respectively; Replaced “Automotive (E):” designation with “Extended (E):” designation; Reformatted some sections for better readability.

Revision H (12/2012)

Revised Table 1-2, Param. 21.

Revision G (11/2011)

Added TDFN Package.

Revision F (7/2009)

Replaced 6-Lead SOT-23 package drawing (from CH to OT); Revised 8-Lead DFN (MC); Added 8-Lead DFN (MC) Land Pattern.

Revision E (10/2007)

Revised Features (Pb-free); Replaced Package Drawings.

Revision D (5/2007)

Removed Preliminary status; Replaced package drawings (Rev. AP); Revise Table 1-1, Param. D004, D007, D008; Revise Table 1-2, Param. 7, 8, 9 ,10.

Revision C (2/2006)

Added Packages SOT-23, DFN and X-rotated TSSOP; Revised AC Char., Params. 9, 10; Revised Package Legend.

Revision B (12/2003)

Corrections to Section 1.0, Electrical Characteristics

Revision A (9/2003)

Initial Release.

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PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X [1]	–X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	25AA040A	=	4-Kbit, 1.8V, 16-Byte Page SPI Serial EEPROM
	25AA040AX	=	4-Kbit, 1.8V, 16-Byte Page SPI Serial EEPROM, in alternate pinout (ST only)
	25LC040A	=	4-Kbit, 2.5V, 16-Byte Page SPI Serial EEPROM
	25LC040AX	=	4-Kbit, 2.5V, 16-Byte Page SPI Serial EEPROM, in alternate pinout (ST only)
Tape and Reel Option:	Blank	=	Standard packaging (tube)
	T	=	Tape and Reel[1]
Temperature Range:	I	=	-40°C to +85°C (Industrial)
	E	=	-40°C to +125°C (Extended)
Package:	MC	=	Plastic Dual Flat, No Lead – 2x3x1 mm Body 8-Lead (DFN)
	MS	=	Plastic Micro Small Outline – 8-Lead (MSOP)
	P	=	Plastic Dual In-Line – 300 mil Body, 8-Lead (PDIP)
	OT	=	Plastic Small Outline Transistor – 6-Lead (SOT-23)
	SN	=	Plastic Small Outline - Narrow, 3.90 mm (.150 In) Body, 8-Lead (SOIC)
	MNY[2]	=	Plastic Dual Flat, No Lead Package – 2x3x0.8 mm Body, 8-Lead (TDFN)
	ST	=	Plastic Thin Shrink Small Outline – 4x4 mm Body, 8-Lead (TSSOP)

Examples

a) 25AA040A-I/MS: 4-Kbit, 1.8V Serial EEPROM, Industrial temp., MSOP package.

b) 25AA040AT-I/SN: 4-Kbit, 1.8V Serial EEPROM, Tape and Reel, Industrial temp., SOIC package.

c) 25LC040AT-I/SN: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Industrial temp., SOIC package.

d) 25LC040AT-I/ST: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Industrial temp., TSSOP package.

e) 25LC040AT-E/SN: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Extended temp., SOIC package.

f) 25LC040AX-E/ST: 4-Kbit, 2.5V Serial EEPROM, Rotated pinout, Extended temp., TSSOP package.

g) 25LC040AT-I/MNY: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Industrial temp., TDFN package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: “Y” indicates a Nickel Palladium Gold (NiPdAu) finish.

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X [1]	–X	/XX	XXX [2,3]
Device	Tape and Reel Option	Temperature Range	Package	Variant

Device:	25AA040A	=	4-Kbit, 1.8V, 16-Byte Page SPI Serial EEPROM
	25LC040A	=	4-Kbit, 2.5V, 16-Byte Page SPI Serial EEPROM
Tape and Reel Option:	Blank	=	Standard packaging (tube)
	T	=	Tape and Reel
Temperature Range:	I	=	-40°C to+85°C (AEC-Q100 Grade 3)
	E	=	-40°C to+125°C (AEC-Q100 Grade 1)
Package:	MS	=	Plastic Micro Small Outline – 8-Lead (MSOP)
	OT	=	Plastic Small Outline Transistor – 6-Lead (SOT-23)
	SN	=	Plastic Small Outline - Narrow, 3.90 mm (.150 In) Body, 8-Lead (SOIC)
	ST	=	Plastic Thin Shrink Small Outline – 4x4 mm Body, 8-Lead (TSSOP)
Variant: [2,3]	16KVAO	=	Standard Automotive, 16K Process
	16KVXX	=	Customer-Specific Automotive, 16K Process

Examples

a) 25LC040AT-I/SN16KVAO: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 3, SOIC package.

b) 25LC040A-E/SN16KVAO: 4-Kbit, 1.8V Serial EEPROM, Automotive Grade 1, SOIC package.

c) 25LC040A-E/ST16KVAO: 4-Kbit, 2.5V, Serial EEPROM, Automotive Grade 1, TSSOP package.

d) 25LC040AT-E/SN16KVAO: 4-Kbit, 2.5V, Serial EEPROM, Tape and Reel, Automotive Grade 1, SOIC package.

e) 25LC040AT-E/ST16KVAO: 4-Kbit, 2.5V, Serial EEPROM, Tape and Reel, Automotive Grade 1, TSSOP package.

f) 25LC040AT-E/MS16KVAO: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 1, MSOP package.

g) 25LC040AT-E/OT16KVAO: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 1, SOT-23 package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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Tel: 48-22-3325737

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Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
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UK - Wokingham
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Fax: 44-118-921-5820