AT9919

Hysteretic Buck High-Brightness LED Driver with High-Side Current Sensing

Features

- AEC-Q100 Qualified
- Hysteretic Control with High-side Current Sensing
- Wide Input Voltage Range: 4.5V to 40V
- >90% Efficiency
- Typical ±5% LED Current Accuracy
- Up to 2 MHz Switching Frequency
- Adjustable Constant LED Current
- Analog or Pulse-Width Modulation (PWM) Control Signal for PWM Dimming
- Overtemperature Protection
- –40°C to +125°C Operating Temperature Range

Applications

- LED Lighting Applications
- Automotive Applications

General Description

AT9919 is a PWM controller IC designed to drive high-brightness LEDs using a buck topology. It operates from an input voltage of 4.5 VDC to 40 VDC and employs hysteretic control with a high-side current sense resistor to set the constant output current.

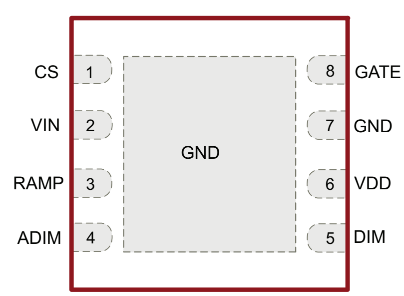
The operating frequency range can be set by selecting the proper inductor. Operation at high switching frequency is possible since the hysteretic control maintains accuracy even at high frequencies. This permits the use of small inductors and capacitors, minimizing space and cost in the overall system.

LED brightness control is achieved with PWM dimming from an analog or PWM input signal. Unique PWM circuitry allows true constant color with a high dimming range. The dimming frequency is programmed using a single external capacitor.

AT9919 comes in a small, 8-Lead WDFN package and is qualified for LED lighting applications.
AT9919 passes the automotive AEC-Q100 reliability testing.

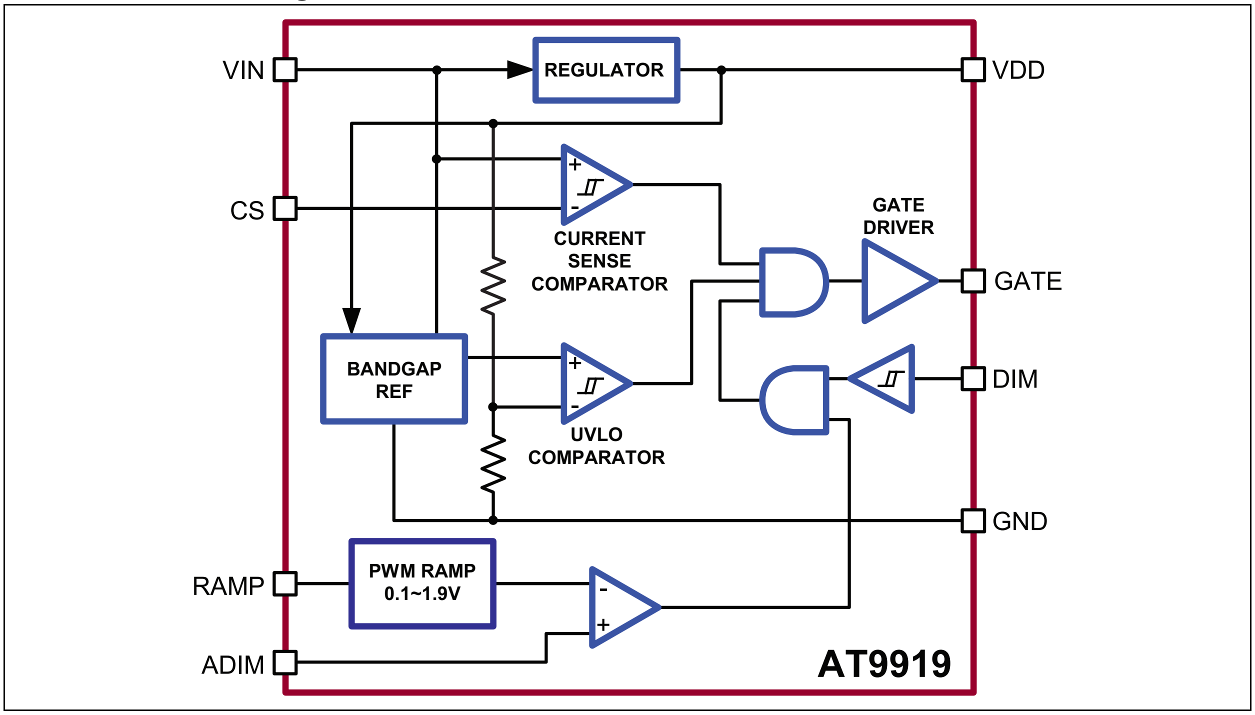
Package Type

8-Lead WDFN
(Top View)

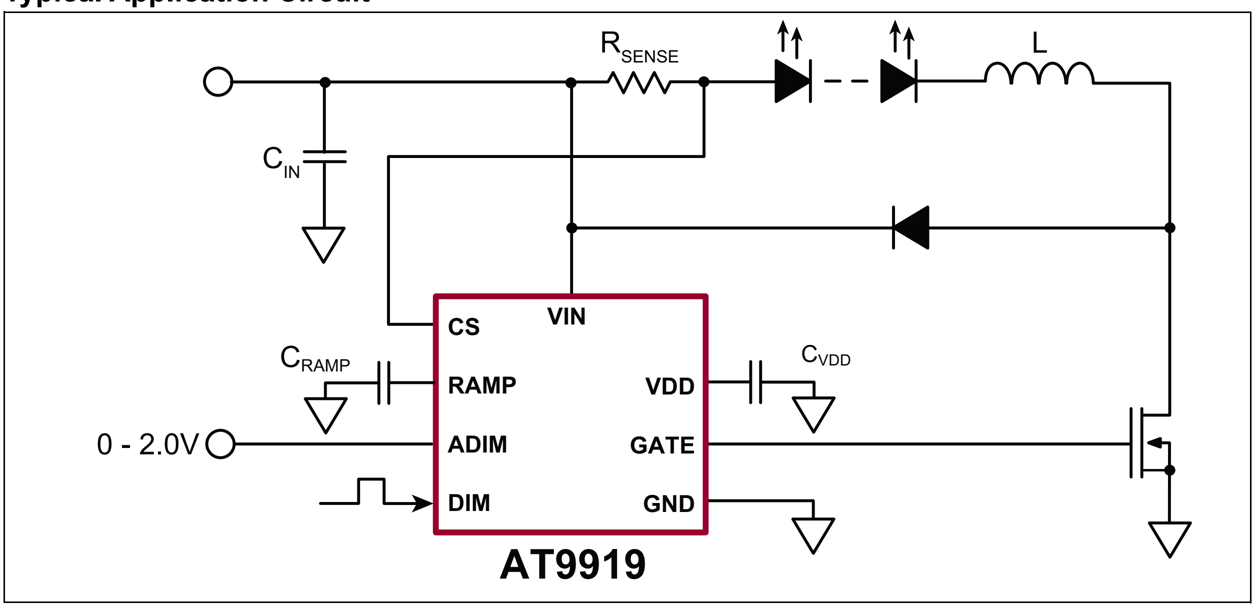


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN} and CS to GND .... -0.3V to +45V
V_{DD}, GATE, RAMP, DIM, ADIM to GND .... -0.3V to +6V
CS to V_{IN} .... -1V to +0.3V
Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... 150°C
Storage Temperature Range .... -65°C to 150°C
Continuous Power Dissipation (T_A = +25°C) 1.6W

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{IN} = 12V, V_{DIM} = V_{DD}, V_{RAMP} = GND, C_{VDD} = 1 µF, R_{SENSE} = 0.5Ω, T_A = T_J = -40ºC to +125ºC (**Note 1**) unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input DC Supply Voltage Range	V_{IN}	4.5	—	40	V	DC input voltage
Internally Regulated Voltage	V_{DD}	4.5	—	5.5	V	V_{IN} = 6V to 40V
Supply Current	I_{IN}	—	—	1.5	mA	GATE open
Shutdown Supply Current	$I_{IN, SDN}$	—	—	900	µA	DIM < 0.7V
Current Limit	$I_{IN, LIM}$	—	30	—	mA	V_{IN} = 4.5V, V_{DD} = 0V
		—	8	—		V_{IN} = 4.5V, V_{DD} = 4V
Oscillator Frequency	f_{OSC}	—	—	2	MHz	
V_{DD} Undervoltage Lockout Threshold	UVLO	—	—	4.5	V	V_{DD} rising
V_{DD} Undervoltage Lockout Hysteresis	$UVLO_{HYST}$	—	500	—	mV	V_{DD} falling
SENSE COMPARATOR						
Sense Voltage Threshold High	$V_{CS(HI)}$	198	230	257	mV	($V_{IN} – V_{CS}$) rising
Sense Voltage Threshold Low	$V_{CS(LO)}$	147	170	195	mV	($V_{IN} – V_{CS}$) falling
Average Reference Voltage	$V_{CS(AVG)}$	186	200	214	mV	$V_{CS(AVG)} = 0.5V_{CS(HI)} + 0.5V_{CS(LO)}$
Propagation Delay to Output High	t_{DPDH}	—	70	—	ns	Falling edge of $V_{IN} – V_{CS} = V_{RS(LO)}$ – 70 mV
Propagation Delay to Output Low	t_{DPDL}	—	70	—	ns	Rising edge of $V_{IN} – V_{CS} = V_{RS(HI)}$ + 70 mV
Current Sense Input Current	I_{CS}	—	—	1	µA	$V_{IN} – V_{CS}$ = 200 mV
Current Sense Threshold Hysteresis	$V_{CS(HYST)}$	—	56	80	mV	
DIM INPUT						
Pin DIM Input High Voltage	V_{IH}	2.2	—	—	V	
Pin DIM Input Low Voltage	V_{IL}	—	—	0.7	V	
Turn-on Time	t_{ON}	—	100	—	ns	DIM rising edge to V_{GATE} = 0.5 x V_{DD}, C_{GATE} = 2 nF
Turn-off Time	t_{OFF}	—	100	—	ns	DIM falling edge to V_{GATE} = 0.5 x V_{DD}, C_{GATE} = 2 nF

Note 1: Limits obtained by design and characterization.
2: For design guidance only

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: V_{IN} = 12V, V_{DIM} = V_{DD}, V_{RAMP} = GND, C_{VDD} = 1 µF, R_{SENSE} = 0.5Ω, T_A = T_J = -40ºC to +125ºC (**Note 1**) unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
GATE DRIVER						
GATE Current, Source	I_{GATE}	0.3	0.5	—	A	V_{GATE} = GND (**Note 2**)
GATE Current, Sink		0.7	1	—	A	V_{GATE} = V_{DD} (**Note 2**)
GATE Output Rise Time	T_{RISE}	—	40	55	ns	C_{GATE} = 2 nF
GATE Output Fall Time	T_{FALL}	—	17	25	ns	C_{GATE} = 2 nF
GATE High Output Voltage	$V_{GATE(HI)}$	V_{DD} – 0.5	—	—	V	I_{GATE} = 10 mA
GATE Low Output Voltage	$V_{GATE(LO)}$	—	—	0.5	V	I_{GATE} = –10 mA
OVERTEMPERATURE PROTECTION						
Over Temperature Trip Limit	T_{OT}	128	140	—	ºC	**Note 2**
Temperature Hysteresis	ΔT_{HYST}	—	60	—	ºC	**Note 2**
ANALOG CONTROL OF PWM DIMMING						
Dimming Frequency	f_{RAMP}	130	—	300	Hz	C_{RAMP} = 47 nF
		550	—	1250		C_{RAMP} = 10 nF
RAMP Threshold, Low	V_{LOW}	—	0.1	—	V	
RAMP Threshold, High	V_{HIGH}	1.8	—	2.1	V	
ADIM Offset Voltage	V_{OS}	–35	—	+35	mV	

Note 1: Limits obtained by design and characterization.

2: For design guidance only

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Temperature	T_A	–40	—	+125	°C	
Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
8-Lead WDFN	θ_{JA}	—	+37	—	°C/W	

2.0 PIN DESCRIPTION

The details on the pins of AT9919 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	CS	Current sense input. Senses LED string current.
2	VIN	Input voltage 4.5V to 40V DC.
3	RAMP	Analog PWM dimming ramp output.
4	ADIM	Analog input signal, 0V~2V, for PWM Dimming control.
5	DIM	PWM Dimming input signal
6	VDD	Internally regulated supply voltage. Connect a capacitor from VDD to ground.
7	GND	Device ground.
8	GATE	Drives GATE of the external MOSFET.
TAB	GND	Must be wired to pin 7 on PCB.

3.0 APPLICATION INFORMATION

3.1 General Description

AT9919 is a step-down constant-current high-brightness LED (HB LED) driver. The device operates from a 4.5V to 40V input voltage range and provides the gate driver output to an external N-channel MOSFET. A high-side current sense resistor sets the output current and a dedicated PWM dimming input (DIM) allows for a wide range of dimming duty ratios. The PWM dimming could also be achieved by applying a DC voltage between 0V and 2V to the analog dimming input (ADIM). In this case, the dimming frequency can be programmed using a single capacitor at the RAMP pin. The high-side current sensing scheme minimizes the number of external components while delivering LED current with a ±8% accuracy, using a 1% sense resistor.

3.2 Undervoltage Lockout (UVLO)

AT9919 includes a 3.7V UVLO with a typical 500 mV hysteresis. When V_{IN} falls below 3.7V, GATE goes low, turning off the external N-channel MOSFET. GATE goes high once V_{IN} is 4.5V or higher.

3.3 5V Regulator

V_{DD} is the output of a 5V regulator capable of sourcing 8 mA. Bypass V_{DD} to GND with a 1 µF capacitor.

3.4 DIM Input

AT9919 allows dimming with a PWM signal at the DIM input. A logic level below 0.7V at DIM forces the $GATE_{OUTPUT}$ low, turning off the LED current. To turn on the LED current, the logic level at DIM must be at least 2.2V.

3.5 ADIM and RAMP Inputs

The PWM dimming scheme can also be implemented by applying an analog control signal to the ADIM pin. If an analog control signal of 0V~2.0V is applied to ADIM, the device compares this analog input to a voltage ramp to pulse width modulate the LED current. Connecting an external capacitor to RAMP programs the PWM dimming ramp frequency. See Equation 3-1.

EQUATION 3-1:

$$f_{PWM} = \frac{1}{C_{RAMP} \times 120k\Omega}$$

The DIM and ADIM inputs can be used simultaneously. In such case, a $f_{PWM(MAX)}$ lower than the frequency of the dimming signal at DIM must be selected. The smaller dimming duty cycle of ADIM and DIM will determine the GATE signal.

When the analog control of PWM dimming feature is not used, RAMP must be wired to GND and ADIM should be connected to V_{DD}.

One possible application of the ADIM feature may include protection of the LED load from overtemperature by connecting an NTC thermistor to ADIM as shown in Figure 3-1.

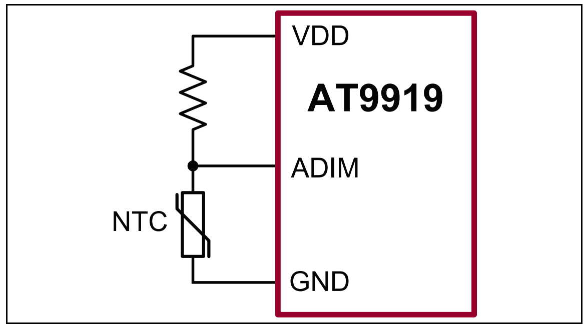


FIGURE 3-1: *Overtemperature Protection using ADIM Pin.*

3.6 Setting LED Current with the External Resistor (R_{SENSE})

The output current in the LED is determined by the external current sense resistor (R_{SENSE}) connected between V_{IN} and CS. Disregarding the effect of the propagation delays, the sense resistor can be calculated as seen in Equation 3-2.

EQUATION 3-2:

$$R_{SENSE} \approx \left(\frac{1}{2}\right) \times \left(\frac{V_{RS(HI)} + V_{RS(LO)}}{I_{LED}}\right) = \frac{200mV}{I_{LED}}$$

3.7 Selecting Buck Inductor (L)

AT9919 regulates the LED output current using an input comparator with hysteresis. (See Figure 3-2.) As the current through the inductor ramps up and the voltage across the sense resistor reaches the upper threshold, the voltage at GATE goes low, turning off the external MOSFET. The MOSFET turns on again when the inductor current ramps down through the freewheeling diode until the voltage across the sense resistor equals the lower threshold.

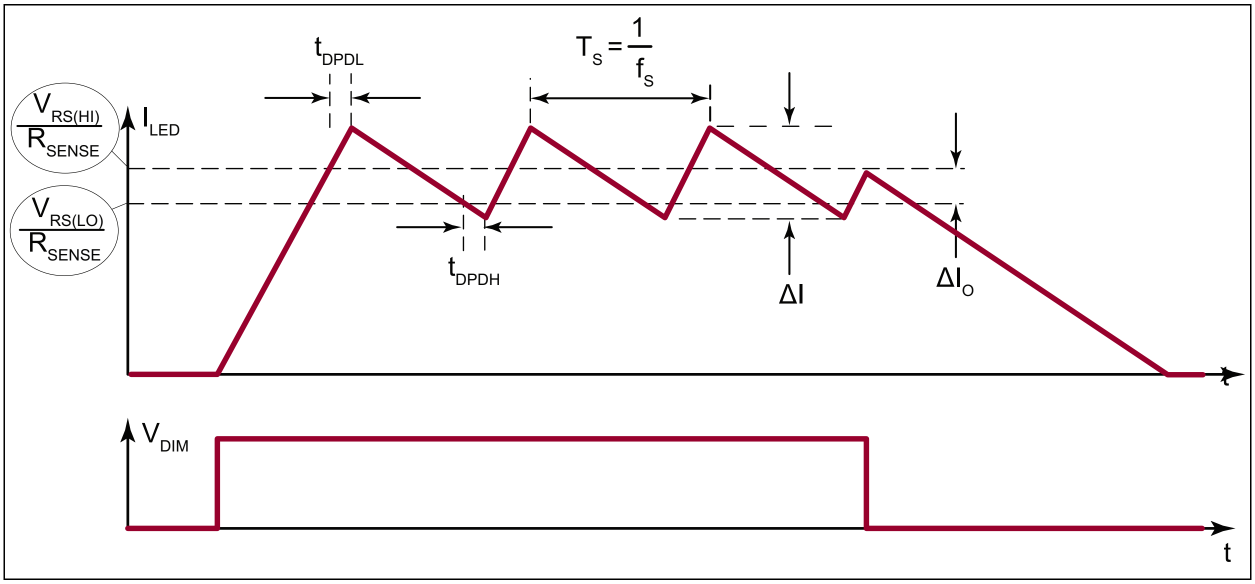


FIGURE 3-2: *Inductor Current Waveform.*

Equation 3-3 shows how to determine the inductor value for a desired operating frequency (f_S).

EQUATION 3-3:

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f_S V_{IN} \Delta I_O} - \frac{(V_{IN} - V_{OUT}) \times t_{DPDL}}{\Delta I_O} - \frac{V_{OUT} t_{DPDH}}{\Delta I_O}$$

Where:

$$\Delta I_O = \frac{V_{RS(HI)} - V_{RS(LO)}}{R_{SENSE}}$$

and t_{DPDL} and t_{DPDH} are the propagation delays.
Note that the current ripple (ΔI) in the inductor (L) is greater than ΔI_O.

The current ripple in the inductor (L) can be calculated with Equation 3-4.

EQUATION 3-4:

$$\Delta I = \Delta I_O + \frac{(V_{IN} - V_{OUT}) \times t_{DPDL}}{L} + \frac{V_{OUT} t_{DPDH}}{L}$$

For proper inductor selection, note that the maximum switching frequency occurs at the highest V_{IN} and $V_{OUT} = V_{IN}/2$.

3.8 MOSFET Selection

MOSFET selection is based on the maximum input operating voltage V_{IN}, output current I_{LED} and operating switching frequency. Choose a MOSFET that has a higher breakdown voltage than the maximum operation voltage, low $R_{DS(ON)}$ and low total charge for better efficiency. MOSFET threshold voltage must be adequate when operated at the low end of the input voltage operating range.

3.9 Freewheeling Diode Selection

The forward voltage of the freewheeling diode should be as low as possible for better efficiency. A Schottky diode is a good choice as long as the breakdown voltage is high enough to withstand the maximum operating voltage. The forward current rating of the diode must be at least equal to the maximum LED current.

3.10 LED Current Ripple

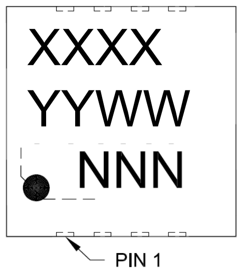
The LED current ripple is equal to the inductor current ripple. In cases when a lower LED current ripple is needed, a capacitor can be placed across the LED terminals.

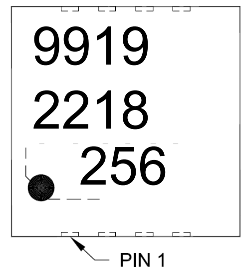
3.11 PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and stable operation. Use a multilayer board whenever possible for better noise immunity. Minimize ground noise by connecting high-current ground returns, the input bypass capacitor ground lead and the output filter ground lead to a single point (star ground configuration). The fast *di/dt* loop is composed of the input capacitor C_{IN}, the freewheeling diode and the MOSFET. To minimize noise interaction, this loop area should be as small as possible. Place R_{SENSE} as close as possible to the input filter and V_{IN}. For better noise immunity, a Kelvin connection is strongly recommended between CS and R_{SENSE}. Connect the exposed tab of the IC to a large area ground plane for improved power dissipation.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information





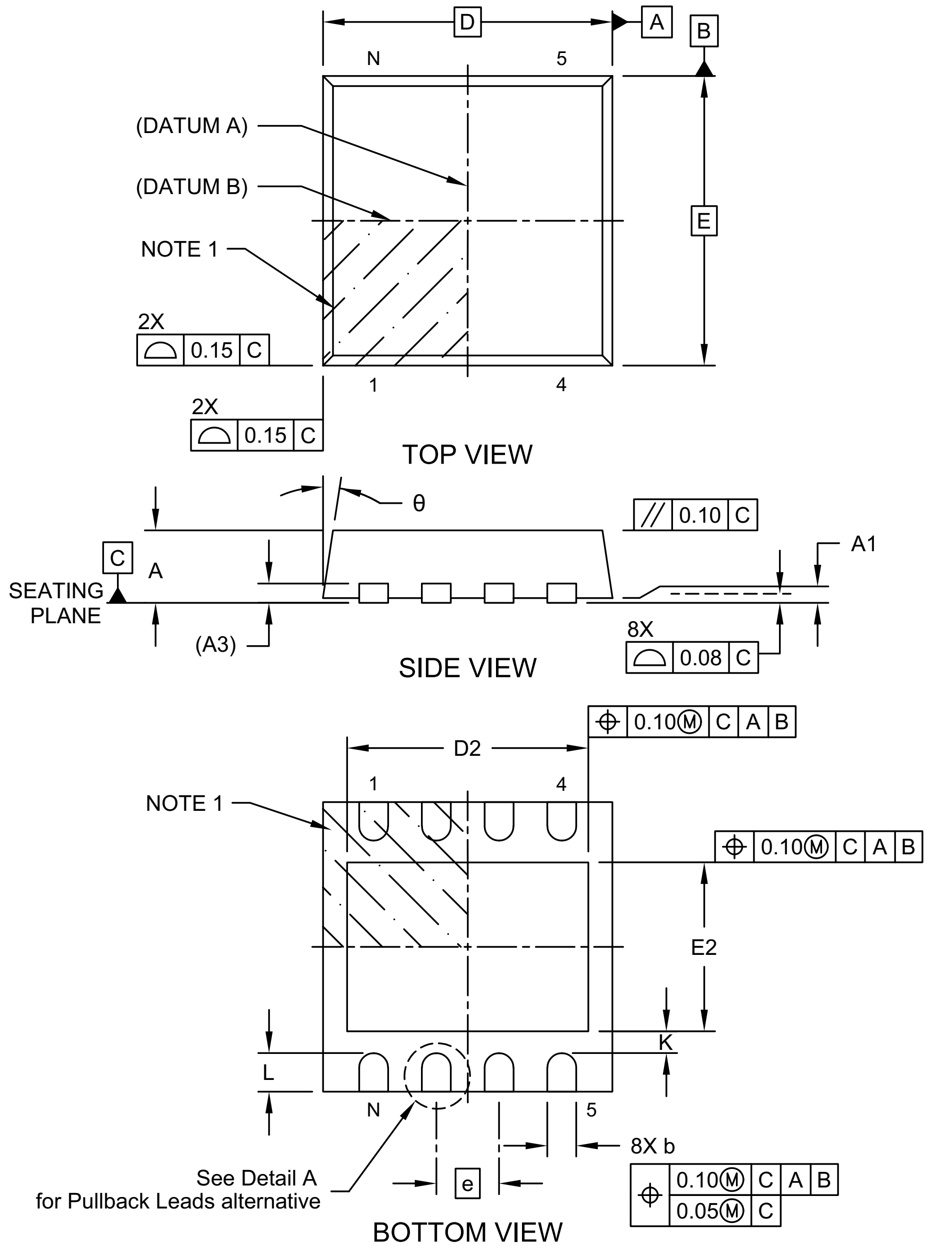
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (UQ) - 3x3 mm Body [WDFN]; Supertex Legacy Package

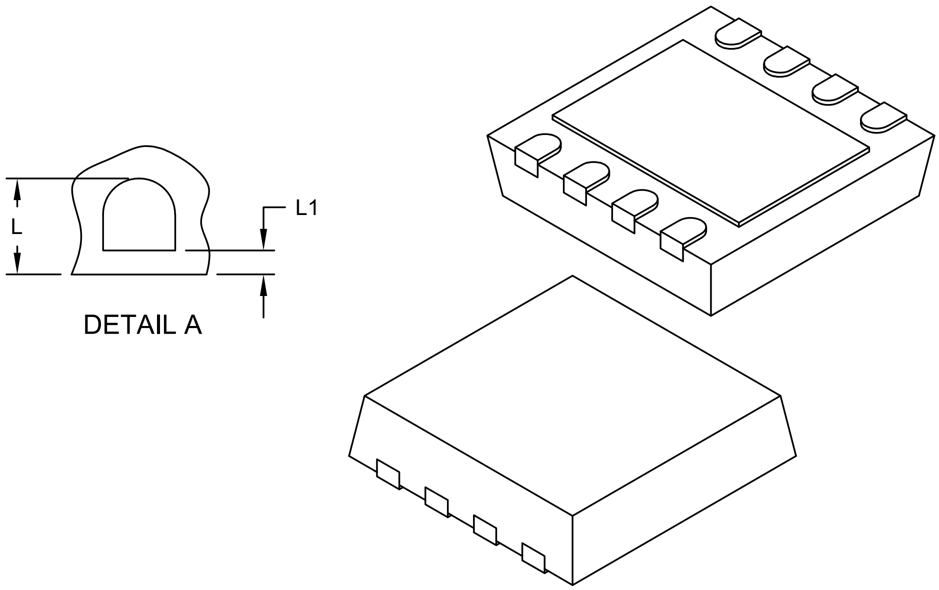
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-291 Rev A Sheet 1 of 2

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (UQ) - 3x3 mm Body [WDFN]; Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.60	-	2.50
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.35	-	1.75
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Pullback	L1	-	-	0.15
Mold Angle	θ	0°	7°	14°
Terminal-to-Exposed-Pad	K	0.20	-	-

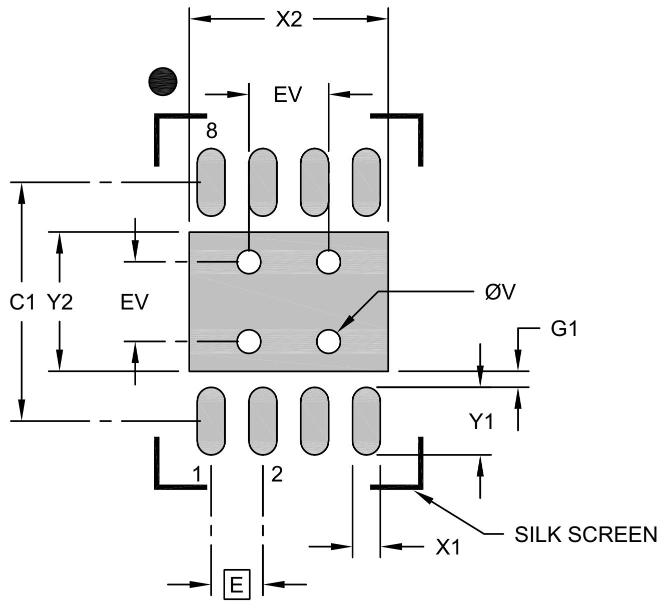
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-291A Sheet 2 of 2

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (UQ) - 3x3 mm Body [WDFN]; Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			2.50
Optional Center Pad Length	Y2			1.75
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2291 Rev A

APPENDIX A: REVISION HISTORY

Revision B (July 2022)

- Added information about the automotive qualification status of the device in **Section "Features"**.
- Updated **Section 4.1 "Package Marking Information"**.
- Modified package type from 8-Lead DFN to 8-Lead WDFN.
- Updated **Section "Product Identification System"**, with Automotive Qualified devices.
- Minor text and format changes throughout.

Revision A (October 2016)

- Converted Supertex Doc# DSFP-AT9919 to Microchip DS20005595A.
- Changed packaging quantity of 8-lead DFN from 3000/Reel to 3300/Reel.
- Made minor text changes throughout the document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-X	XXX
Device	Package Options	Environmental	Qualification

Device:	AT9919	=	Hysteretic Buck High-Brightness LED Driver with High-Side Current Sensing
Package:	K7	=	8-Lead (3x3) WDFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Qualification:	<Blank>	=	Standard Part
	VAO	=	Automotive AEC-Q100 Qualified

Example:

a) AT9919K7-G: Hysteretic Buck High-Brightness LED Driver with High-Side Current Sensing, 8-Lead (3x3) WDFN Package, 3300/Reel

b) AT9919K7-GVAO: Hysteretic Buck High-Brightness LED Driver with High-Side Current Sensing, 8-Lead (3x3) WDFN Pack-age, Automotive Qualified, 3300/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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