AT28LV010

1-Mbit (128K x 8) Industrial Grade Low-Voltage Paged Parallel EEPROM

Features

- Fast Read Access Time: 200 ns
- Automatic Page Write Operation:
  - Internally organized as 131,072 x 8 (1M)
  - Internal address and data latches for 128 bytes
  - Internal control timer
- Fast Write Cycle Time:
  - Page Write cycle time: 10 ms maximum
  - 1 to 128-byte Page Write operation
- Low-Power Dissipation:
  - 15 mA active current
  - 50 µA CMOS standby current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology:
  - Endurance: 100,000 cycles
  - Data retention: 10 years
- Single 3.3V ± 10% Supply
- JEDEC® Approved Byte-Wide Pinout
- Industrial Temperature Range
- Green (Pb/Halide-free) Packaging Option

Packages

- 32-Lead PLCC, 32-Lead TSOP

Table of Contents

Features ... 1

Packages ... 1

1. Package Types (not to scale) ... 4

2. Pin Descriptions ... 5

3. Description ... 6
   - 3.1. Block Diagram ... 6

4. Electrical Characteristics ... 7
   - 4.1. Absolute Maximum Ratings ... 7
   - 4.2. DC and AC Operating Range ... 7
   - 4.3. DC Characteristics ... 7
   - 4.4. Pin Capacitance ... 8

5. Device Operation ... 9
   - 5.1. Operating Modes ... 9
   - 5.2. AC Read Characteristics ... 10
   - 5.3. AC Read Waveforms ... 10
   - 5.4. Input Test Waveforms and Measurement Level ... 11
   - 5.5. Output Test Load ... 11
   - 5.6. AC Write Characteristics ... 11
   - 5.7. AC Write Waveforms ... 12
   - 5.8. Software Protected Write Characteristics ... 13
   - 5.9. Programming Algorithm(1) ... 13
   - 5.10. Software Protected Program Cycle Waveform(1,2,3) ... 14
   - 5.11. $\overline{\text{Data}}$ Polling Characteristics(1) ... 14
   - 5.12. $\overline{\text{Data}}$ Polling Waveforms ... 15
   - 5.13. Toggle Bit Characteristics(1) ... 15
   - 5.14. Toggle Bit Waveforms ... 15

6. Packaging Information ... 17
   - 6.1. Package Marking Information ... 17

7. Revision History ... 20

The Microchip Website ... 21

Product Change Notification Service ... 21

Customer Support ... 21

Product Identification System ... 22

Microchip Devices Code Protection Feature ... 22

Legal Notice ... 23

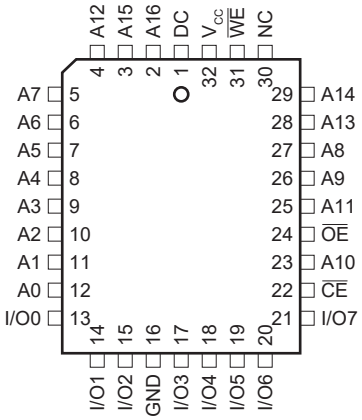
Trademarks ... 23

Quality Management System..... 24

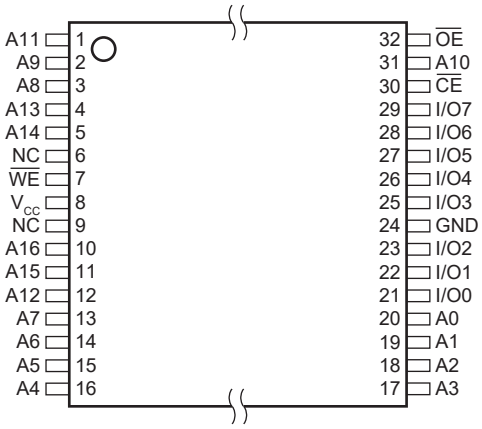
Worldwide Sales and Service.....25

1. Package Types (not to scale)

32-Lead PLCC
Top View



32-Lead TSOP
Top View



2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	32-Lead PLCC	32-Lead TSOP	Function
DC	1	—	Don't Connect
A16	2	10	Address
A15	3	11	Address
A12	4	12	Address
A7	5	13	Address
A6	6	14	Address
A5	7	15	Address
A4	8	16	Address
A3	9	17	Address
A2	10	18	Address
A1	11	19	Address
A0	12	20	Address
I/O0	13	21	Data Input/Output
I/O1	14	22	Data Input/Output
I/O2	15	23	Data Input/Output
GND	16	24	Ground
I/O3	17	25	Data Input/Output
I/O4	18	26	Data Input/Output
I/O5	19	27	Data Input/Output
I/O6	20	28	Data Input/Output
I/O7	21	29	Data Input/Output
$\overline{CE}$	22	30	Chip Enable
A10	23	31	Address
$\overline{OE}$	24	32	Output Enable
A11	25	1	Address
A9	26	2	Address
A8	27	3	Address
A13	28	4	Address
A14	29	5	Address
NC	30	6, 9	No Connect
$\overline{WE}$	31	7	Write Enable
V_{CC}	32	8	Device Power Supply

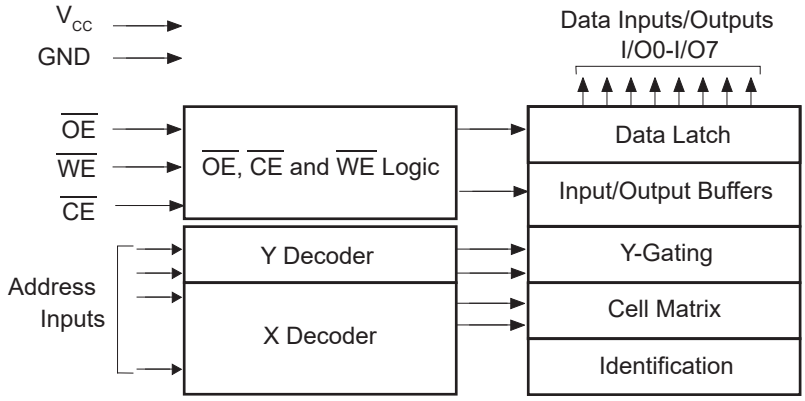
3. Description

The AT28LV010 is a high-performance 3-volt only Electrically Erasable and Programmable Read-Only Memory (EEPROM). Its 1-Mb memory is organized as 131,072 words by 8 bits. Manufactured with Microchip's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 50 µA.

The AT28LV010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ Polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The AT28LV010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. A software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128 bytes of EEPROM for device identification or tracking.

3.1 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
All input voltages (including NC pins) with respect to ground	-0.6V to +6.25V
All output voltages with respect to ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with respect to ground	-0.6V to +13.5V

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

		AT28LV010-20
Operating Temperature (Case)	Industrial	-40°C to +85°C
V_{CC} Power Supply		3.3V ± 10%

4.3 DC Characteristics

Table 4-2. DC Characteristics

Parameter	Symbol	Minimum	Maximum	Units	Test Conditions
Input Load Current	I_{LI}	—	1	µA	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{LO}	—	1	µA	$V_{I/O}$ = 0V to V_{CC}
V_{CC} Standby Current CMOS	I_{SB}	—	50	µA	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V
V_{CC} Active Current	I_{CC}	—	15	mA	f = 5 MHz; I_{OUT} = 0 mA, V_{CC} = 3.6V
Input Low Voltage	V_{IL}	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	V	
Output Low Voltage	V_{OL}	—	0.45	V	I_{OL} = 1.6 mA, V_{CC} = 3.0V
Output High Voltage	V_{OH1}	2.4	—	V	I_{OH} = -100 µA, V_{CC} = 3.0V

4.4 Pin Capacitance

Table 4-3. Pin Capacitance(1,2)

Symbol	Typical	Maximum	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes:

1. This parameter is characterized but is not 100% tested in production.
2. f = 1 MHz, T_A = 25°C

5. Device Operation

READ: The AT28LV010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

WRITE: The write operation of the AT28LV010 allows 1 to 128 bytes of data to be written into the device during a single internal programming period. Each write operation must be preceded by the software data protection (SDP) command sequence. This sequence is a series of three unique write command operations that enable the internal write circuitry. The command sequence and the data to be written must conform to the software protected write cycle timing. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last and data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28LV010 will cease accepting data and commence the internal programming operation. If more than one data byte is to be written during a single programming operation, they must reside on the same page as defined by the state of the A7-A16 inputs. For each $\overline{WE}$ high-to-low transition during the page write operation, A7-A16 must be the same. The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28LV010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next write cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28LV010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Hardware and software features that will protect the memory against inadvertent writes are incorporated.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28LV010 in the following ways:

- V_{CC} power-on delay – once V_{CC} has reached 2.0V, the device will automatically time out 5 ms (typical) before allowing a write
- Write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles
- Noise filter – pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle

SOFTWARE DATA PROTECTION: The AT28LV010 incorporates the industry standard software data protection (SDP) function. Unlike standard 5-volt only EEPROM's, the AT28LV010 has SDP enabled at all times. Therefore, all write operations must be preceded by the SDP command sequence.

The data in the 3-byte command sequence is not written to the device; the addresses in the command sequence can be utilized just like any other location in the device. Any attempt to write to the device without the 3-byte sequence will start the internal timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

5.1 Operating Modes

Table 5-1. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(1)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(2)	X	High-Z

.....continued				
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{WE}$**	**I/O**
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High-Z

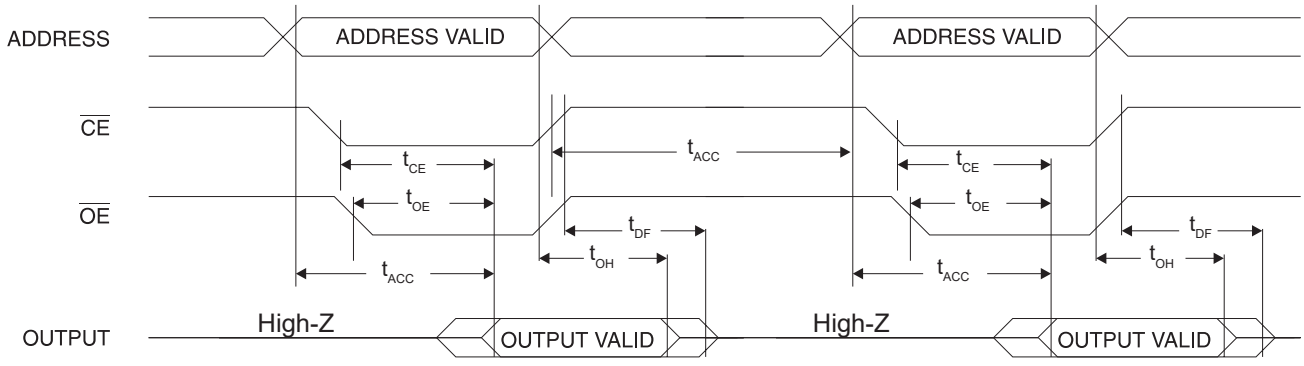
Notes:
1. Refer to AC Programming Waveforms.
2. X can be V_{IL} or V_{IH}.

5.2 AC Read Characteristics

Table 5-2. AC Read Characteristics

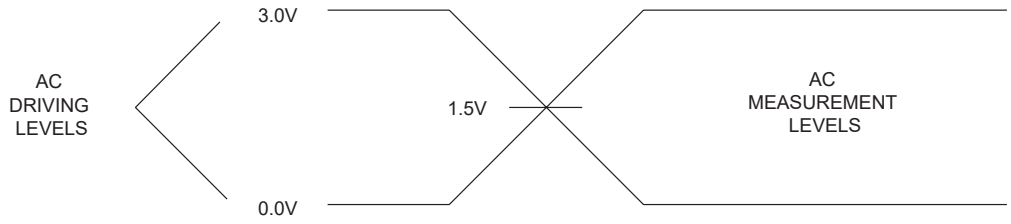
Parameter	Symbol	AT28LV010-20		Units
		Min.	Max.	
Address to Output Delay	t_{ACC}	—	200	ns
$\overline{CE}$ to Output Delay	t_{CE}(1)	—	200	ns
$\overline{OE}$ to Output Delay	t_{OE}(2)	0	80	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float	t_{DF}(3,4)	0	55	ns
Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	t_{OH}	0	—	ns
CE Pulse High Time	t_{CEPH}(5)	50	—	ns

5.3 AC Read Waveforms



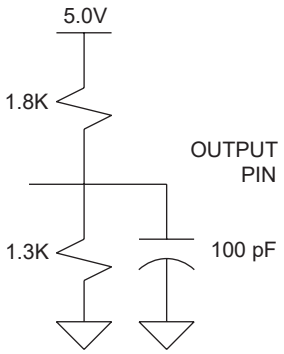
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC}-t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC}-t_{OE} after an address change without impact in t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.
5. If $\overline{CE}$ is de-asserted, it must remain de-asserted for at least 50 ns during read operations otherwise incorrect data may be read.

5.4 Input Test Waveforms and Measurement Level



Note: t_R, t_F < 5 ns.

5.5 Output Test Load



5.6 AC Write Characteristics

Table 5-3. AC Write Characteristics(1)

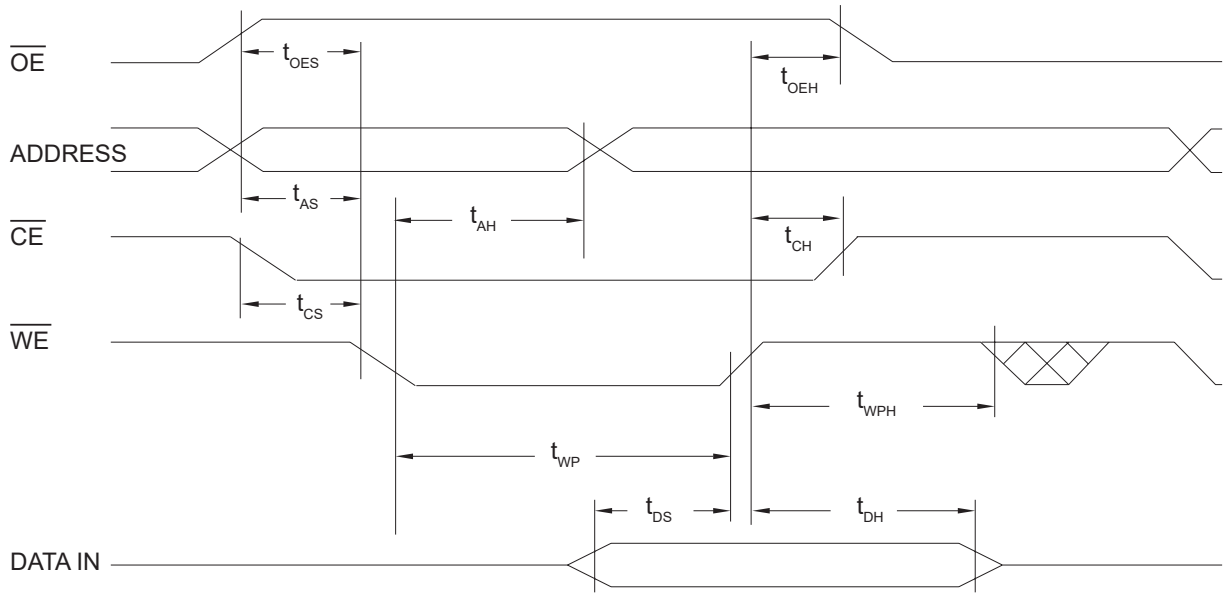
Parameter	Symbol	Minimum	Maximum	Units
Address, $\overline{OE}$ Setup Time	t_{AS}, t_{OES}	0	—	ns
Address Hold Time	t_{AH}	100	—	ns
Chip Select Setup Time	t_{CS}	0	—	ns
Chip Select Hold Time	t_{CH}	0	—	ns
Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	t_{WP}	200	—	ns
Data Setup Time	t_{DS}	100	—	ns
Data, $\overline{OE}$ Hold Time	t_{DH}, t_{OEH}	10	—	ns

Note:

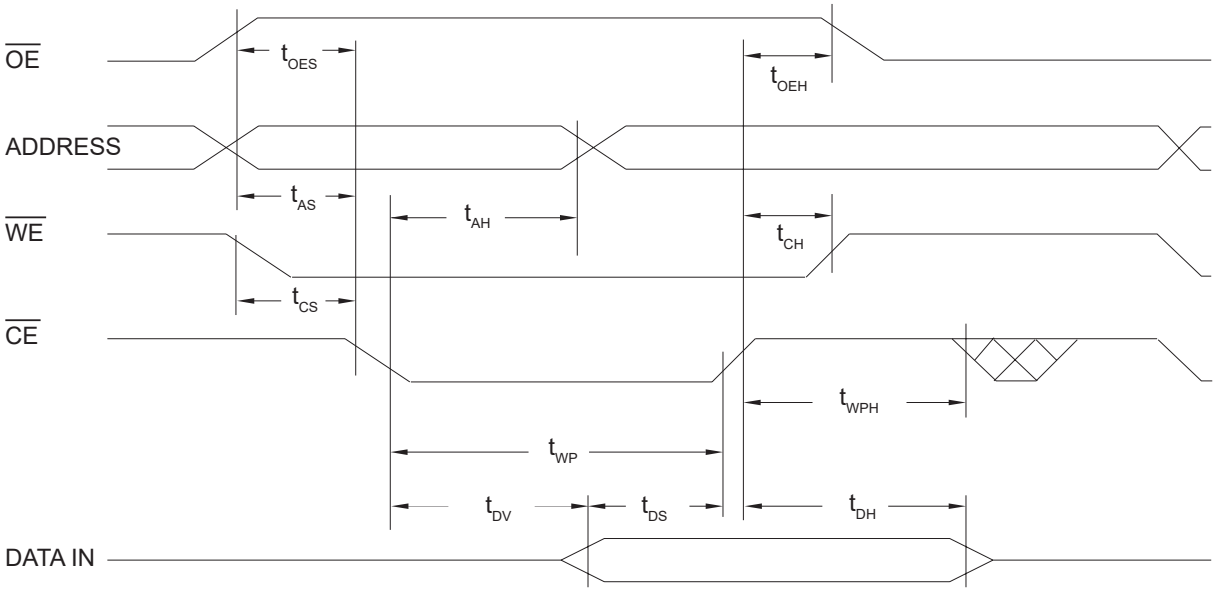
1. All write operations must be preceded by the SDP command sequence.

5.7 AC Write Waveforms

5.7.1 $\overline{WE}$ Controlled



5.7.2 $\overline{CE}$ Controlled

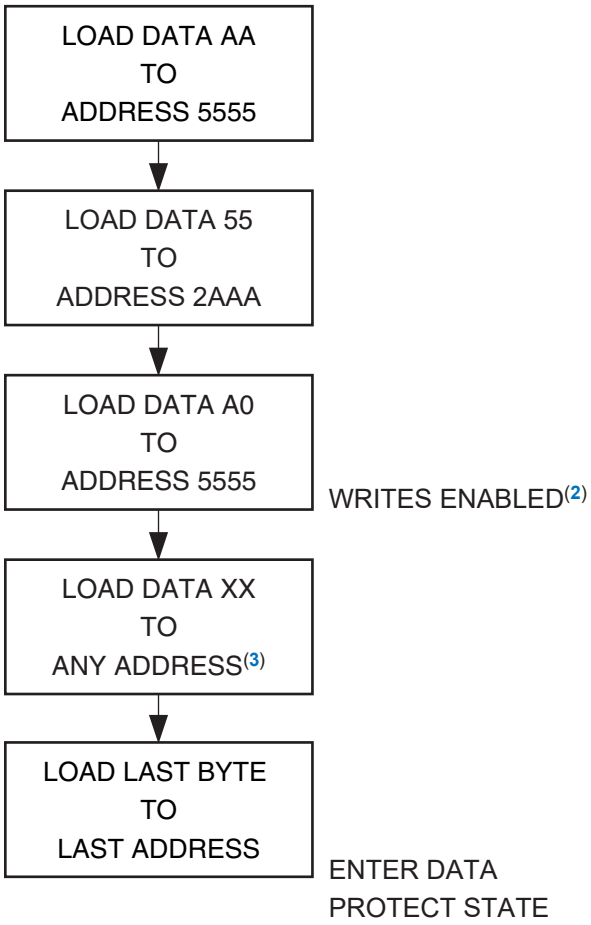


5.8 Software Protected Write Characteristics

Table 5-4. Software Protected Write Characteristics

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t_{WC}	—	10	ms
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	100	—	ns
Data Setup Time	t_{DS}	100	—	ns
Data Hold Time	t_{DH}	10	—	ns
Write Pulse Width	t_{WP}	200	—	ns
Byte Load Cycle Time	t_{BLC}	—	150	µs
Write Pulse Width High	t_{WPH}	100	—	ns

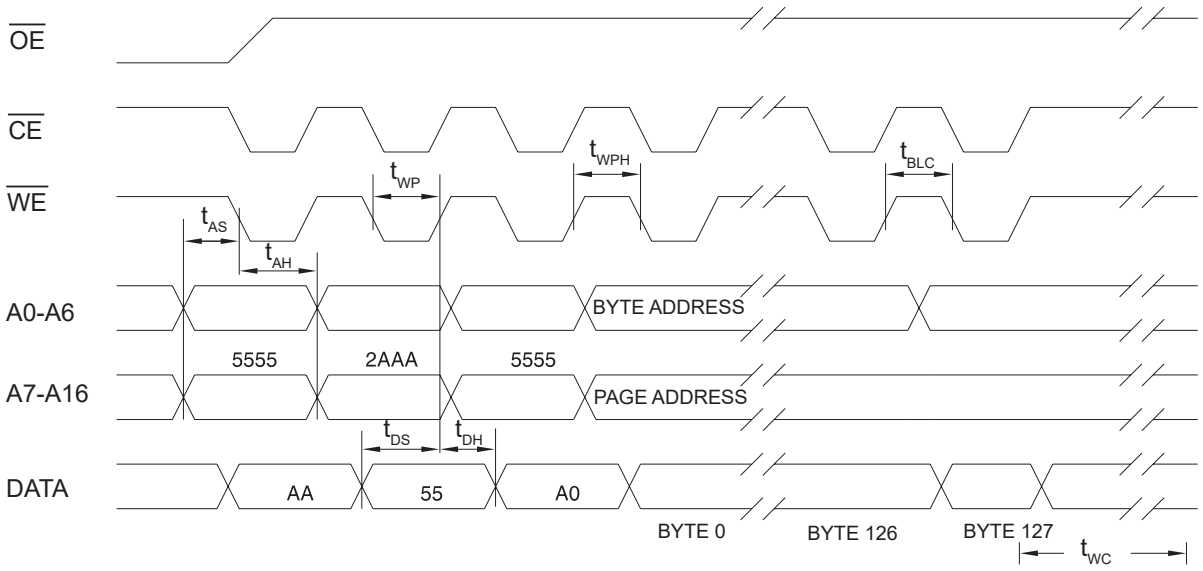
5.9 Programming Algorithm(1)



Notes:

1. Data format: I/O7-I/O0 (Hex); Address format: A16-A0 (Hex).
2. Data Protect state will be re-activated at the end of program cycle.
3. 1 to 128 bytes of data are loaded.

5.10 Software Protected Program Cycle Waveform(1,2,3)



Notes:

1. A0-A16 must conform to the addressing sequence for the first 3 bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A16) must be the same for each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

5.11 $\overline{Data}$ Polling Characteristics(1)

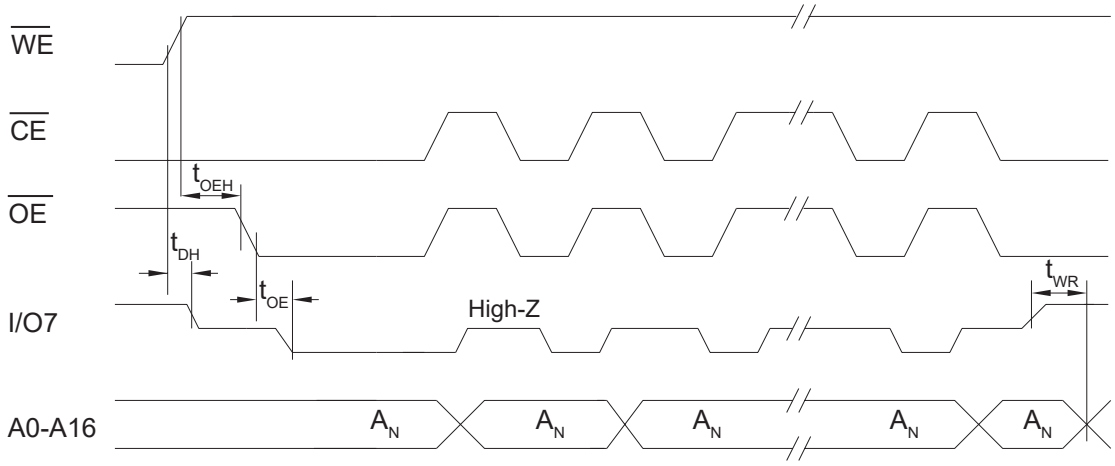
Table 5-5. Data Polling Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t_{DH}	10	—	—	ns
$\overline{OE}$ Hold Time	t_{OEH}	10	—	—	ns
$\overline{OE}$ to Output Delay(2)	t_{OE}	—	—	—	ns
Write Recovery Time	t_{WR}	0	—	—	ns

Notes:

1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

5.12 $\overline{\text{Data}}$ Polling Waveforms



5.13 Toggle Bit Characteristics[1]

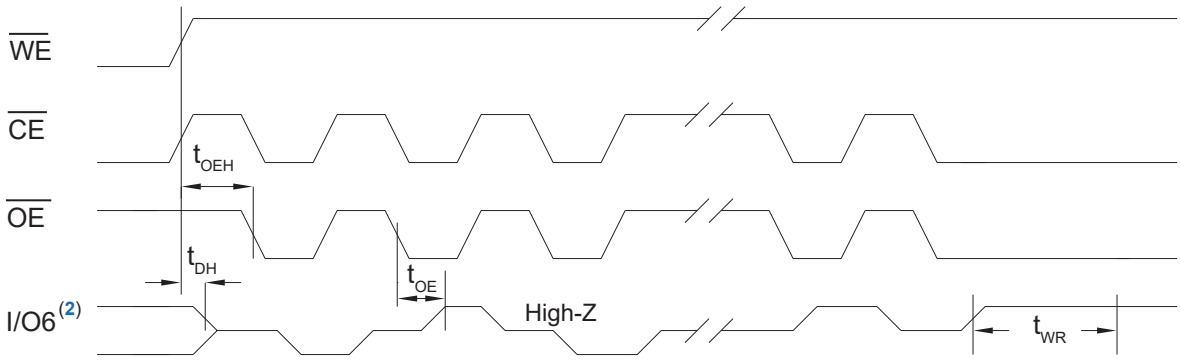
Table 5-6. Toggle Bit Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t_{DH}	10	—	—	ns
$\overline{\text{OE}}$ Hold Time	t_{OEH}	10	—	—	ns
$\overline{\text{OE}}$ to Output Delay[2]	t_{OE}	—	—	—	ns
$\overline{\text{OE}}$ High Pulse[2]	t_{OEHP}	150	—	—	ns
Write Recovery Time	t_{WR}	0	—	—	ns

Notes:

1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

5.14 Toggle Bit Waveforms



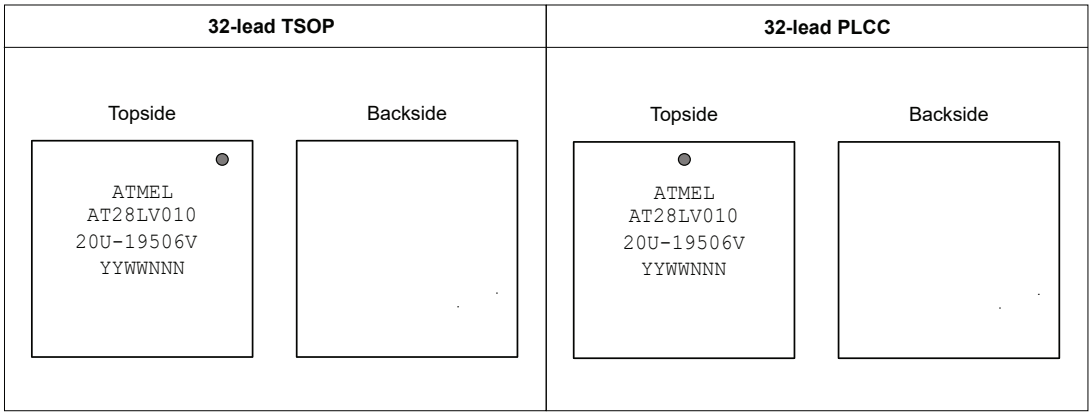
Notes:

1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

6. Packaging Information

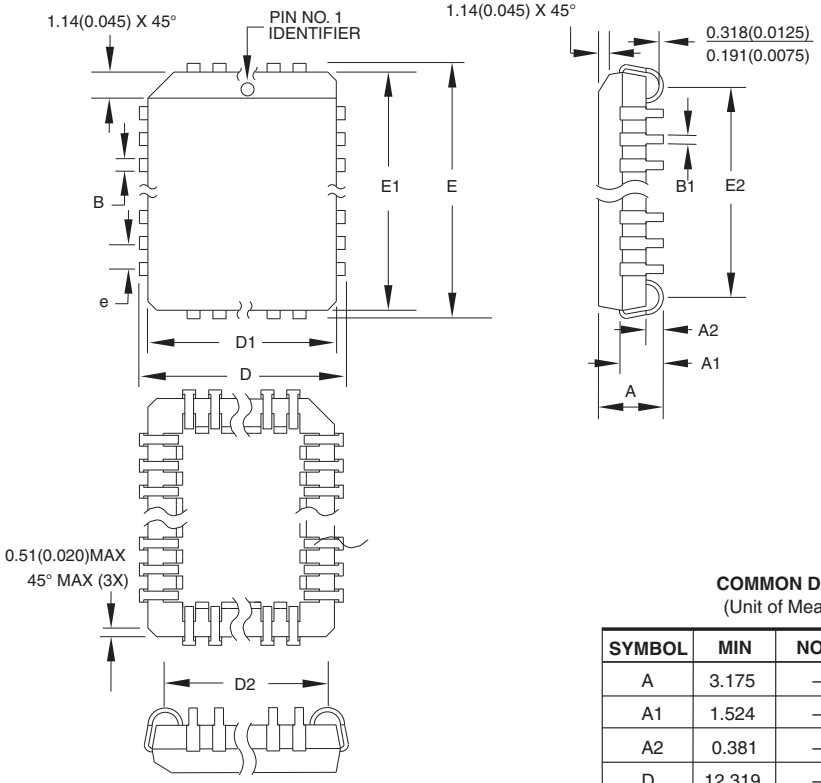
6.1 Package Marking Information

AT28LV010: Package Marking Information (Industrial Grade)



Note: No backside marking on these device packages.

	Lot Trace Code		
	YWWNNN: Lot Trace Code Y: Year, WW: Work Week, NNN: Assembly Trace Code		



Notes: 1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

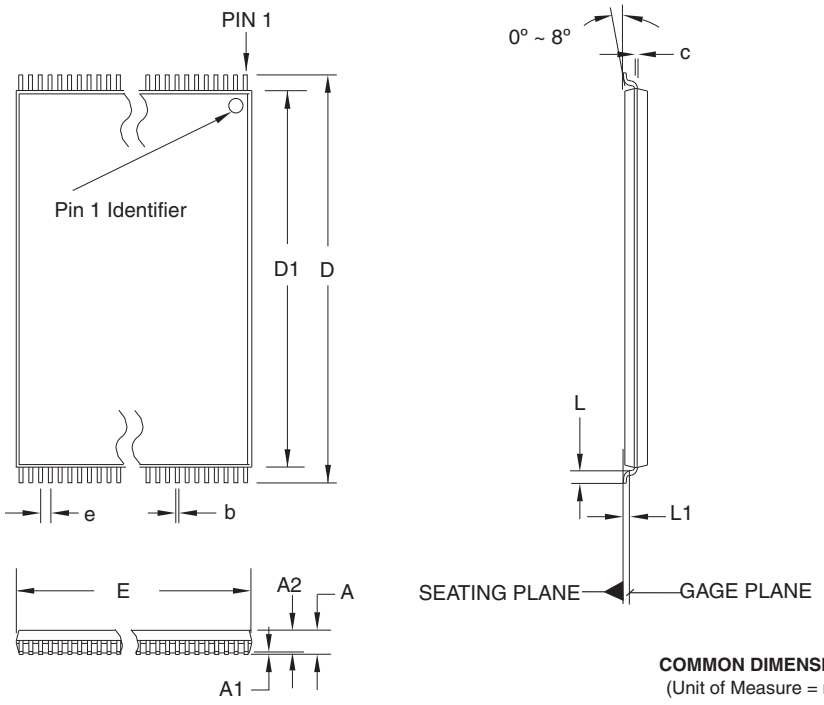
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

10/04/01

	TITLE	DRAWING NO.	REV.
	32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
	32T, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	32T	B

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

7. Revision History

Revision A (August 2020)
Updated to Microchip template. Microchip DS20006405 replaces Atmel document 0395. Added updated Part Markings to include new trace code format.

Atmel Document 0395 Revision F (August 2009)
Added Revision History section. Updated AC Characteristics and ordering information.

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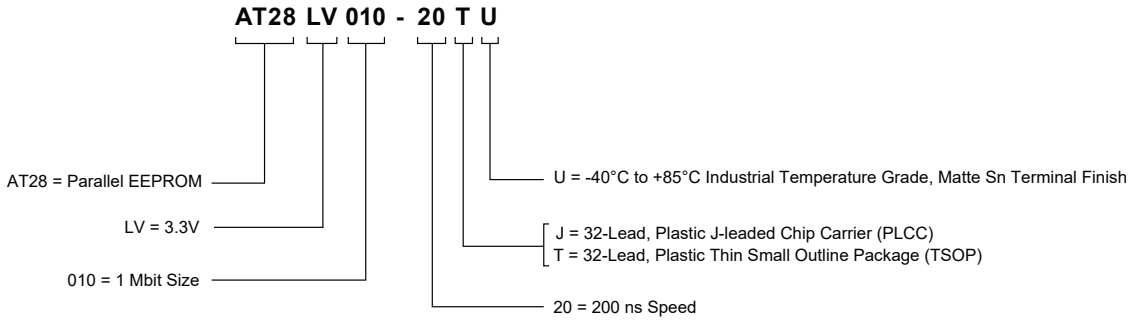
- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Examples

Table 11-1. AT28LV010 Ordering Information

Ordering Code	Package Number	t_{ACC}(ns)	Quantity	Operating Range
AT28LV010-20JU	32J	200	Tube 32	Industrial (-40°C to 85°C)
AT28LV010-20JU-T	32J		Reel 750	
AT28LV010-20TU	32T		Tray 156	
AT28LV010-20TU-T	32T		Reel 1500	

Package Types	
32J	32-Lead, Plastic J-Leaded Carrier (PLCC)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

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