MIC4950

Hyper Speed Control® 5A Buck Regulator

Features

- Input Voltage: 2.7V to 5.5V
- 5A Output Current
- Up to 95% Efficiency
- Up to 3.3 MHz Operation
- Safe Start-Up Into a Pre-Biased Output
- Power Good Output
- Ultra-Fast Transient Response
- Low Output Voltage Ripple
- Low $R_{DS(ON)}$ Integrated MOSFET Switches
- 0.01 µA Shutdown Current
- Thermal Shutdown and Current-Limit Protection
- Output Voltage as Low as 0.7V
- 3 mm x 4 mm 10-Lead FDFN
- –40°C to +125°C Junction Temperature Range

Applications

- DTVs
- Set-Top Boxes
- Printers
- DVD Players
- Distributed Power Supplies

General Description

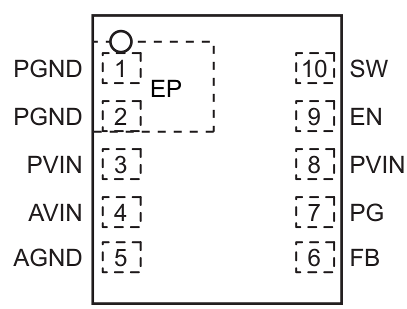
The MIC4950 is a highly efficient, 5A synchronous buck regulator with ultra-fast transient response. It is perfectly suited for supplying processor core and I/O voltages from a 5V or 3.3V bus. The MIC4950 provides a switching frequency up to 3.3 MHz while achieving peak efficiencies up to 95%. An additional benefit of high-frequency operation is very low output ripple voltage throughout the entire load range with the use of a small output capacitor. The MIC4950 is designed for use with a very small inductor, down to 1 µH, and an output ceramic capacitor as small as 10 µF, without the need for external ripple injection. The MIC4950 can also accommodate a wide range of output capacitor types and values.

The MIC4950 supports safe start-up into a pre-biased output, and offers short-circuit and thermal shutdown protections.

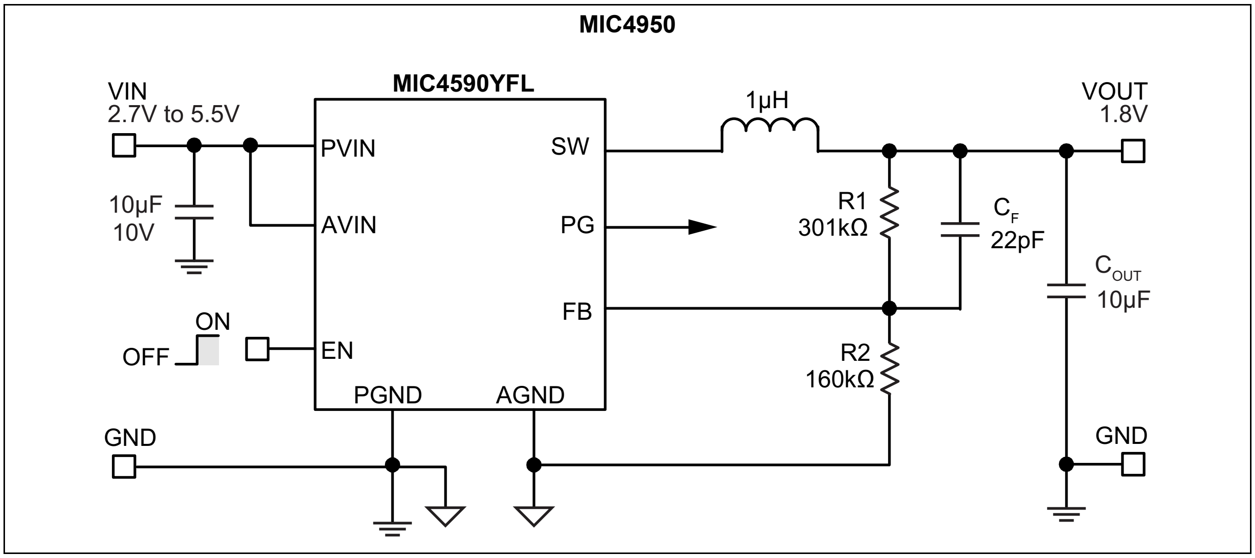
The MIC4950 is available in a 10-lead 3 mm x 4 mm FDFN package with an operating junction temperature range from –40°C to +125°C.

Package Type

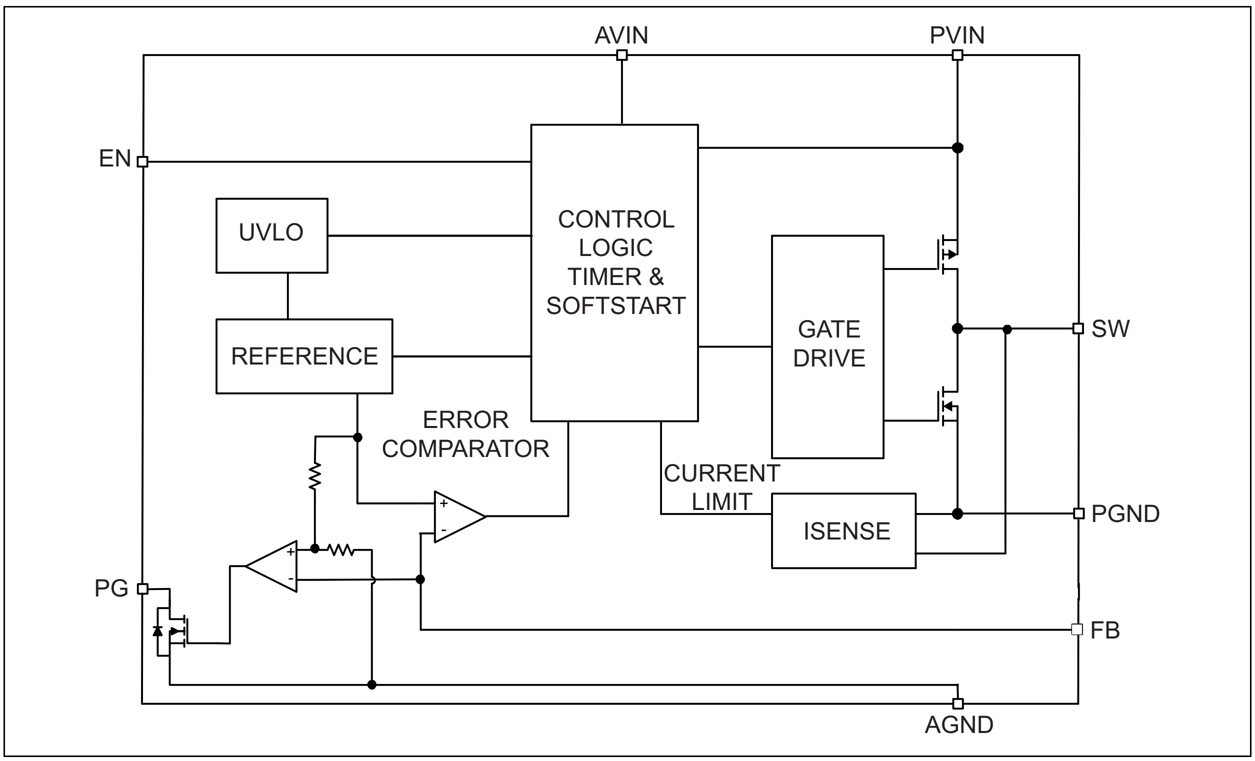
MIC4950
10-Lead FDFN (FL)
(Top View)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PVIN, AVIN Supply Voltage (V_{IN}) .... –0.3V to +6V
SW Output Switch Voltage (V_{SW}) .... –0.3V to V_{IN}
EN, PG (V_{EN}, V_{PG}) .... –0.3V to V_{IN}
FB Feedback Input Voltage (V_{FB}) .... –0.3V to V_{IN}
ESD Rating (Note 1) .... 2 kV, HBM

Operating Ratings ††

Supply Voltage (V_{IN}) .... +2.7V to +5.5V
Enable Input Voltage (V_{EN}) .... 0V to V_{IN}

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = V_{EN} = 3.3V; L = 1.0 µH; C_{IN} = 10 µF; C_{OUT} = 10 µF; T_A = +25°C. **Bold** values valid for –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Range	V_{IN}	**2.7**	—	**5.5**	V	—
Undervoltage Lockout Threshold	V_{UVLO}	**2.41**	2.5	**2.61**	V	Turn-On
Undervoltage Lockout Hysteresis	V_{UVLOH}	—	400	—	mV	—
Quiescent Current	I_Q	—	0.8	**2**	mA	I_{OUT} = 0 mA, FB > 1.2 x $V_{FB(NOM)}$
Shutdown Current	I_{SHDN}	—	0.01	**2**	µA	V_{EN} = 0V
Feedback Voltage	V_{FB}	**0.609**	0.625	**0.64**	V	—
Current Limit	I_{LIMIT}	5.5	7.5	10	A	FB = 0.9 x $V_{FB(NOM)}$
Output Voltage Line Regulation	LINEREG	—	1	—	%/V	V_{IN} = 2.7 to 3.5V, $V_{OUT(NOM)}$ = 1.8V, I_{LOAD} = 20 mA
						V_{IN} = 4.5V to 5.5V if $V_{OUT(NOM)}$ ≥ 2.5V, I_{LOAD} = 20 mA
Output Voltage Load Regulation	LOADREG	—	0.3	—	%	20 mA < I_{LOAD} < 500 mA, V_{IN} = 3.6V if $V_{OUT(NOM)}$ < 2.5V
						20 mA < I_{LOAD} < 500 mA, V_{IN} = 5.0V if $V_{OUT(NOM)}$ ≥ 2.5V
		—	1	—	%	20 mA < I_{LOAD} < 5A, V_{IN} = 3.6V if $V_{OUT(NOM)}$ < 2.5V
						20 mA < I_{LOAD} < 5A, V_{IN} = 5.0V if $V_{OUT(NOM)}$ ≥ 2.5V
PWM Switch ON-Resistance	R_{DSON-P}	—	30	—	mΩ	I_{SW} = 1A, P-Channel MOSFET
	R_{DSON-N}	—	25	—		I_{SW} = –1A, N-Channel MOSFET

Note 1: Specification for packaged product only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{EN} = 3.3V$; L = 1.0 µH; C_{IN} = 10 µF; C_{OUT} = 10 µF; T_A = +25°C. **Bold** values valid for –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Maximum Turn-On Time	t_{ON}	—	665	—	ns	V_{IN} = 4.5V, V_{FB} = 0.5V
		—	1000	—		V_{IN} = 3.0V, V_{FB} = 0.5V
		—	1120	—		V_{IN} = 2.7V, V_{FB} = 0.5V
Minimum Turn-Off Time	t_{OFF}	—	176	—	ns	V_{IN} = 3.0V, V_{FB} = 0.5V
Soft-Start Time	$t_{SOFT-ON}$	—	500	—	µs	V_{OUT} = 90% of $V_{OUT(NOM)}$
Enable Threshold	V_{EN}	**0.5**	0.8	**1.2**	V	Turn-On
Enable Input Current	I_{EN}	—	0.1	**1**	µA	—
Power Good Threshold	V_{OUTPG}	**82**	88	**94**	%	Rising
Power Good Hysteresis	V_{OUTPGH}	—	7	—	%	—
Overtemperature Shutdown	T_{SHDN}	—	150	—	°C	—
Overtemperature Shutdown Hysteresis	T_{SHDNH}	—	20	—	°C	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
Thermal Resistance, FDFN 10-Ld	θ_{JA}	—	35	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

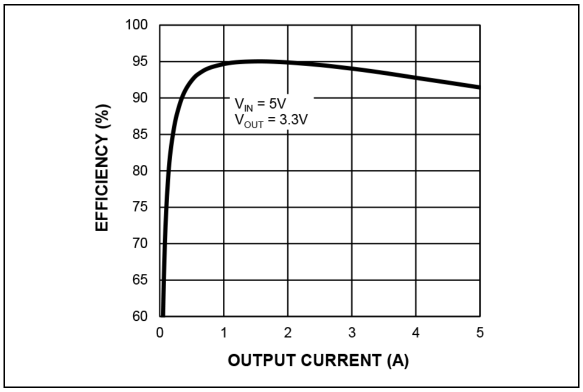


FIGURE 2-1: *Efficiency vs. Output Current.*

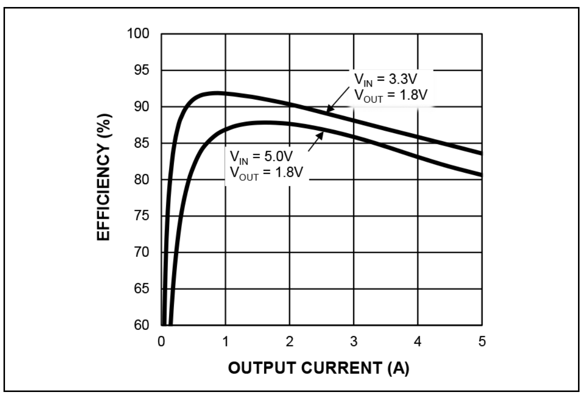


FIGURE 2-2: *Efficiency vs. Output Current.*

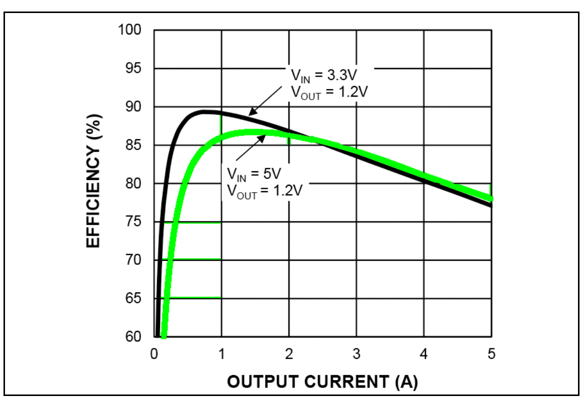


FIGURE 2-3: *Efficiency vs. Output Current.*

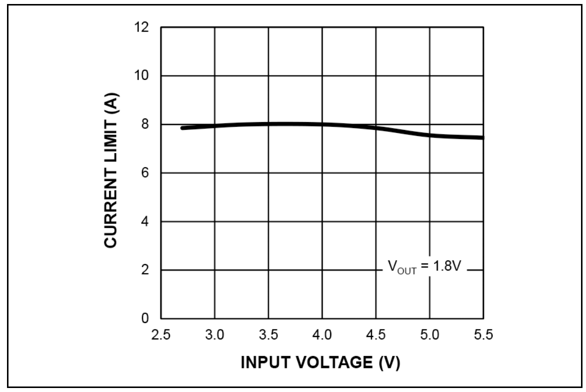


FIGURE 2-4: *Current Limit vs. Input Voltage.*

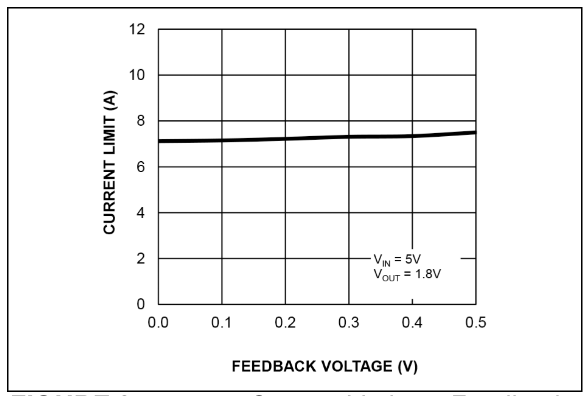


FIGURE 2-5: *Current Limit vs. Feedback Voltage.*

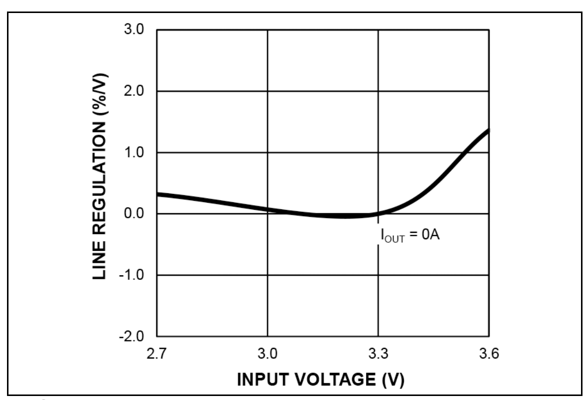


FIGURE 2-6: *Line Regulation vs. Input Voltage.*

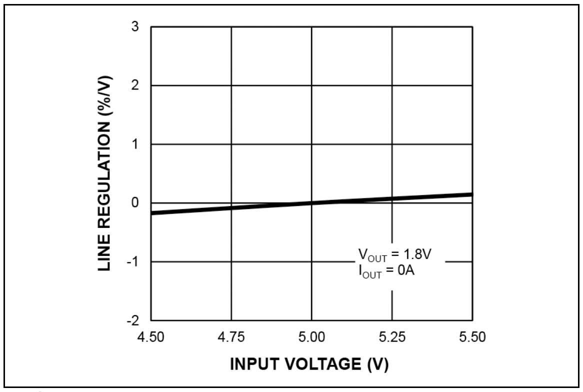


FIGURE 2-7: *Line Regulation vs. Input Voltage.*

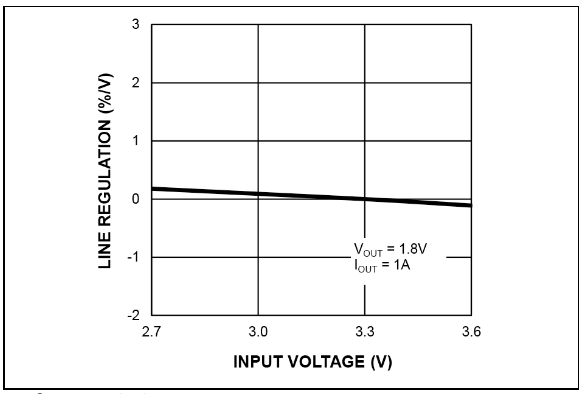


FIGURE 2-8: *Line Regulation vs. Input Voltage.*

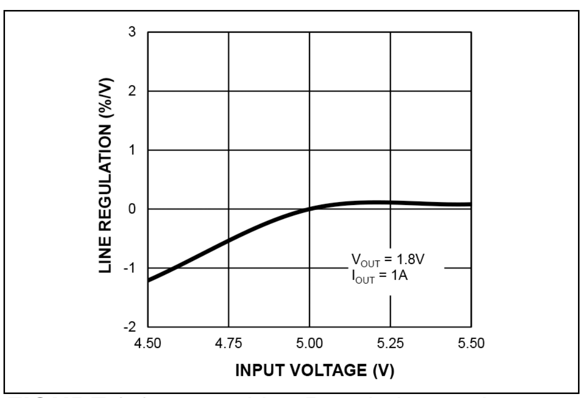


FIGURE 2-9: *Line Regulation vs. Input Voltage.*

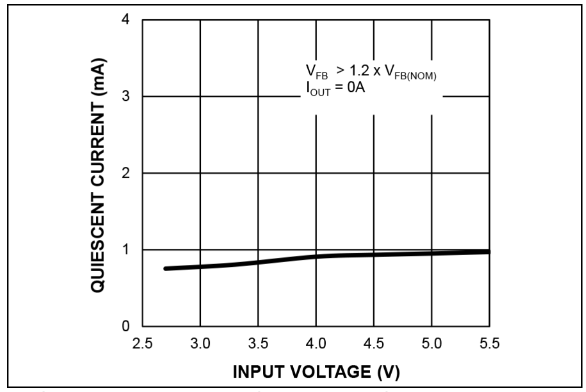


FIGURE 2-10: *Quiescent Current vs. Input Voltage.*

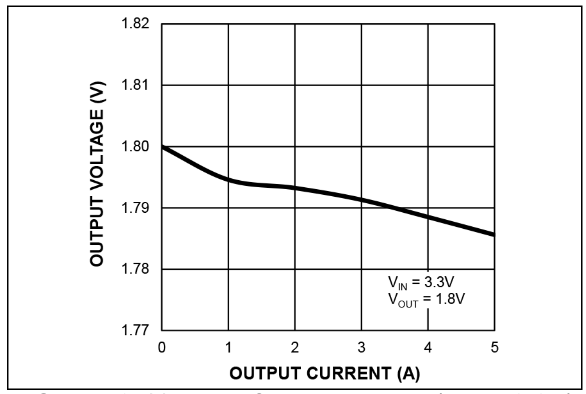


FIGURE 2-11: *Output Voltage (V_{IN} = 3.3V) vs. Output Current.*

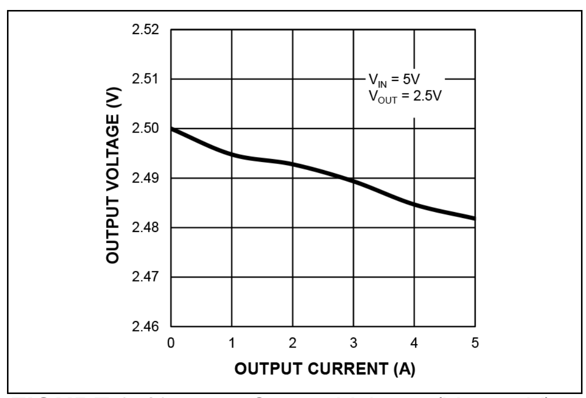


FIGURE 2-12: *Output Voltage (V_{IN} = 5V) vs. Output Current.*

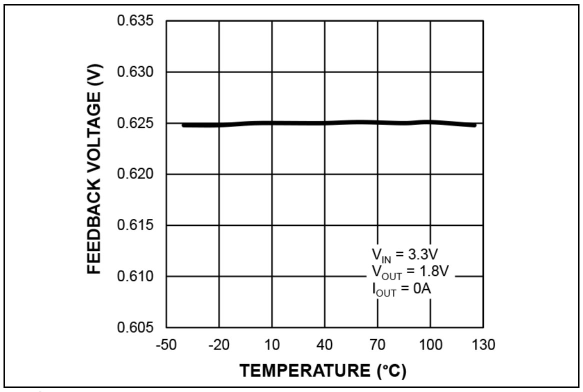


FIGURE 2-13: *Feedback Voltage vs. Temperature.*

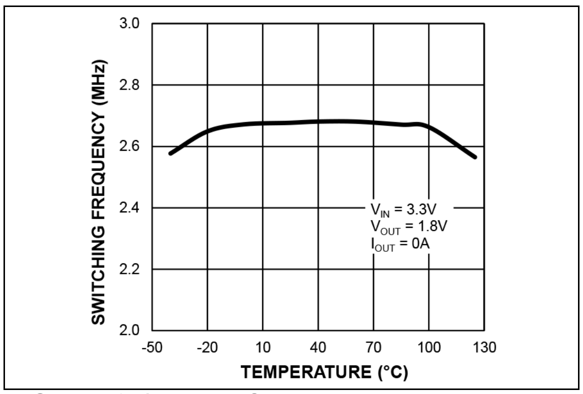


FIGURE 2-14: *Switching Frequency vs. Temperature.*

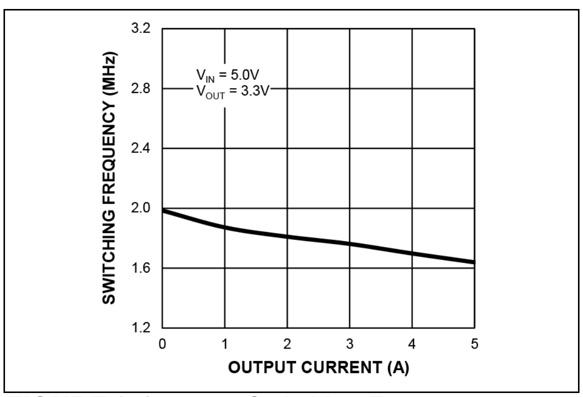


FIGURE 2-15: *Switching Frequency vs. Output Current.*

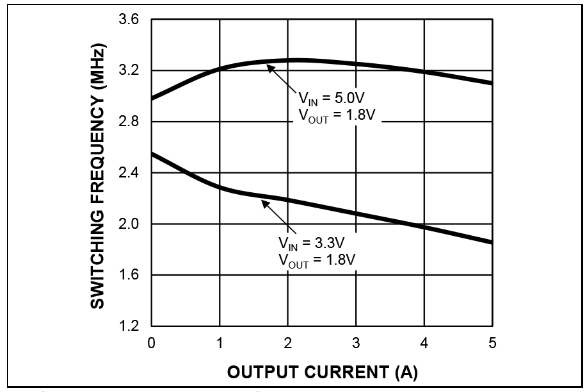


FIGURE 2-16: *Switching Frequency vs. Output Current.*

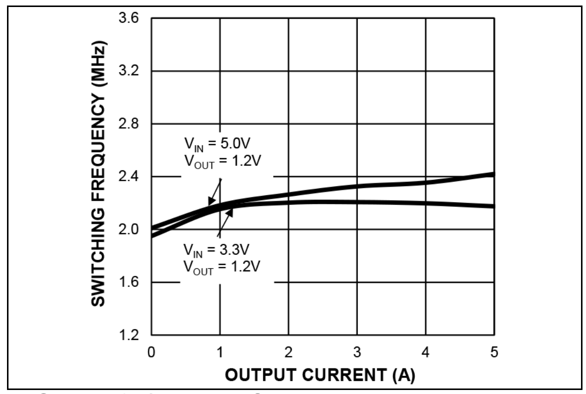


FIGURE 2-17: *Switching Frequency vs. Output Current.*

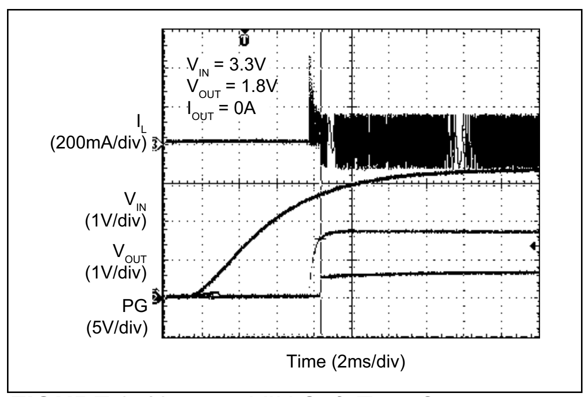


FIGURE 2-18: *VIN Soft Turn-On.*

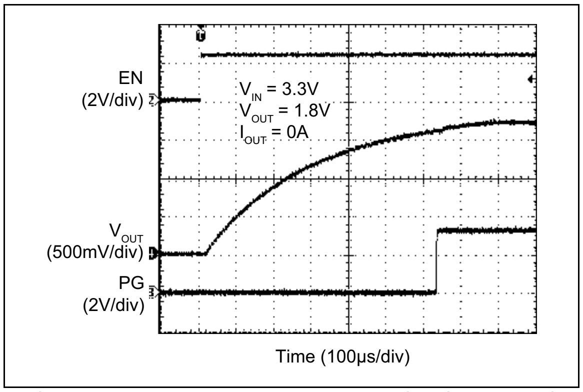


FIGURE 2-19: *Enable Turn-On (No Load).*

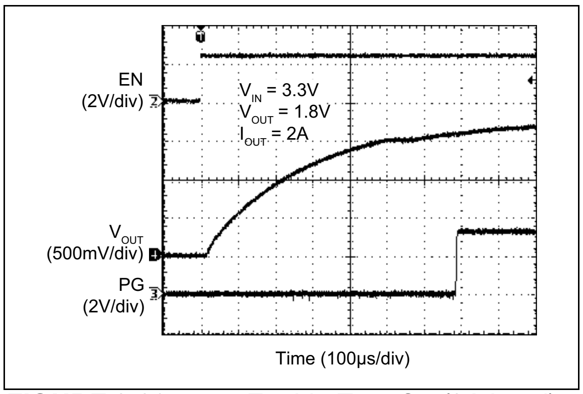


FIGURE 2-20: *Enable Turn-On (2A Load).*

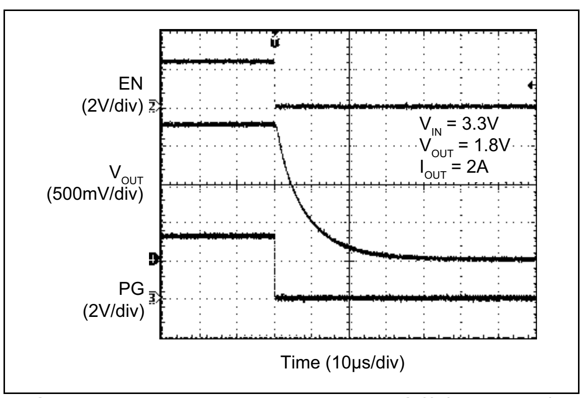


FIGURE 2-21: *Enable Turn-Off (2A Load).*

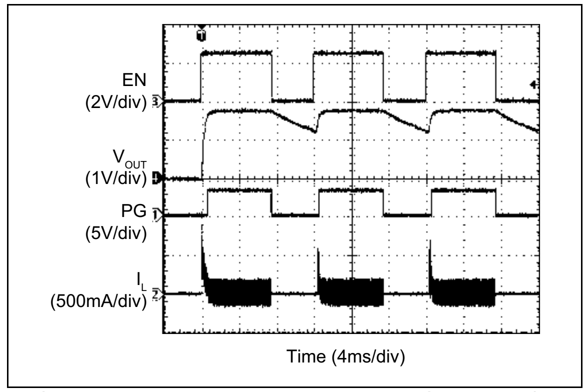


FIGURE 2-22: *1.4V Pre-Bias Start-Up (EN Rising).*

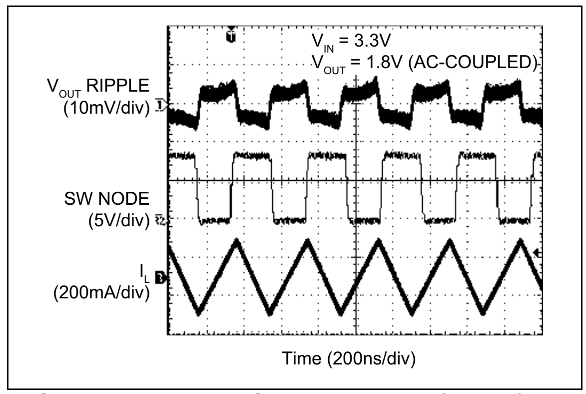


FIGURE 2-23: *Switching Waveforms (I_{OUT} = 0A).*

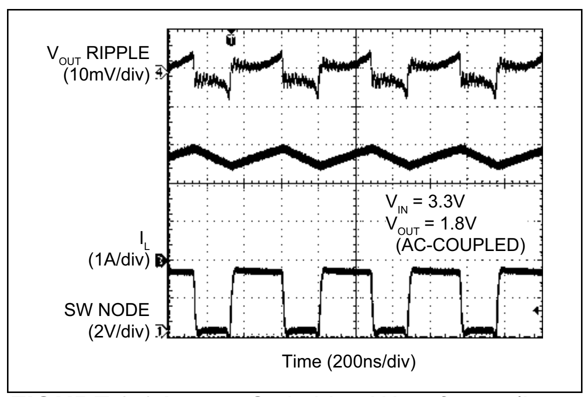


FIGURE 2-24: *Switching Waveforms (I_{OUT} = 2.5A).*

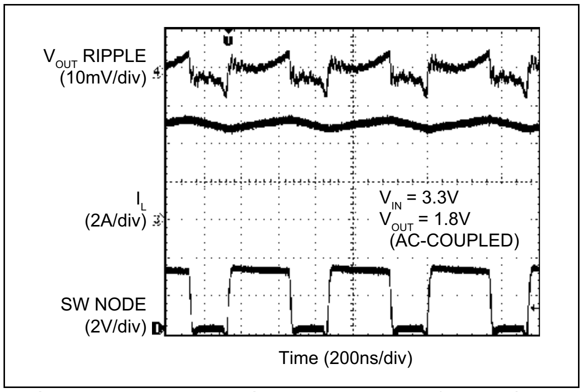


FIGURE 2-25: *Switching Waveforms (I_{OUT} = 5A).*

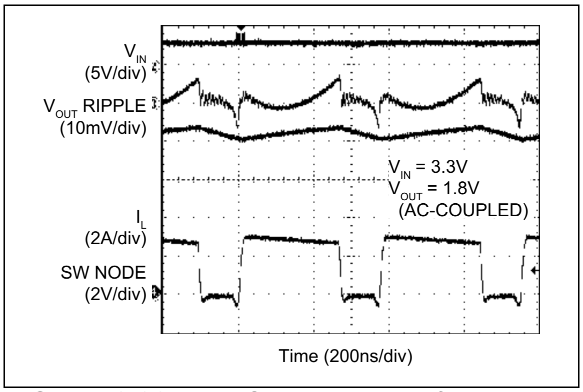


FIGURE 2-26: *Switching Waveforms (Current Limit).*

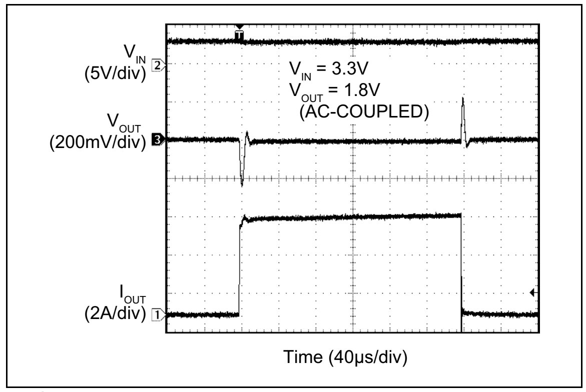


FIGURE 2-27: *Load Transient Response (I_{OUT} = 5A).*

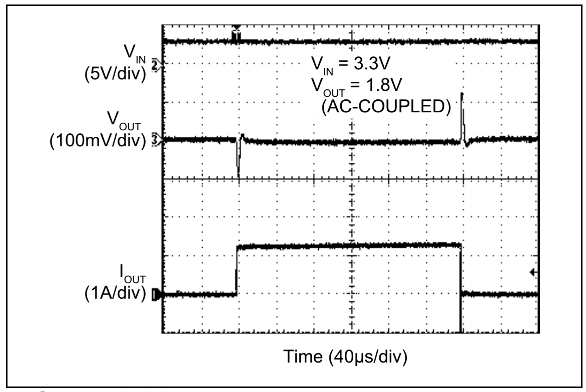


FIGURE 2-28: *Load Transient Response (I_{OUT} = 2.5A).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number FDFN-10	Pin Name	Description
1, 2, EP	PGND	Power Ground.
3, 8	PVIN	Power Input Voltage: Connect a 10 µF ceramic capacitor between PVIN and PGND for input decoupling. Pins 3 and 8 are internally connected.
4	AVIN	Analog Input Voltage: Connect a 1 µF ceramic capacitor between AVIN and AGND to decouple the noise from the internal reference and error comparator.
5	AGND	Analog Ground Input: Connect to a quiet ground plane for best operation. Do not route power switching currents on the AGND net. Connect AGND and PGND nets together at a single point.
6	FB	Feedback (Input): Connect an external divider between VOUT and AGND (Analog Ground) to program the output voltage.
7	PG	Power Good (Output): Open-drain output. A pull-up resistor from this pin to a voltage source is required to detect an output power-is-good condition.
9	EN	Enable (Input): Logic high enables operation of the regulator. Logic low shuts down the device. Do not leave floating.
10	SW	Switch (Output): Internal power MOSFET output switches.

4.0 FUNCTIONAL DESCRIPTION

4.1 PVIN

The power input (PVIN) pin provides power to the internal MOSFETs for the switch mode regulator section of the MIC4950. The input supply operating range is from 2.7V to 5.5V. A low-ESR ceramic capacitor of at least 10 µF is required for bypass from PVIN to (Power) GND. See the “Applications Information” section for further details.

4.2 AVIN

The analog power input (AVIN) pin provides power to the internal control and analog supply circuitry. Careful layout is important to ensure that high-frequency switching noise caused by PVIN is reduced before reaching AVIN. Always place a 1 µF minimum ceramic capacitor very close to the IC between AVIN and AGND pins. For additional high-frequency switching noise attenuation, RC filtering can be used (R = 10Ω).

4.3 EN

A logic high signal on the enable (EN) pin activates the output of the switch. A logic low on the EN pin deactivates the output and reduces the supply current to the nominal 0.01 µA. Do not leave this pin floating.

4.4 SW

The switch (SW) pin connects directly to one side of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load and output capacitor. Due to the high-speed switching on this pin, the switch node should be routed away from sensitive nodes, whenever possible, to avoid unwanted injection of noise.

4.5 PGND

The power ground (PGND) is the ground return terminal for the high current in the switching node SW. The current loop for the PGND should be as short as possible and kept separate from the AGND net whenever applicable.

4.6 AGND

The analog ground (AGND) is the ground return terminal for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop. Refer to the “PCB Layout Recommendations” section for further details.

4.7 PG

The power-is-good (PG) pin is an open-drain output that indicates logic high when the output voltage is typically above 88% of its steady-state voltage. A pull-up resistor of 10 kΩ or greater should be connected from PG to VOUT.

4.8 FB

To program the output voltage, an external resistive divider network is connected to this pin from the output voltage to AGND, as shown in the Typical Application circuit, and is compared to the internal 0.625V reference within the regulation loop. Equation 4-1 is used to program the output voltage:

EQUATION 4-1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Table 4-1 lists recommended feedback resistor values.

TABLE 4-1: RECOMMENDED RESISTOR FEEDBACK VALUES

V_{OUT}	R1	R2
1.0V	120 kΩ	180 kΩ
1.2V	274 kΩ	294 kΩ
1.5V	316 kΩ	226 kΩ
1.8V	301 kΩ	160 kΩ
2.5V	316 kΩ	105 kΩ
3.3V	309 kΩ	71.5 kΩ

4.9 Hyper Speed Control®

MIC4950 uses an ON- and OFF-time proprietary ripple-based control loop that features three different timers:

- Minimum ON-Time
- Maximum ON-Time
- Minimum OFF-Time

When the required duty cycle is very low, the required OFF-time is typically far from the Minimum OFF-time limit (about 176 ns typ). In this case, the MIC4950 operates by delivering at each switching cycle a determined ON-time (dependent on the input voltage). A new ON-time is invoked by the error comparator when the FB voltage falls below the regulation threshold. In this mode the MIC4950 operates as an adaptive Constant-ON-Time ripple controller, with nearly constant switching frequency. Regulation takes place by controlling the valley of the FB ripple waveform.

When higher duty cycles are required, regulation can no longer be maintained by decreasing the OFF-time below the Minimum OFF-time limit. When this limit is reached, then the OFF-time is no longer reduced, and the MIC4950 smoothly transitions to an ON-time modulation mode. In the ON-time modulation region, frequency reduces with the increase of the required ON-time/duty cycle, and regulation finally takes place on the peak of the FB ripple waveform.

Note that because of the shift of the regulation threshold between different modes, line regulation might suffer when the input voltage and/or duty cycle variations force the MIC4950 to switch form one regulation mode to the other. In applications where wide input voltage variations are expected, ensure that the line regulation is adequate for the intended application.

5.0 APPLICATION INFORMATION

The MIC4950 is a highly efficient, 5A synchronous buck regulator ideally suited for supplying processor core and I/O voltages from a 5V or 3.3V bus.

5.1 Input Capacitor

A 10 µF ceramic capacitor or greater should be placed close to the PVIN pin and PGND pin for bypassing. A X5R or X7R temperature rating is recommended for the input capacitor. It is important to take into account C versus bias effect to estimate the effective capacitance and the input ripple at the V_{IN} voltage.

5.2 Output Capacitor

The MIC4950 is designed for use with a 10 µF or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response. A low equivalent-series resistance (ESR) ceramic output capacitor is recommended based on performance, size, and cost. Ceramic capacitors with X5R or X7R temperature ratings are recommended.

5.3 Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)
- Core losses

The MIC4950 is designed for use with a 1 µH to 2.2 µH inductor. For faster transient response, a 1 µH inductor will yield the best result. For lower output ripple, a 2.2 µH inductor is recommended.

Inductor current ratings are generally given in two methods: permissible DC current, and saturation current. Permissible DC current can be rated for a 20°C to 40°C temperature rise. Saturation current can be rated for a 10% to 30% loss in inductance. Make sure that the nominal current of the application is well within the permissible DC current ratings of the inductor, also depending on the allowed temperature rise. Note that the inductor permissible DC current rating typically does not include inductor core losses. These are a very important contribution to the total inductor core loss and temperature increase in high-frequency DC-to-DC converters, because core losses increase with at least the square of the excitation frequency. For more accurate core loss estimation, refer to manufacturers' data sheets or websites.

When saturation current is specified, make sure that there is enough design margin, so that the peak current does not cause the inductor to enter saturation.

Also pay attention to the inductor saturation characteristic in current limit. The inductor should not heavily saturate even in current limit operation, otherwise the current might instantaneously run away and reach potentially destructive levels. Typically, ferrite-core inductors exhibit an abrupt saturation characteristic, while powdered-iron or composite inductors have a soft-saturation characteristic.

Peak current can be calculated in Equation 5-1:

EQUATION 5-1:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT} \times \left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L}\right)\right]$$

As shown by the calculation above, the peak inductor current is inversely proportional to the switching frequency and the inductance. The lower the switching frequency or inductance, the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the Typical Application circuit and the Bill of Materials in the MIC4950 Evaluation Board User's Guide for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the "Efficiency Considerations" subsection.

5.4 Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied (see the Typical Characteristics curves):

EQUATION 5-2:

$$Efficiency\ \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

There are two types of losses in switching converters: DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high-side switch during the ON cycle. Power loss is equal to the high-side MOSFET $R_{DS(ON)}$ multiplied by the switch current squared. During the OFF cycle, the low-side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required to drive the gates on and off at high frequency and the switching transitions make up the switching losses.

At the higher currents for which the MIC4950 is designed, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor losses. Higher input supply voltages will increase the gate-to-source threshold on the internal MOSFETs, thereby reducing the internal $R_{DS(ON)}$. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In this case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as in Equation 5-3.

EQUATION 5-3:

$$P_{DCR} = I_{OUT}^{2} \times DCR$$

From that, the loss in efficiency due to inductor DCR and core losses (P_{CORE}) can be calculated as in Equation 5-4.

EQUATION 5-4:

$$EL = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{DCR} + P_{CORE}}\right)\right] \times 100$$

Where:
EL = Efficiency loss value in percent.

5.5 External Ripple Injection

The MIC4950 control loop is ripple-based and relies on an internal ripple injection network to generate enough ripple amplitude at the FB pin when negligible output voltage ripple is present. The internal ripple injection network is typically sufficient when recommended R1-R2 and C_F values are used. The FB ripple amplitude should fall in the 20 mV to 100 mV range.

If significantly lower divider resistors and/or higher C_F values are used, the amount of internal ripple injection may not be sufficient for stable operation. In this case, external ripple injection is needed. This is accomplished by connecting a series R_{inj}-C_{inj} circuit between the SW and the FB pins, as shown in Figure 5-1.

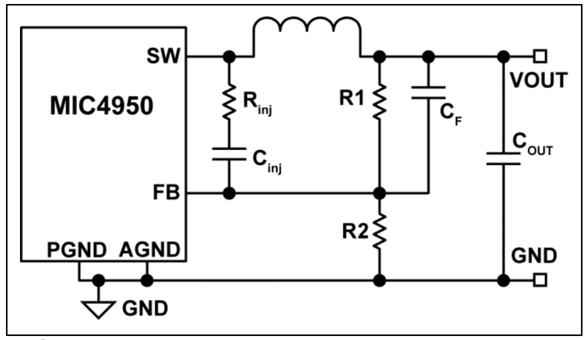


FIGURE 5-1: External Ripple Injection.

The injected ripple is calculated using Equation 5-5.

EQUATION 5-5:

$$\Delta V_{FB(PP)} = V_{IN} \times K_{DIV} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

Where:
V_{IN} = Power stage input voltage
D = Duty cycle
f_{SW} = Switching frequency
$\tau = (R1//R2//R_{inj}) \times C_F$

K_{DIV} is calculated using Equation 5-6.

EQUATION 5-6:

$$K_{DIV} = \frac{R1//R2}{R_{inj} + R1//R2}$$

In both equations, it is assumed that the time constant associated with C_F must be much greater than the switching period:

EQUATION 5-7:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1$$

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

10-Lead DFN*	Example
XXX XXXX NNN ●	MIC 4950 994 ●

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

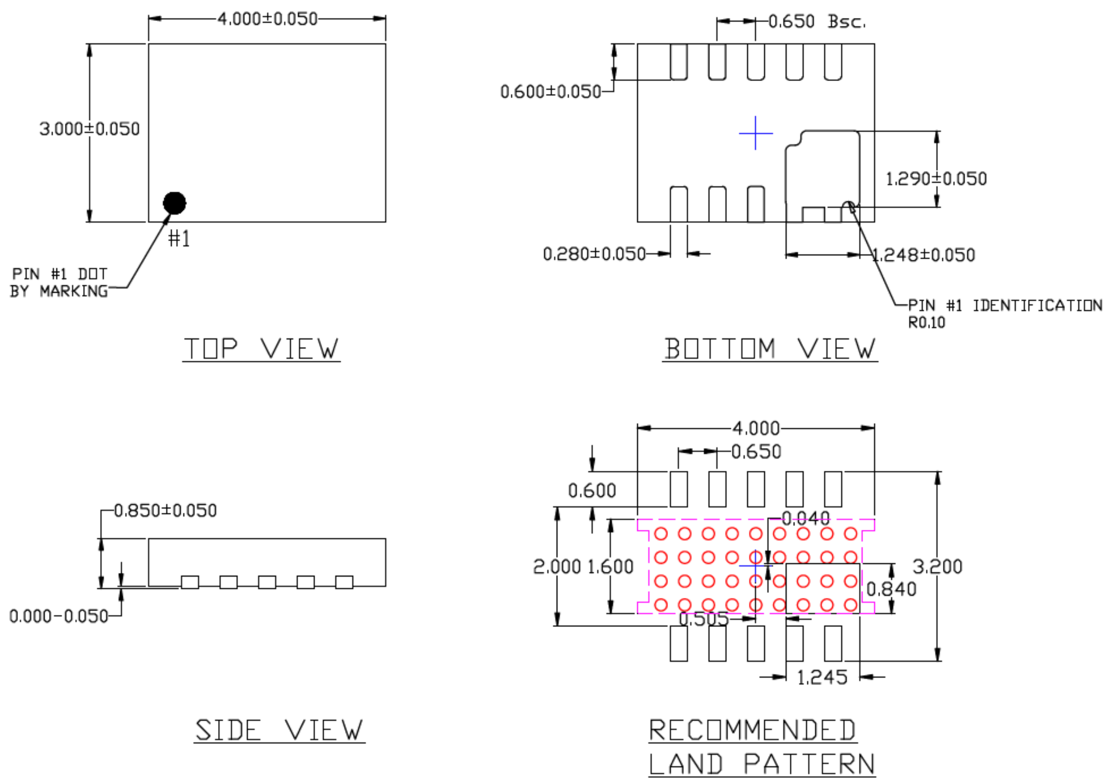
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

10-Lead FDFN 3 mm x 4 mm Package Outline and Recommended Land Pattern

TITLE
10 LEAD FDFN 3x4mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	FDFN34-10LD-PL-9	UNIT	MM



NOTE :
1. Max package warpage is 0.05mm
2. Max allowable burr is 0.076mm in all directions
3. Pin #1 will be laser marked
4. Red circle in land pattern indicate thermal via.
   Size should be 0.20mm in diameter, 0.40mm pitch
   & connected to GND for max thermal performance.
5. Purple hidden lines are recommended metal trace/
   GND planes for improved thermal performance.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (March 2021)

- Converted Micrel document MIC4950 to Microchip data sheet template DS20006514A.
- Minor grammatical text changes throughout.
- Removed all reference to the ML, SOIC-8 version of the device.
- Evaluation Board Schematic, BOM, and PCB Layout sections from original data sheet moved to the part's Evaluation Board User's Guide.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	MIC4950:		Hyper Speed Control® 5A Buck Regulator
Junction Temperature Range:	Y	=	–40°C to +125°C, RoHS-Compliant
Package:	FL	=	10-Lead 3 mm x 4 mm FDFN
Media Type:	T5 TR	= =	500/Reel 5,000/Reel

Examples:

a) MIC4950YFL-T5: MIC4950, –40°C to +125°C Temperature Range, 10-Lead FDFN, 500/Reel

b) MIC4950YFL-TR: MIC4950, –40°C to +125°C Temperature Range, 10-Lead FDFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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