MIC24046

Pin-Programmable, 19V Input, 5A Step-Down Converter

Features

- 4.5V to 19V Input Voltage Range
- 2.5V to 19V Power Stage Input Voltage Range with VDDA Externally Applied
- 5A (Maximum) Output Current
- High Efficiency (>90%)
- Pin-Selectable Output Voltages:
  - 0.7V, 0.8V, 0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V
- ±1% Output Voltage Accuracy
- Supports Safe Start-Up with Pre-Biased Output
- Pin-Selectable Current Limit and Switching Frequency
- Internal Soft-Start and Thermal Shutdown Protection
- Hiccup-Mode Short-Circuit Protection
- Available in a 20-lead 3 mm × 3 mm VQFN Package
- –40°C to +125°C Junction Temperature Range

Applications

- Servers, Data Storage, Routers, and Base Stations
- FPGAs, DSP, and Low-Voltage ASIC Power

General Description

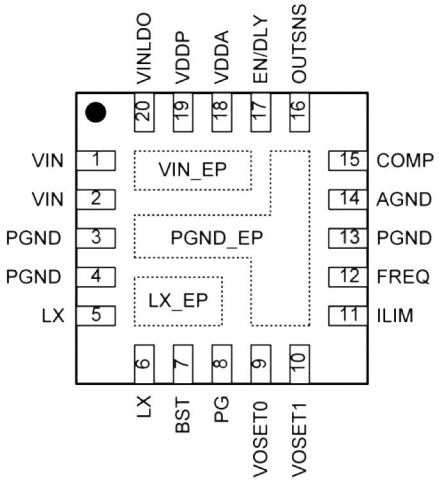
The MIC24046 is a pin-programmable, high-efficiency, wide input range, 5A synchronous step-down regulator. The MIC24046 is perfectly suited for multiple-voltage rail application environments typically found in computing and telecommunication systems.

It can be programmed by pin strapping various parameters, such as output voltage, switching frequency, and current-limit values. The pin-selectable switching frequency, valley-current mode control technique, high-performance error amplifier, and external compensation allow for the best trade-offs between high efficiency and the smallest possible solution size.

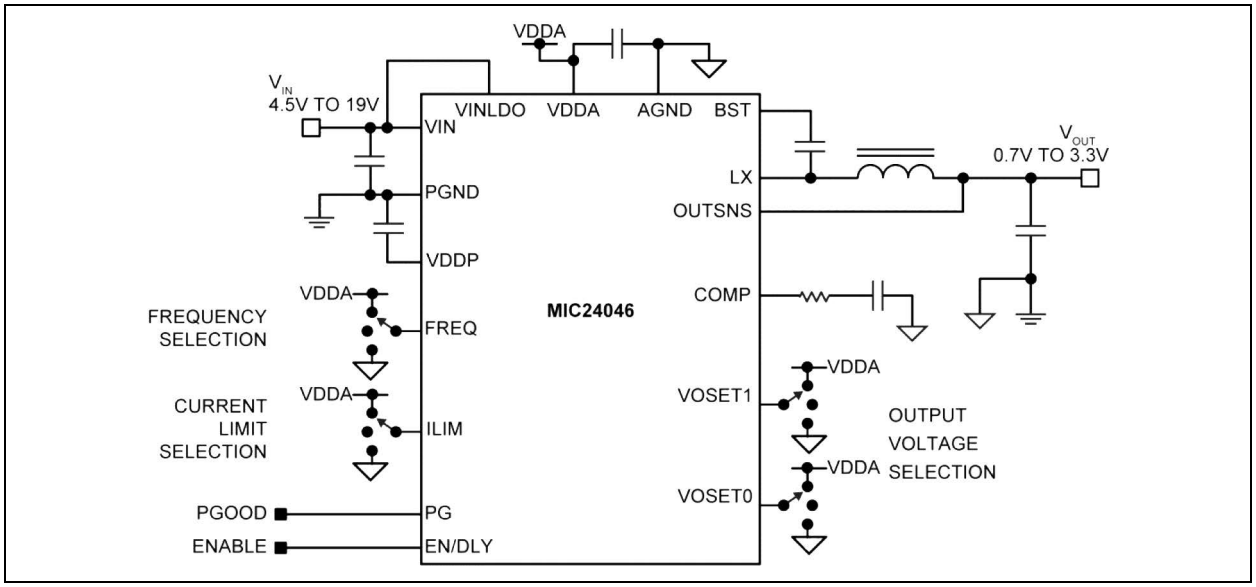
The MIC24046 is available in a thermally efficient, space-saving, 20-lead 3 mm × 3 mm VQFN package with an operating junction temperature range of –40°C to +125°C.

Package Type

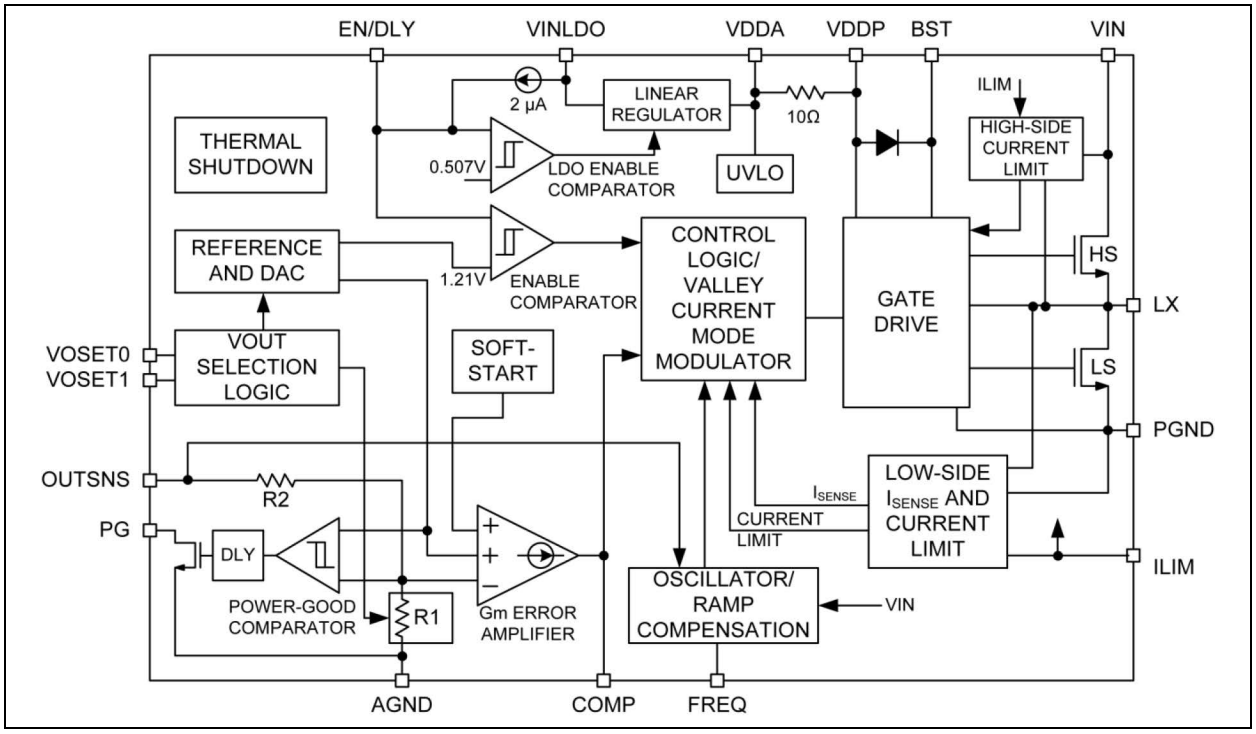
MIC24046
20-Lead 3 mm × 3 mm VQFN
(Top View)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{VIN}, V_{VINLDO} to AGND ..... −0.3V to +20V
V_{VDDP}, V_{VDDA} to AGND ..... −0.3V to +6V
V_{VINLDO} to V_{VDDA} ..... −0.3V to +20V
V_{VDDP} to V_{VDDA} ..... −0.3V to +0.3V
V_{VOSETx}, V_{FREQ}, V_{ILIM}, to AGND ..... −0.3V to +6V
V_{BST} to V_{LX} ..... −0.3V to +6V
V_{BST} to AGND ..... −0.3V to +26V
$V_{EN/DLY}$ to AGND ..... −0.3V to V_{VDDA} + 0.3V, +6V
V_{PG} to AGND ..... −0.3V to +6V
V_{COMP}, V_{OUTSNS} to AGND ..... −0.3V to V_{VDDA} + 0.3V, +6V
AGND to PGND ..... −0.3V to +0.3V
ESD Rating (Note 1)
HBM ..... 2 kV
MM 150V

Operating Ratings ‡

Supply Voltage (V_{VINLDO}) ..... 4.5V to 19V
Power Stage Supply Voltage (V_{VIN}) (Note 2) ..... 2.5V to 19V
Externally Applied Analog and Drivers Supply Voltage (V_{VINLDO} = V_{VDDA} = V_{VDDP}) ..... 4.5V to 5.5V
Enable Voltage ($V_{EN/DLY}$) ..... 0V to V_{VDDA}
Power-Good (PG) Pull-up Voltage (V_{PU_PG}) ..... 0V to 5.5V
Output Current 5A

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

2: When VDDA is externally supplied.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, $V_{IN} = V_{INLDO}$ = 12V; C_{VDDA} = 2.2 µF, C_{VDDP} = 2.2 µF, T_A = +25°C. **Bold** values valid for –40°C ≤ T_J ≤ +125°C. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
V_{IN} Supply						
Input Range	V_{INLDO}	**4.5**	—	**19**	V	—
	V_{IN}	**2.5**	—	**19**	V	VDDA = V_{INLDO} = 5V, externally applied
Disable Current	I_{VINQ}	—	0.2	**2**	µA	EN/DLY = 0V
	$I_{VINLDOQ}$	—	35	42	µA	EN/DLY = 0V, $T_A = T_J$ = 25°C
		—	—	**56**	µA	EN/DLY = 0V, −40°C ≤ T_J ≤ +125°C
Operating Current	I_{VINOp}	—	0.45	0.75	mA	EN/DLY > 1.28V, V_{OUTSNS} = 1.15 × $V_{OUT(NOM)}$, no switching, $T_A = T_J$ = 25°C
	$I_{VINLDOOp}$	—	5.6	7	mA	EN/DLY > 1.28V, V_{OUTSNS} = 1.15 × $V_{OUT(NOM)}$, no switching, $T_A = T_J$ = 25°C
VDDA 5V Supply						
Operating Voltage	VDDA	**4.8**	5.1	**5.4**	V	EN/DLY > 0.58V, $I_{(VDDA)}$ = 0 mA to 10 mA
Dropout Operation		**3.6**	3.75	—	V	V_{INLDO} = 4.5V, EN/DLY > 0.58V, $I_{(VDDA)}$ = 10 mA
VDDA Undervoltage Lockout						
VDDA UVLO Rising	UVLO_R	**3.1**	3.5	**3.9**	V	VDDA Rising, EN/DLY > 1.28V
VDDA UVLO Falling	UVLO_F	**2.87**	3.2	**3.45**	V	VDDA Falling, EN/DLY > 1.28V
VDDA UVLO Hysteresis	UVLO_H	—	300	—	mV	—
EN/DLY Control						
LDO Enable Threshold	EN_LDO_R	—	507	**580**	mV	Turns On VDDA LDO
LDO Disable Threshold	EN_LDO_F	**460**	491	—	mV	Turns Off VDDA LDO
LDO Threshold Hysteresis	EN_LDO_H	—	16	—	mV	—
EN/DLY Rising Threshold	EN_R	**1.14**	1.21	**1.28**	V	Initiates power-stage operation
EN/DLY Falling Threshold	EN_F	—	1.06	—	V	Stops power-stage operation
EN/DLY Hysteresis	EN_H	—	150	—	mV	—
EN/DLY Pull-up Current	EN_I	1	2	3	µA	$T_A = T_J$ = 25°C
Switching Frequency						
Programmable Frequency (High Z)	f_{sz}	**360**	400	**440**	kHz	FREQ = High Z (open)
Programmable Frequency 0	f_{s0}	**500**	565	**630**	kHz	FREQ = Low (GND)
Programmable Frequency 1	f_{s1}	**700**	790	**880**	kHz	FREQ = High (VDDA)

Note 1: Specification for packaged product only.

2: When VIN=2.5V to 4.5V, VDDA=VINLDO=5V needs to be applied.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, V_{IN} = V_{INLDO} = 12V; C_{VDDA} = 2.2 µF, C_{VDDP} = 2.2 µF, T_A = +25°C. **Bold** values valid for –40°C ≤ T_J ≤ +125°C. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Overcurrent Protection						
HS Current Limit 0	I_{LIM_HS0}	**6.0**	7.1	**8.1**	A	I_{LIM} = Low (GND)
HS Current Limit 1	I_{LIM_HS1}	**8.1**	9.3	**10.3**	A	I_{LIM} = High (VDDA)
HS Current Limit Z	I_{LIM_HSZ}	**9.3**	10.5	**11.9**	A	I_{LIM} = High Z (Open)
Top FET Current-Limit Leading Edge-Blanking Time	LEB	—	108	—	ns	—
LS Current Limit 0	I_{LIM_LS0}	**3.0**	4.6	**6.3**	A	I_{LIM} = Low (GND)
LS Current Limit 1	I_{LIM_LS1}	**4.0**	6.2	**7.9**	A	I_{LIM} = High (VDDA)
LS Current Limit Z	I_{LIM_LSZ}	**5.0**	6.8	**8.6**	A	I_{LIM} = High Z (Open)
OC Events Count for Hiccup	IN_{HICC_DE}	—	15	—	Clock Cycles	Number of subsequent cycles in current limit before entering hiccup overload protection.
Hiccup Wait Time	t_{HICC_WAIT}	—	3 × Soft-Start Time	—	—	Duration of the High-Z state on LX before new soft-start.
Power Switches						
Bottom FET ON resistance	R_{BOTTOM}	—	16	21	mΩ	V_{IN} = V_{INLDO} = VDDP = VDDA = 5V, V_{BST} – V_{LX} = 5V, T_A = T_J = 25°C
Top FET ON resistance	R_{TOP}	—	38	50	mΩ	V_{IN} = V_{INLDO} = VDDP = VDDA = 5V, V_{BST} – V_{LX} = 5V, T_A = T_J = 25°C
Pulse-Width Modulation (PWM)						
Minimum LX ON Time	$t_{ON(MIN)}$	—	26	—	ns	T_A = T_J = 25°C
Minimum LX OFF time	$t_{OFF(MIN)}$	90	135	190	ns	V_{IN} = V_{INLDO} = VDDA = 5V, V_{OUTSNS} = 3V, FREQ = Open (400 kHz setting), V_{OSET0} = V_{OSET1} = GND (3.3V setting), T_A = T_J = 25°C
Minimum Duty Cycle	D_{MIN}	—	0	—	%	V_{OUTSNS} > 1.1 × $V_{OUT(NOM)}$
g_m Error Amplifier						
Error-Amplifier Transconductance	gm_{EA}	—	1.5	—	mmho	—
Error-Amplifier DC Gain	A_{EA}	—	50000	—	V/V	—
Error-Amplifier Source/Sink Current	I_{SR_SNK}	−400	—	+400	µA	—
COMP Output Swing High	COMP_H	—	2.4	—	V	—
COMP Output Swing Low	COMP_L	—	0.8	—	V	—
COMP-to-Inductor Current Transconductance	gm_{PS}	—	12.5	—	A/V	V_{OUT} = 1.2V, I_{OUT} = 4A

Note 1: Specification for packaged product only.

2: When VIN=2.5V to 4.5V, VDDA=VINLDO=5V needs to be applied.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, $V_{IN} = V_{INLDO} = 12V$; $C_{VDDA} = 2.2\ \mu F$, $C_{VDDP} = 2.2\ \mu F$, $T_A = +25°C$. **Bold** values valid for $-40°C \le T_J \le +125°C$. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Output Voltage DC Accuracy						
Output Voltage Accuracy for Ranges 1 and 2	OutErr12	**−1**	—	**1**	%	$2.5V \le V_{IN} \le 19V$, V_{OUT} = 0.7V to 1.8V, $T_A = T_J = -40°C$ to 125°C, I_{OUT} = 0A (Note 2)
Output Voltage Accuracy for Range 3	OutErr3	**−1.5**	—	**1.5**	%	$4.75V \le V_{IN} \le 19V$, V_{OUT} = 2.49V to 3.3V, $T_A = T_J = -40°C$ to 125°C, I_{OUT} = 0A
Load Regulation	LoadReg	—	0.25	—	%	I_{OUT} = 0A to 5A
Line Regulation	LineReg	—	0.1	—	%	$6V < V_{IN} < 19V$, I_{OUT} = 2A
Internal Soft-Start						
Reference Soft-Start Slew Rate 0	SS_SR	—	0.45	—	V/ms	V_{OUT} = 0.7V, 0.8V, 0.9V, 1.0V, 1.2V
Power Good (PG)						
PG Low Voltage	PG_V_{OL}	—	0.18	**0.4**	V	$I_{(PG)}$ = 4 mA
PG Leakage Current	PG_I_{LEAK}	**−1**	0.02	**1**	µA	V_{PG} = 5V
PG Rise Threshold	PG_R	**90**	92.5	**95**	%	V_{OUT} Rising
PG Fall Threshold	PG_F	**87.5**	90	**92.5**	%	V_{OUT} Falling
PG Rise Delay	PG_R_DLY	—	0.45	—	ms	V_{OUT} Rising
PG Fall Delay	PG_F_DLY	—	70	—	µs	V_{OUT} Falling
Thermal Shutdown						
Thermal Shutdown	T_{SHDN}	—	160	—	°C	—
Thermal-Shutdown Hysteresis	T_{SHDN_HYST}	—	25	—	°C	—
Efficiency						
Efficiency	η	—	82.3	—	%	V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 2A, $f_S = f_{SZ}$ = 400 kHz, L = 1.2 µH, T_A = 25°C

Note 1: Specification for packaged product only.

2: When VIN=2.5V to 4.5V, VDDA=VINLDO=5V needs to be applied.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature	T_J	−40	—	+125	°C	—
Storage Temperature Range	T_A	−65	—	+150	°C	—
Lead Temperature	—	—	260	—	°C	Soldering, 10 seconds
Junction to Ambient Thermal Resistances (Note 1)						
Thermal Resistance, 20-LD 3x3 VQFN	θ_{JA}	—	29	—	°C/W	—

Note 1: θ_{JA} is measured on the MIC24046 evaluation board.

2.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise noted, $V_{IN} = V_{INLDO} = 12V$; $C_{VDDA} = 2.2\ \mu F$, $C_{VDDP} = 2.2\ \mu F$, $T_A = 25°C$.

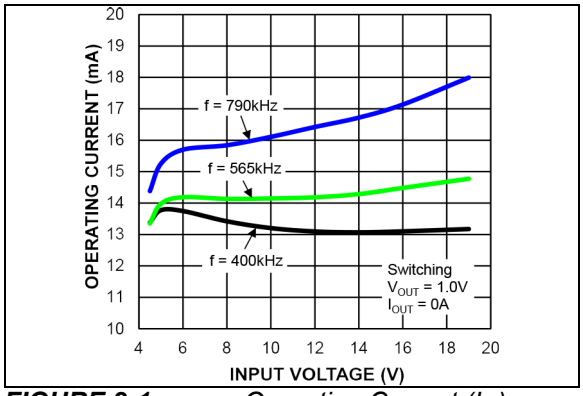


FIGURE 2-1: *Operating Current (I_Q) vs. Input Voltage.*

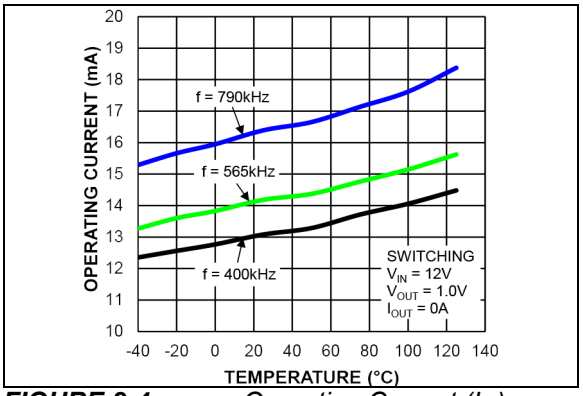


FIGURE 2-4: *Operating Current (I_Q) vs. Temperature.*

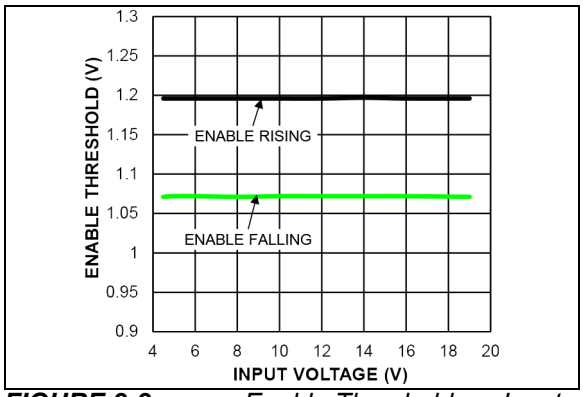


FIGURE 2-2: *Enable Threshold vs. Input Voltage.*

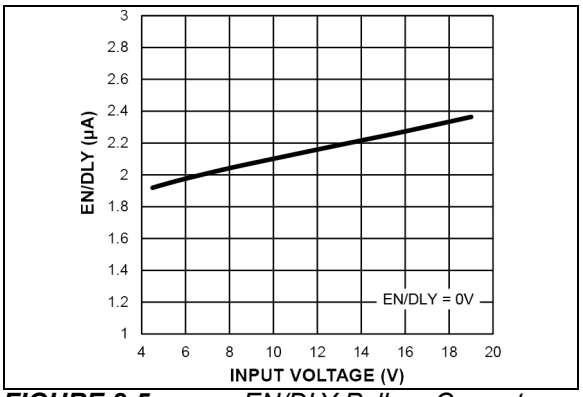


FIGURE 2-5: *EN/DLY Pull-up Current vs. Input Voltage.*

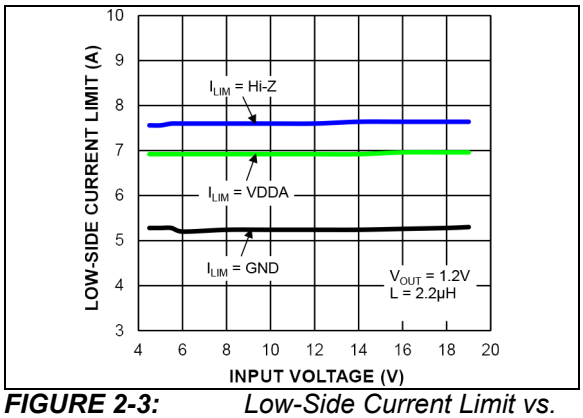


FIGURE 2-3: *Low-Side Current Limit vs. Input Voltage.*

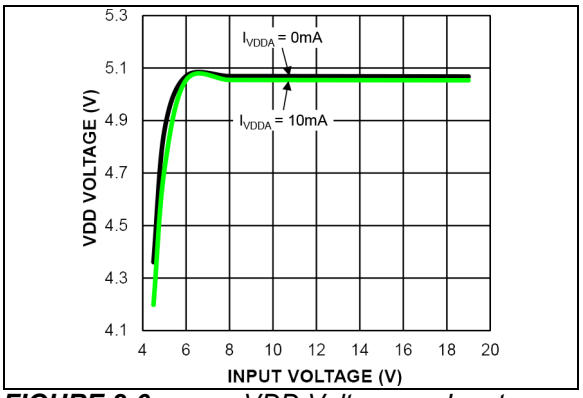


FIGURE 2-6: *VDD Voltage vs. Input Voltage.*

Note: Unless otherwise noted, $V_{IN} = V_{INLDO} = 12V$; C_{VDDA}= 2.2 µF, C_{VDDP} = 2.2 µF, T_A = 25°C.

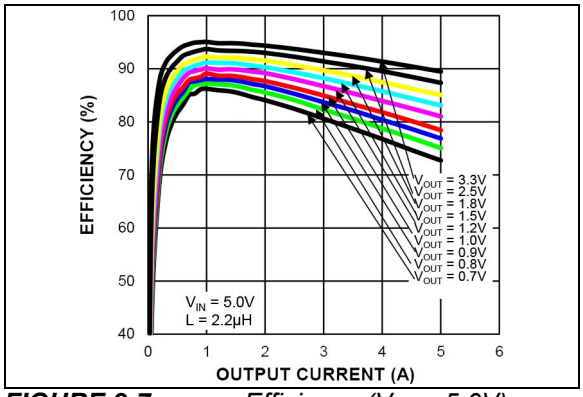


FIGURE 2-7: *Efficiency (V_{IN} = 5.0V) vs. Output Current.*

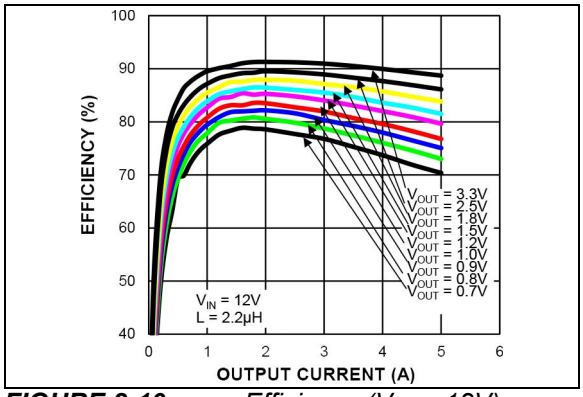


FIGURE 2-10: *Efficiency (V_{IN} = 12V) vs. Output Current.*

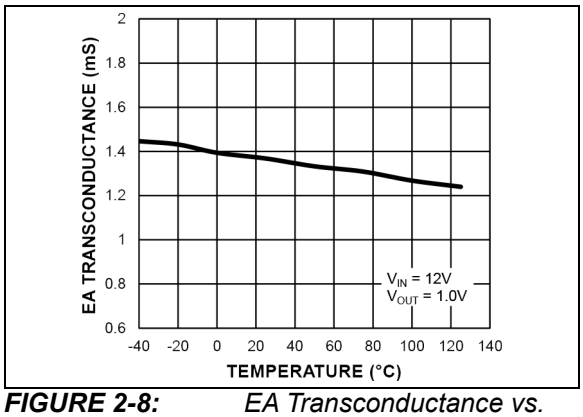


FIGURE 2-8: *EA Transconductance vs. Temperature.*

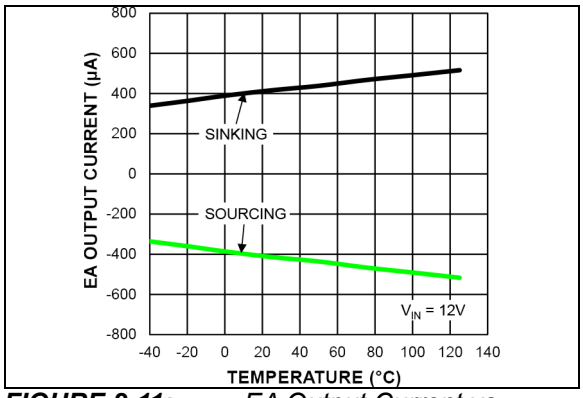


FIGURE 2-11: *EA Output Current vs. Temperature.*

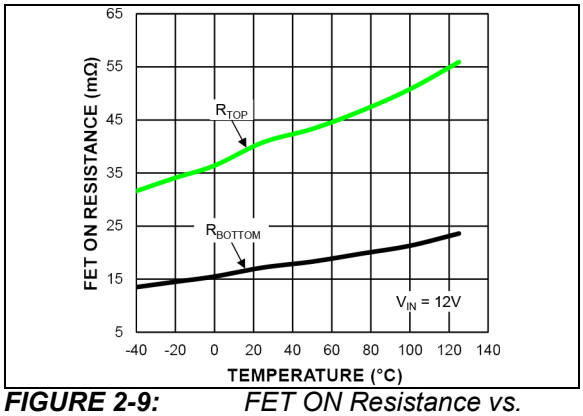


FIGURE 2-9: *FET ON Resistance vs. Temperature.*

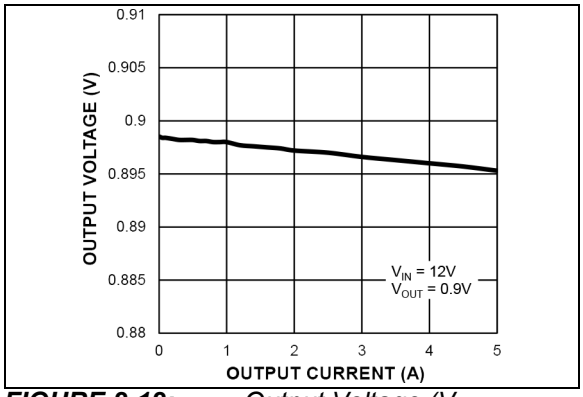


FIGURE 2-12: *Output Voltage (V_{OUT}= 0.9V) vs. Output Current.*

Note: Unless otherwise noted, $V_{IN} = V_{INLDO} = 12V$; $C_{VDDA} = 2.2\ \mu F$, $C_{VDDP} = 2.2\ \mu F$, $T_A = 25°C$.

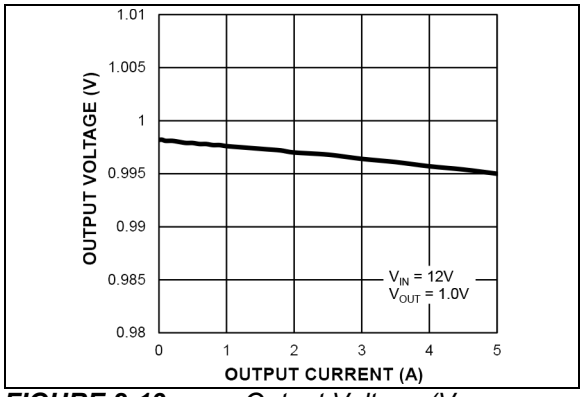


FIGURE 2-13: *Output Voltage (V_{OUT}= 1.0V) vs. Output Current.*

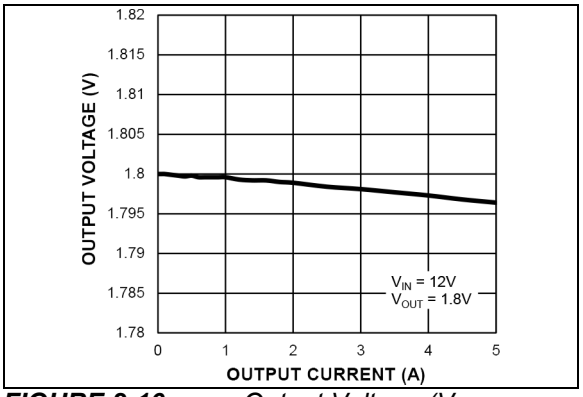


FIGURE 2-16: *Output Voltage (V_{OUT}= 1.8V) vs. Output Current.*

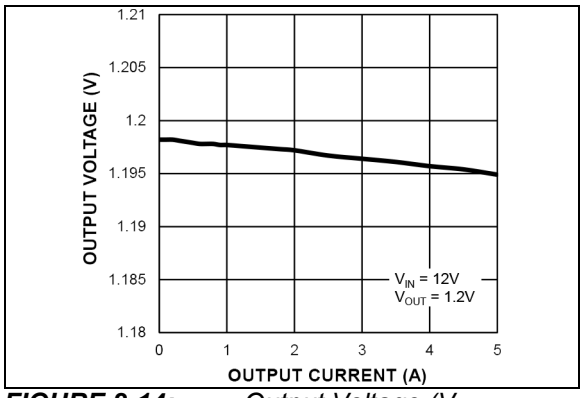


FIGURE 2-14: *Output Voltage (V_{OUT}= 1.2V) vs. Output Current.*

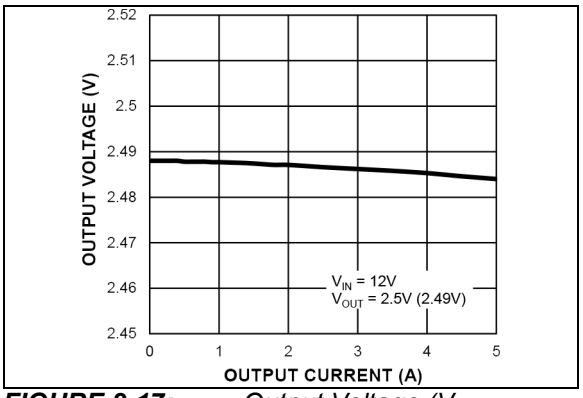


FIGURE 2-17: *Output Voltage (V_{OUT}= 2.5V) vs. Output Current.*

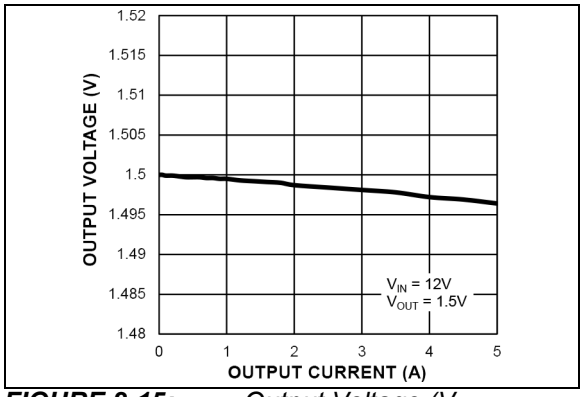


FIGURE 2-15: *Output Voltage (V_{OUT}= 1.5V) vs. Output Current.*

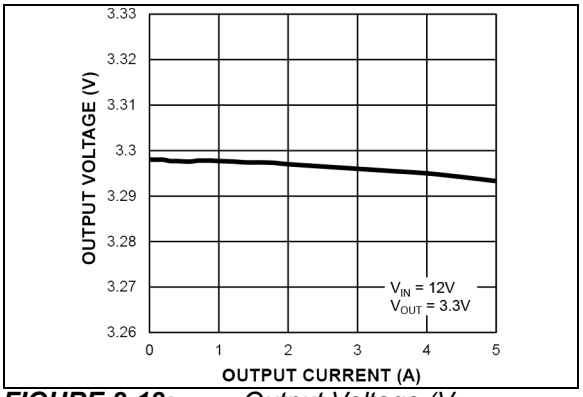


FIGURE 2-18: *Output Voltage (V_{OUT}= 3.3V) vs. Output Current.*

Note: Unless otherwise noted, $V_{IN} = V_{INLDO} = 12V$; $C_{VDDA} = 2.2\ \mu F$, $C_{VDDP} = 2.2\ \mu F$, $T_A = 25°C$.

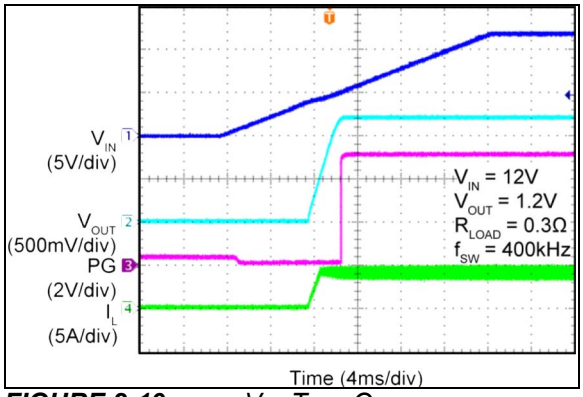


FIGURE 2-19: *V_{IN} Turn-On.*

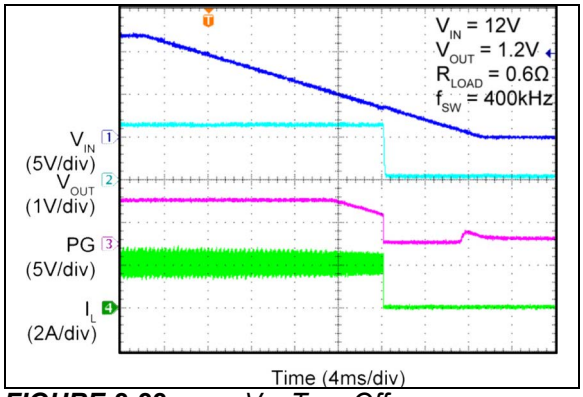


FIGURE 2-22: *V_{IN} Turn-Off.*

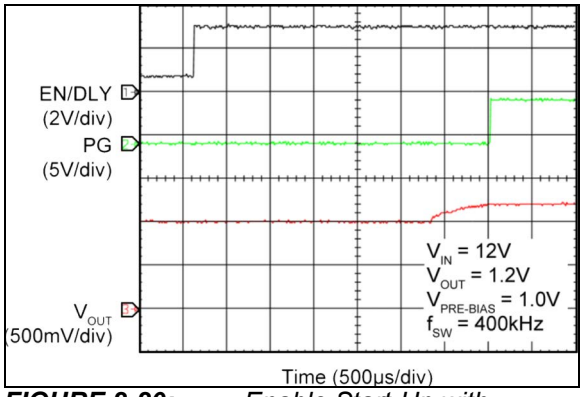


FIGURE 2-20: *Enable Start-Up with Pre-Biased Output.*

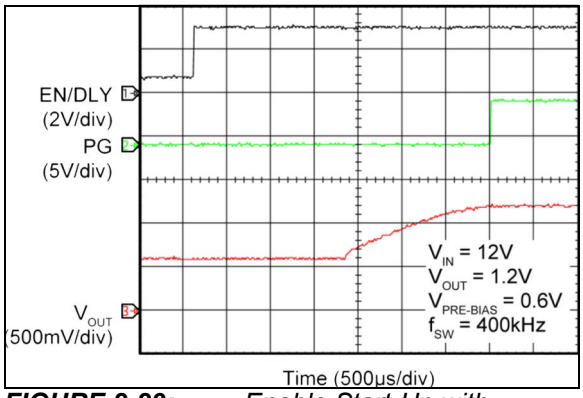


FIGURE 2-23: *Enable Start-Up with Pre-Biased Output.*

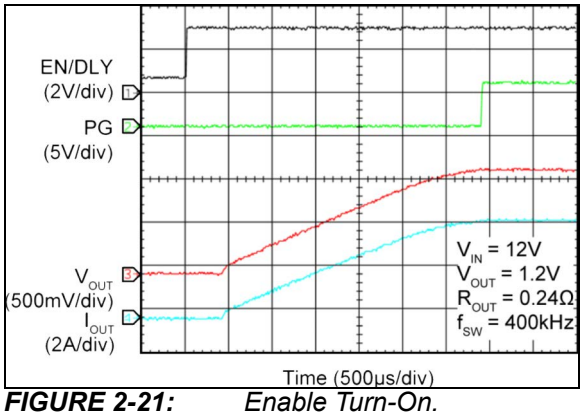


FIGURE 2-21: *Enable Turn-On.*

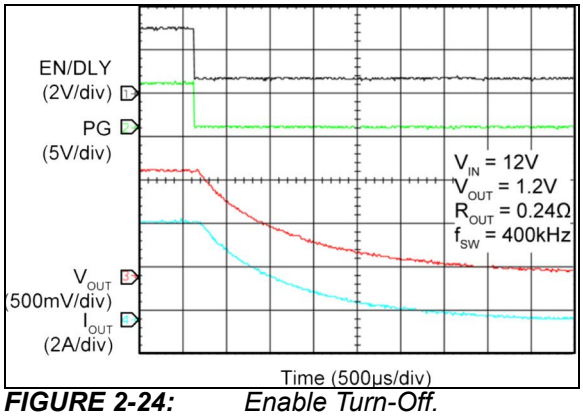


FIGURE 2-24: *Enable Turn-Off.*

Note: Unless otherwise noted, V_{IN} = V_{INLDO} = 12V; C_{VDDA}= 2.2 µF, C_{VDDP} = 2.2 µF, T_A = 25°C.

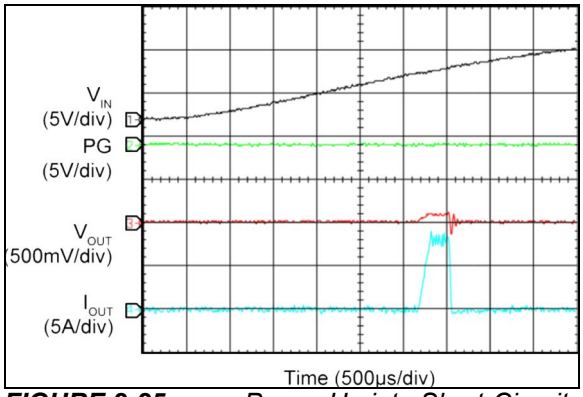


FIGURE 2-25: *Power-Up into Short-Circuit.*

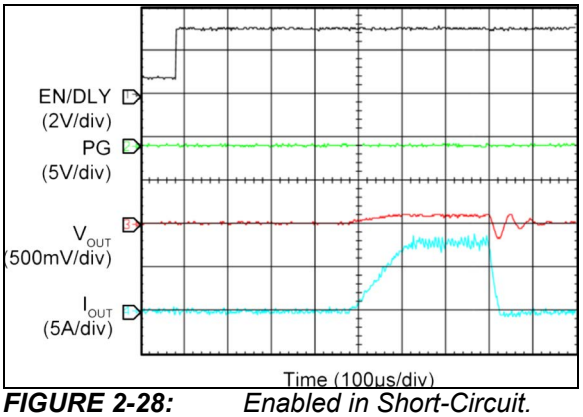


FIGURE 2-28: *Enabled in Short-Circuit.*

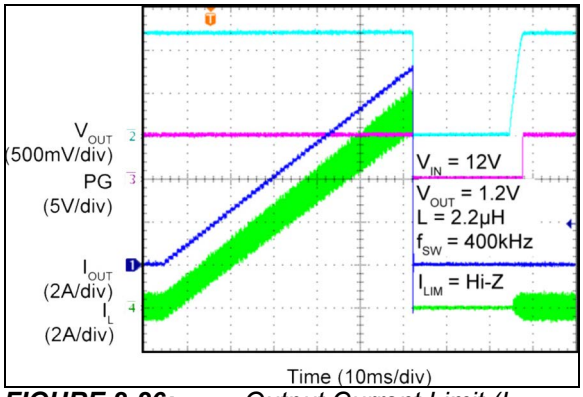


FIGURE 2-26: *Output Current Limit (I_{LIM} = Hi-Z).*

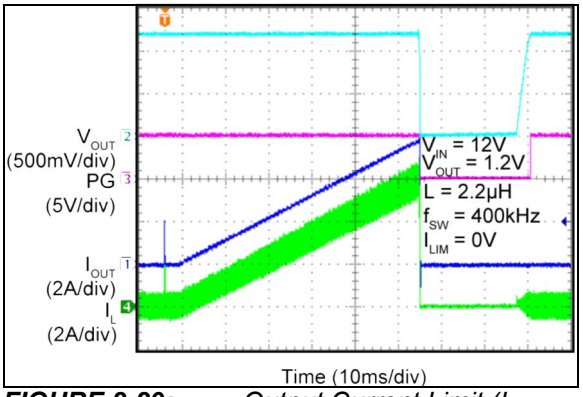


FIGURE 2-29: *Output Current Limit (I_{LIM} = 0V).*

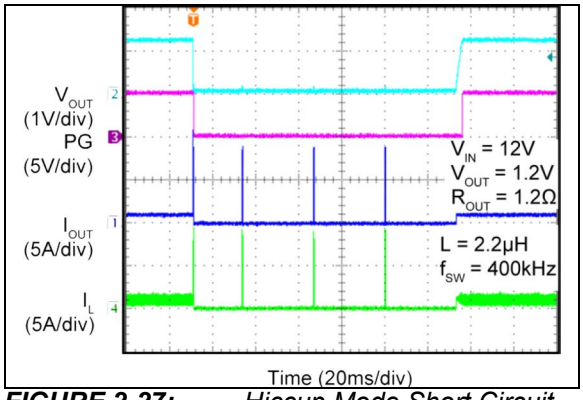


FIGURE 2-27: *Hiccup Mode Short Circuit and Output Recovery.*

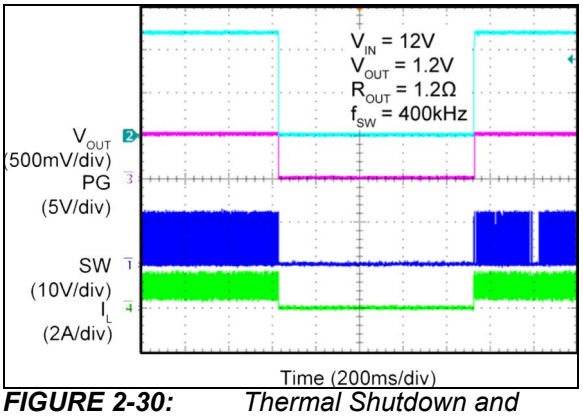


FIGURE 2-30: *Thermal Shutdown and Thermal Recovery.*

Note: Unless otherwise noted, $V_{IN} = V_{INLDO} = 12V$; $C_{VDDA} = 2.2\ \mu F$, $C_{VDDP} = 2.2\ \mu F$, $T_A = 25°C$.

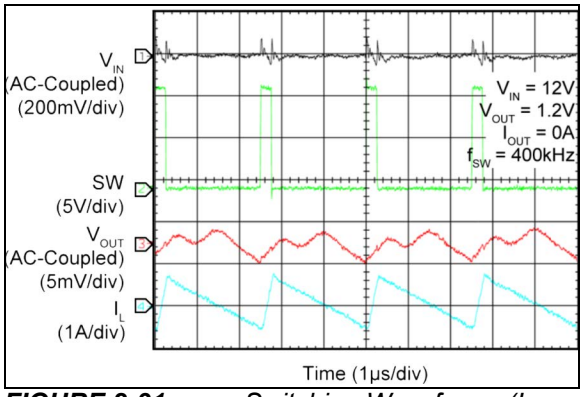


FIGURE 2-31: *Switching Waveforms (I_{OUT} = 0A).*

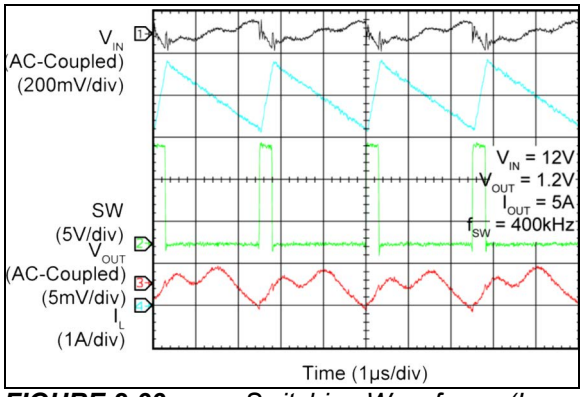


FIGURE 2-33: *Switching Waveforms (I_{OUT} = 5A).*

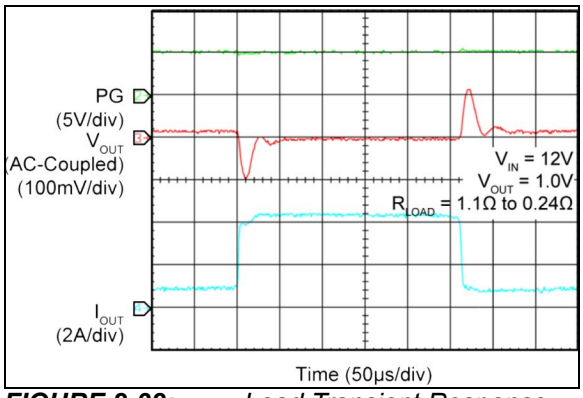


FIGURE 2-32: *Load Transient Response.*

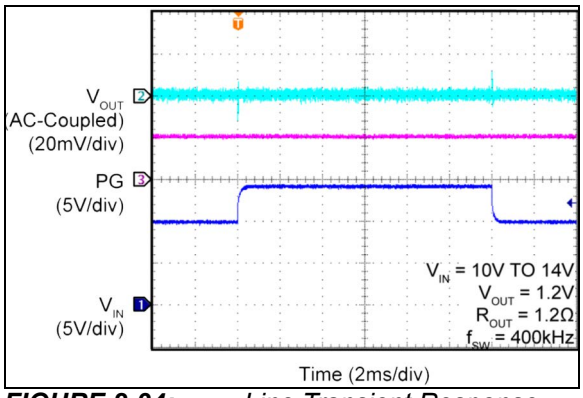


FIGURE 2-34: *Line Transient Response.*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2	VIN	Input Voltage for the Buck Converter Power Stage: These pins are the drain terminal of the internal high-side N-channel MOSFET. A 10 µF minimum ceramic capacitor should be connected from VIN to PGND as close as possible to the device. A combination of multiple ceramic capacitors of different sizes is recommended.
3, 4, 13	PGND	Low-Side MOSFET Source Terminal and Low-Side Driver Return: Connect the ceramic input capacitors to PGND as close as possible to the device.
5, 6	LX	Switch Node: Drain (low-side MOSFET) and source (high-side MOSFET) connection of the internal power N-channel FETs. The external inductor (switched side) and bootstrap capacitor (bottom terminal) must be connected to these pins.
7	BST	Bootstrap: Supply voltage for the driver of the high-side N-channel power MOSFET. Connect the bootstrap capacitor (top terminal) to this pin.
8	PG	Power Good (Output): When the output voltage is within 92.5% of the nominal set point, this pin will go from logic low to logic high through an external pull-up resistor. This pin is the drain connection of an internal N-channel FET.
9	VOSET0	Three-state Pin (Low, High, and High-Z) for Output Voltage Programming: Together with VOSET1, VOSET0 defines nine logic values corresponding to nine output voltage selections.
10	VOSET1	Three-State Pin (Low, High, and High-Z) for Output Voltage Programming: Together with VOSET0, VOSET1 defines nine logic values corresponding to nine output voltage selections.
11	ILIM	Three-State (Low, High, and High-Z) Current-Limit Selection Pin.
12	FREQ	Three-State (Low, High, and High-Z) Switching Frequency Selection Pin.
14	AGND	Analog Ground: Quiet ground for the analog circuitry of the internal regulator and return terminal for the external compensation network.
15	COMP	Transconductance Error Amplifier Output: Connect a compensation network from this pin to AGND.
16	OUTSNS	Output Sensing: Connect this pin directly to the buck converter output voltage. This pin is the top side terminal of the internal feedback divider.
17	EN/DLY	Precision Enable/Turn-On Delay Input. The EN/DLY pin is first compared against a 507 mV threshold to turn-on the on-board LDO regulator. The EN/DLY pin is then compared against a 1.21V (typical) threshold to initiate output power delivery. A 150 mV typical hysteresis prevents chattering when power delivery is started. A 2 µA (typical) current source pulls up the EN/DLY pin. Turn-on delay can be achieved by connecting a capacitor from EN/DLY to ground, while using an open-drain output to drive the EN/DLY pin.
18	VDDA	Output of the internal linear regulator and internal supply for analog control. A 1µF minimum ceramic capacitor should be connected from this pin to AGND; 2.2 µF nominal value recommended.
19	VDDP	Internal Supply Rail for the MOSFET Drivers (fed by the VDDA pin): An internal resistor (10Ω) between pins VDDP and VDDA is provided in the regulator in order to implement an RC filter for switching noise suppression. A 1 µF minimum ceramic capacitor should be connected from this pin to PGND; 2.2 µF nominal value recommended.
20	VINLDO	Input of the Internal Linear Regulator: This pin is typically connected to the input voltage of the buck converter stage (VIN). If VINLDO and VIN are connected to different voltage rails, individually bypass VINLDO to ground with a 100 nF ceramic capacitor.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
PGND_EP	PGND	PGND Exposed Pad: Electrically connected to PGND pins. Connect with thermal vias to the ground plane to ensure adequate heat-sinking.
VIN_EP	VIN	VIN Exposed Pad: Electrically connected to VIN pins. If an input power distribution plane is available, connect with thermal vias to that plane to improve heat-sinking.
LX_EP	LX	LX Exposed Pad: Electrically connected to LX pins.

4.0 FUNCTIONAL DESCRIPTION

The MIC24046 is a pin-programmable, 5A valley current-mode controlled regulator featuring an input voltage range from 4.5V to 19V.

The MIC24046 requires a minimal amount of external components. Only the inductor, supply decoupling capacitors, and compensation network are external. The flexibility in the external compensation design allows the user to optimize their design across the entire input voltage and selectable output voltages range.

4.1 Theory of Operation

Valley-current-mode control is a fixed-frequency, leading-edge modulated PWM current-mode control. Differing from the peak-current-mode, the valley-current-mode clock marks the turn-off of the high-side switch. Upon this instant, the MIC24046 low-side switch current level is compared against the reference current signal from the error amplifier. When the falling low-side switch current signal drops below the current reference signal, the high side switch is turned on. As a result, the inductor valley current is regulated to a level dictated by the output of the error amplifier.

As shown in the Compensation Design section, the feedback loop includes an internal programmable reference (REF_{DAC}) and output voltage sensing attenuator (R2/R1), which removes the need for external feedback components and improves regulation accuracy. Output voltage feedback is achieved by connecting OUTSNS directly to the output. The high-performance transconductance error amplifier drives an external compensation network at the COMP pin. The COMP pin voltage represents the reference current signal. The COMP pin voltage is fed to the valley-current-mode modulator, which also adds slope compensation to guarantee current-loop stability. Valley-current-mode control requires slope compensation at duty cycles less than 50% for current-loop stability. The slope compensation circuit is internal, and it is automatically adapted in amplitude depending upon the frequency, output voltage range, and voltage differential ($V_{IN} - V_{OUTSNS}$). The internal low-$R_{DS(ON)}$ power MOSFETs, associated adaptive gate driver, and internal bootstrap diode complete the power train.

Overcurrent protection and thermal shutdown protect the MIC24046 from faults or abnormal operating conditions.

4.2 Internal LDO, Supply Rails (VIN, VINLDO, VDDA, VDDP)

VIN represents the power train input. These pins are the drain connection of the internal high-side MOSFET and should be bypassed to GND with an X5R or X7R 10 µF (minimum) ceramic capacitor, placed as close as possible to the IC. A combination of ceramic capacitors of different sizes is recommended.

An internal LDO (input = VINLDO) provides a clean voltage supply (5.1V, typical) for the analog circuits at pin VDDA. The internal LDO is typically powered from the same power rail feed as VIN; however, VINLDO can also be higher or lower than VIN, and can be connected to any other voltage within its recommended limits. VINLDO and VDDA should be locally bypassed (see the Pin Description section). A small series resistor (typically 2Ω-10Ω) can be used in combination with the VINLDO bypass capacitor to implement a RC filter for suppression of large high-frequency switching noise.

The internal LDO is enabled when the voltage at the EN/DLY pin exceeds about 0.51V, and regulation takes place as soon as enough voltage has established between the VINLDO and VDDA pins. If an external 5V±10% is available, it is possible to bypass the internal LDO by connecting VINLDO, VDDA and VDDP together at the external 5V rail, thus improving overall efficiency. An internal undervoltage lock-out circuit (UVLO) monitors the level of VDDA.

VDDP is the power supply rail for the gate drivers and bootstrap circuit. This pin is subject to high-current spike with high-frequency content. To prevent these from polluting the analog VDDA supply, a separate capacitor is needed for VDDP pin bypassing.

An internal 10Ω resistor is provided between VDDA and VDDP allowing a switching noise attenuation RC filter with the minimum amount of external components to be implemented. It is possible—although typically not necessary—to lower the RC time constant by connecting an external resistor between VDDA and VDDP.

4.3 Pin-strapping Programmability (VOSET0, VOSET1, FREQ, ILIM)

The MIC24046 uses pin-strapping to set the output voltage (pins VOSET0, VOSET1), switching frequency (pin FREQ), and current limit (pin ILIM). No external passives are needed, such that external component count is minimized. Each pin is a three-state input (connect to GND for LOW logic level, connect to VDDA for HIGH logic level or leave unconnected for high-Z). The logic level of the pins is read and frozen in the internal configuration logic immediately after the VDDA rail has come up and stabilized. After this instant, any change of the input logic level on the pins will have no effect until the VDDA power is cycled again. The values corresponding to each particular pin-strapping configuration are detailed in the Application Information section.

4.4 Enable/Delay (EN/DLY)

EN/DLY is a dual-threshold pin that turns the internal LDO on and off, and starts/stops the power delivery to the output. This is shown in Figure 4-1:

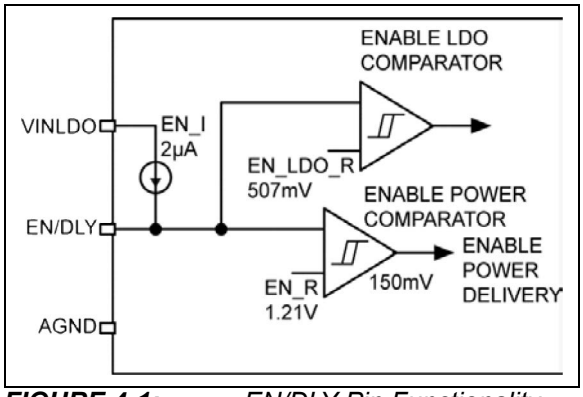


FIGURE 4-1: *EN/DLY Pin Functionality.*

The threshold for power delivery (EN_R) is a precise 1.21V ±70 mV. A 150 mV typical hysteresis prevents chattering due to switching noise and/or slow edges.

A 2 µA typical pull-up current with ±1 µA accuracy permits the implementation of a start-up delay by means of an external capacitor. In this case, it is necessary to use an open-drain driver to disable the MIC24046 while maintaining the start-up delay function.

4.5 Power-Good (PG)

PG is an open-drain output that requires an external pull-up resistor to a pull-up voltage (V_{PU_PG}) less than 5.5V for being asserted to a logic HIGH level. PG is asserted with a typical delay of 0.45 ms when the output voltage (OUTSNS) reaches 92.5% of its target regulation voltage. PG is de-asserted with a typical delay of 70 µs when the output voltage falls below 90% of its target regulation voltage. The PG falling delay acts as a de-glitch timer against very short spikes. The PG output is always immediately de-asserted when the EN/DLY pin is below the power delivery enable threshold (EN_R/EN_F). The pull-up resistor should be large enough to limit the PG pin current to below 2 mA.

4.6 Inductor (LX) and Bootstrap (BST)

The external inductor is connected to LX. The high-side MOSFET driver circuit is powered between BST and LX by means of an external capacitor (typically 100 nF) that is replenished from rail VDDP during the low-side MOSFET ON-time. The bootstrap diode is internal.

4.7 Output Sensing (OUTSNS) and Compensation (COMP)

OUTSNS should be connected exactly to the desired point-of-load regulation avoiding parasitic resistive drops. The impedance seen into OUTSNS is high (tens of kΩ or more, depending on the selected output voltage value), therefore its loading effect is typically negligible. OUTSNS is also used by the slope compensation generator.

COMP is the connection for the external compensation network. COMP is driven by the output of the transconductance error amplifier. Care must be taken to return the compensation network ground directly to AGND.

4.8 Soft-Start

The MIC24046 internal reference is ramped up at a 0.45V/ms rate. Note that this is the internal reference soft-start slew rate and that the actual slew rate seen at the output should take into account the internal divider attenuation as detailed in the Application Information section.

4.9 Switching Frequency (FREQ)

The MIC24046 features three different selectable switching frequencies: 400 kHz, 565 kHz, and 790 kHz.

4.10 Pre-Biased Output Start-Up

The MIC24046 is designed to achieve safe start-up into a pre-biased output without discharging the output capacitors.

4.11 Thermal Shutdown

The MIC24046 has thermal-shutdown protection that prevents operation at excessive temperature. The thermal-shutdown threshold is typically set at 160°C with a hysteresis of 25°C.

4.12 Overcurrent Protection (I_{LIM}) and Hiccup Mode Short-Circuit Protection

The MIC24046 features instantaneous cycle-by-cycle current limit with current sensing on both low-side and high-side switches. It also offers a hiccup mode for prolonged overloads or short-circuit conditions.

Low-side cycle-by-cycle protection detects the current level of the inductor current during the low-side MOSFET ON time. The high-side MOSFET turn-on is inhibited as long as the low-side MOSFET current limit is above the current-limit threshold level.

The inductor current will continue decaying until the current falls below the threshold, where the high-side MOSFET will be enabled again according to the duty cycle requirement from the PWM modulator. The mechanism is illustrated in Figure 4-2.

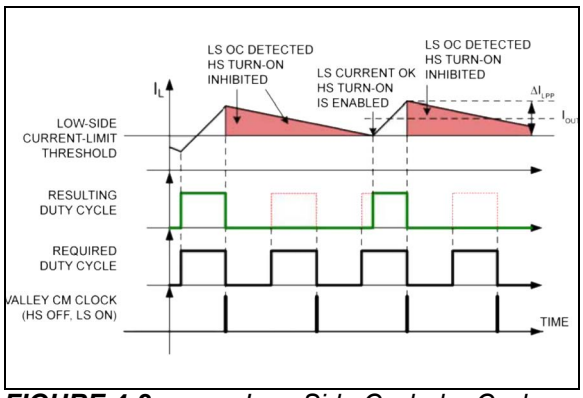


FIGURE 4-2: *Low-Side Cycle-by-Cycle Current-Limit Action.*

The low-side current limit has three different programmable levels (for 3A, 4A, and 5A loads), in order to fit different application requirements. Since the low-side current limit acts on the valley current, the DC output current level (I_{OUT}) where the low-side cycle-by-cycle current limit is engaged will be higher than the current limit value by an amount equal to $\Delta IL_{PP}/2$, where ΔIL_{PP} is the peak-to-peak inductor ripple current.

The high-side current limit is approximately 1.4 to 1.5 times greater than the low-side current limit (typical values). The high-side cycle-by-cycle current limit immediately truncates the high-side ON time without waiting for the OFF clocking event.

A leading edge blanking (LEB) timer (108 ns, typical) is provided on the high-side cycle-by-cycle current limit to mask the switching noise and to prevent falsely triggering the protection. High-side cycle-by-cycle current limit action cannot take place before the LEB timer expires.

Hiccup mode protection reduces power dissipation in permanent short-circuit conditions. On each clock cycle where a low-side cycle-by-cycle current-limit event is detected, a 4-bit up/down counter is incremented.

On each clock cycle, without a concurrent low-side current limit event, the counter is decremented or left at zero. The counter cannot wrap-around below 0000 and above 1111. High-side current limit events do not increment the counter. Only detections from low-side current limit events trigger the counter.

If the counter reaches 1111 (or 15 events), the high- and low-side MOSFETs become tri-stated, and power delivery to the output is inhibited for the duration of three times the soft-start time. This digital integration mechanism provides immunity to momentary overloading of the output. After the wait time, the MIC24046 retries entering operation and initiates a new soft-start sequence.

Figure 4-3 illustrates the hiccup mode short-circuit protection logic flow. Note that hiccup mode short-circuit protection is active at all times, including the soft-start ramp.

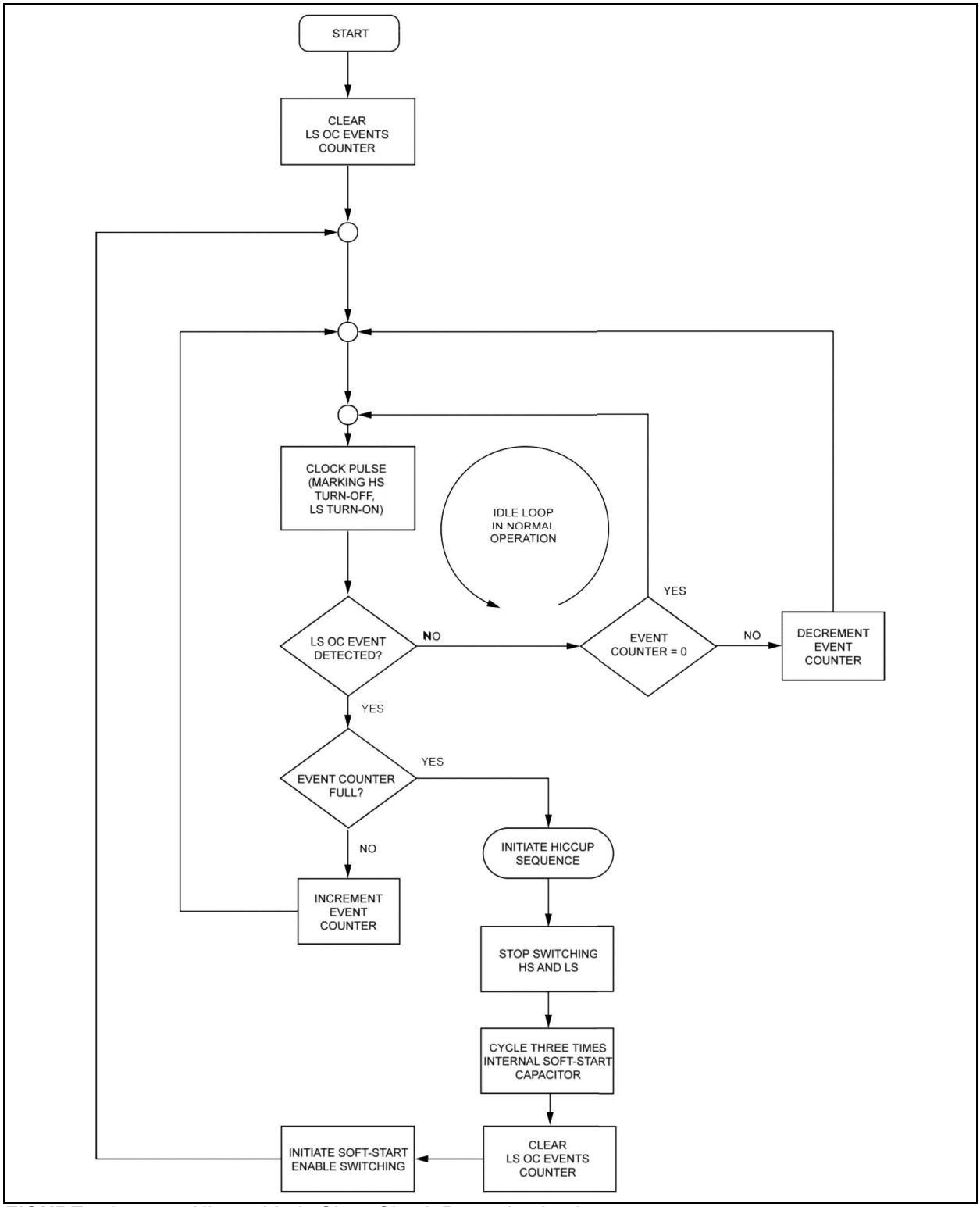


FIGURE 4-3: *Hiccup Mode Short-Circuit Protection Logic.*

5.0 APPLICATION INFORMATION

5.1 Programming Start-Up Delay and External UVLO

The EN/DLY pin allows programming of an external start-up delay. In this case, the driver for the EN/DLY pin should be an open-drain/open-collector type as shown in Figure 5-1:

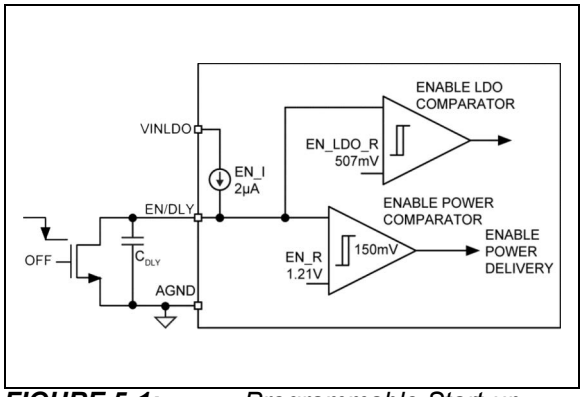


FIGURE 5-1: *Programmable Start-up Delay Function.*

The start-up delay is the delay time from the OFF falling edge to the assertion of the enable power delivery signal and can be calculated as shown in Equation 5-1:

EQUATION 5-1:

$$t_{SU\_DLY} = \frac{EN\_R \times C_{DLY}}{EN\_I}$$

Where:

EN_R = 1.21V

EN_I = 2 µA

C_{DLY} = Delay programming external capacitor

The EN/DLY pin can also be used to program an UVLO threshold for power delivery by means of an external resistor divider, as described in the following Figure 5-2.

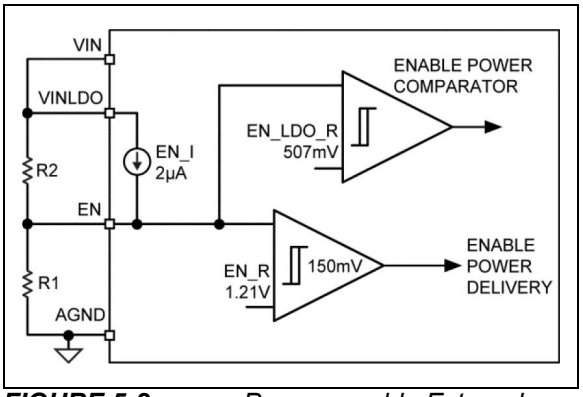


FIGURE 5-2: *Programmable External UVLO Function.*

The programmed V_{IN} UVLO threshold V_{IN_RISE} is given by:

EQUATION 5-2:

$$V_{IN\_RISE} = EN\_R \times \left(1 + \frac{R2}{R1}\right) - EN\_I \times R2$$

Where:

EN_R = 1.21V

EN_I = 2 µA

R1 and R2 are external resistors.

To desensitize the V_{IN} UVLO threshold against variations of the pull-up current EN_I, it is recommended to run the R1 − R2 voltage divider at a significantly higher current level than the EN_I current.

The corresponding V_{IN} UVLO hysteresis V_{IN_HYS} is calculated as follows:

EQUATION 5-3:

$$V_{IN\_HYS} = 150mV \times \left(1 + \frac{R2}{R1}\right)$$

Similar calculations also apply to the internal LDO activation threshold.

5.2 Setting the Switching Frequency

The MIC24046 switching frequency can be programmed using the FREQ pin as shown in Table 5-1:

TABLE 5-1: SWITCHING FREQUENCY SETTINGS

FREQ	Frequency
Hi-Z (Open)	400 kHz
0 (GND)	565 kHz
1 (VDDA)	790 kHz

5.3 Setting the Output Voltage

The MIC24046 output voltage can be programmed by setting pins VOSET0 and VOSET1, as shown in Table 5-2.

TABLE 5-2: OUTPUT VOLTAGE SETTINGS

VOSET1	VOSET0	Output Voltage
0 (GND)	0 (GND)	3.3V
0 (GND)	1 (VDDA)	2.5V (2.49V)
1 (VDDA)	0 (GND)	1.8V
1 (VDDA)	1 (VDDA)	1.5V
0 (GND)	Hi-Z (Open)	1.2V
Hi-Z (Open)	0 (GND)	1.0V
1 (VDDA)	Hi-Z (Open)	0.9V
Hi-Z (Open)	1 (VDDA)	0.8V
Hi-Z (Open)	Hi-Z (Open)	0.7V

To achieve accurate output voltage regulation, the OUTSNS pin (internal feedback divider top terminal) should be Kelvin-connected as close as possible to the point-of-regulation top terminal. Since both the internal reference and the internal feedback divider's bottom terminal refer to AGND, it is important to minimize voltage drops between the AGND and the point-of-regulation return terminal.

5.4 Setting the Current Limit

The MIC24046 valley-mode current limit on the low-side MOSFET can be programmed by means of ILIM pin as shown in Table 5-3.

TABLE 5-3: CURRENT-LIMIT SETTING

ILIM	Low-Side Valley Current Limit (Typical Value)	Rated Output Current
0 (GND)	4.6 A	3A
1 (VDDA)	6.2 A	4A
Hi-Z (Open)	6.8 A	5A

Note that the programmed current-limit values act as pulse-by-pulse current-limit thresholds on the valley inductor current. If the inductor current has not decayed below the threshold at the time the PWM requires a new ON time, the high-side MOSFET turn-on is either delayed until the valley current recovers below the threshold or skipped. Each time the high-side MOSFET turn-on is skipped, a 4-bit up-down counter is incremented. When the counter reaches the configuration 1111, a hiccup sequence is invoked in order to reduce power dissipation under prolonged short-circuit conditions.

The highest current-limit setting (6.8A) is intended to comfortably accommodate a 5A application.

Ensure the value of the operating junction temperature does not exceed the maximum rating in high output power applications.

5.5 Inductor Selection and Slope Compensation

When selecting an inductor, it is important to consider the following factors:

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)
- Core losses

The inductance value is critical to the operation of MIC24046. Because the MIC24046 is a valley current-mode regulator, it needs a slope compensation for the stable current loop operation where duty cycles are below 50%. Slope compensation is internally programmed according to the frequency and output voltage selection, assuming there is a minimum inductance value for the given operating condition. Table 5-4 lists the assumed minimum inductor values recommended for stable current loop operation. Note that the minimum suggested inductance values should be met when taking into account inductor tolerance and its change with current level.

TABLE 5-4: RECOMMENDED INDUCTANCE VALUES AT V_{IN} = 12V

V_{OUT} Selection	Frequency	Minimum Inductance
0.7V, 0.8V, 0.9V, 1.0V, 1.2V	400 kHz	0.97
	565 kHz	0.68
	790 kHz	0.49
1.5V, 1.8V	400 kHz	1.51
	565 kHz	1.06
	790 kHz	0.76
2.49V, 3.3V	400 kHz	2.42
	565 kHz	1.70
	790 kHz	1.21

The slope compensation is also internally adapted to the input-output voltage differential.

In practical implementations of valley-current-mode control, slope compensation is also added to any duty cycle larger than 50% as part of improving current loop stability and noise immunity for all input and output voltage ranges. Consequently, the MIC24046 adds internal slope compensation signal up to 60% duty cycle. Above this, no slope compensation is added. For this reason, the PWM modulator gain exhibits an abrupt change when the duty cycle exceeds 60%, possibly leading to some increase in jitter and noise susceptibility.

If operation around and above 60% duty cycle is considered, a more conservative design of the compensation loop might help in reducing jitter and noise sensitivity.

Inductor current ratings are generally stated as permissible DC current and saturation current. Permissible DC current can be rated for a 20°C to 40°C temperature rise. Saturation current can be rated for a 10% to 30% loss in inductance. Ensure that the nominal current of the application is well within the permissible DC current ratings of the inductor, depending on the allowed temperature rise. Note that the inductor permissible DC current rating typically does not include inductor core losses. These are very important contributors of total inductor core loss and temperature increase in high-frequency DC/DC converters because core losses increase rapidly with the excitation frequency.

When saturation current is specified, make sure that there are enough design margins so the peak current does not cause the inductor to enter deep saturation.

Pay attention to the inductor saturation characteristic in current limit. The inductor should not heavily saturate, even in current limit operation. If there is heavy saturation, the current may instantaneously run away and reach potentially destructive levels. Typically, ferrite-core inductors exhibit an abrupt saturation characteristic, while powdered-iron or composite inductors have a soft-saturation characteristic. Peak current can be calculated with Equation 5-4.

EQUATION 5-4:

$$I_{L,PEAK} = \left[I_O + V_O \left(\frac{1 - V_O / V_{IN}}{2 \times f \times L} \right) \right]$$

As shown in Equation 5-4, the peak inductor current is inversely proportional to the switching frequency and the inductance. The lower the switching frequency or inductance, the higher the peak current. As input voltage increases, the peak current also increases.

5.6 Output Capacitor Selection

Two main requirements determine the size and characteristics of the output capacitor:

- Steady-state ripple
- Maximum voltage deviation during load transient

For steady-state ripple calculation, the ESR and the capacitive ripple both contribute to the total ripple amplitude.

From the switching frequency, input voltage, output voltage setting, and load current, the peak-to-peak inductor current ripple and the peak inductor current can be calculated as:

EQUATION 5-5:

$$\Delta I_{L\_PP} = V_O \left(\frac{1 - V_O / V_{IN}}{f_S \times L} \right)$$

EQUATION 5-6:

$$I_{L,PEAK} = I_O + \frac{\Delta I_{L\_PP}}{2}$$

The capacitive ripple $\Delta V_{R,C}$ and the ESR ripple $\Delta V_{R,ESR}$ are given by:

EQUATION 5-7:

$$\Delta V_{R,C} = \frac{\Delta I_{L\_PP}}{8 \times f_S \times C_O}$$

EQUATION 5-8:

$$\Delta V_{R,ESR} = ESR \times \Delta I_{L\_PP}$$

The total peak-to-peak output ripple is then conservatively estimated as:

EQUATION 5-9:

$$\Delta V_R = \Delta V_{R,C} + \Delta V_{R,ESR}$$

The output capacitor value and ESR should be chosen so ΔV_R is within specifications. Capacitor tolerance should be considered for worst case calculations. In the case of ceramic output capacitors, factor into account the decrease of effective capacitance versus applied DC bias.

The worst-case load transient for output capacitor calculation is an instantaneous 100% to 0% load release when the inductor current is at its peak value. In this case, all the energy stored in the inductor is absorbed by the output capacitor while the converter stops switching and keeps the low-side FET ON.

The peak output voltage overshoot (ΔV_{OUT}) happens when the inductor current has decayed to zero. This can be calculated with Equation 5-10:

EQUATION 5-10:

$$\Delta V_O = \sqrt{V_O^2 + \frac{L}{C_O} \times I_{L,PEAK}^2} - V_O$$

Equation 5-11 calculates the minimum output capacitance value ($C_{O(MIN)}$) needed to limit the output overshoot below ΔV_{OUT}.

EQUATION 5-11:

$$C_{O(MIN)} = \frac{L \times I_{L,PEAK}^2}{[\Delta V_O - V_O] - V_O^2}$$

The result from the minimum output capacitance value for load transient is the most stringent requirement found for capacitor value in most applications. Low equivalent series resistance (ESR) ceramic output capacitors with X5R or X7R temperature characteristics are recommended.

For low output voltage applications with demanding load transient requirements, using a combination of polarized and ceramic output capacitors may be most convenient for smallest solution size.

5.7 Input Capacitor Selection

Two main requirements determine the size and characteristics of the input capacitor:

- Steady-state ripple
- RMS current

The buck converter input current is a pulse train with very fast rising and falling times so low-ESR ceramic capacitors are recommended for input filtering, because of their good high-frequency characteristics.

For ideal input filtering (assuming a DC input current feeding the filtered buck power stage), and by neglecting the capacitor ESR contribution to the input ripple (typically possible for ceramic input capacitors), the minimum capacitance value $C_{IN(MIN)}$ needed for a given input peak-to-peak ripple voltage $\Delta V_{r,IN}$ can be estimated as shown in Equation 5-12:

EQUATION 5-12:

$$C_{IN(MIN)} = \frac{I_O \times D \times (1-D)}{\Delta V_{r,IN} \times f_S}$$

The RMS current $I_{IN,RMS}$ of the input capacitor is estimated as in Equation 5-13:

EQUATION 5-13:

$$I_{IN,RMS} = I_O \times \sqrt{D \times (1-D)}$$

Note that for a given output current I_O, the worst case values are obtained at D = 0.5.

Multiple input capacitors can be used to reduce input ripple amplitude and/or individual capacitor RMS current.

5.8 Compensation Design

As a simple first-order approximation, the valley-current-mode-controlled buck power stage can be modeled as a voltage-controlled current-source feeding the output capacitor and load. The inductor current state-variable is removed and the power-stage transfer function from COMP to the inductor current is modeled as a transconductance (gm_{PS}).

The simplified model of the control loop is shown in Figure 5-3. The power-stage transconductance gm_{PS} shows some dependence on current levels and it is also somewhat affected by process variations, therefore some design margin is recommended against the typical value gm_{PS} = 12.5A/V (see the Electrical Characteristics table).

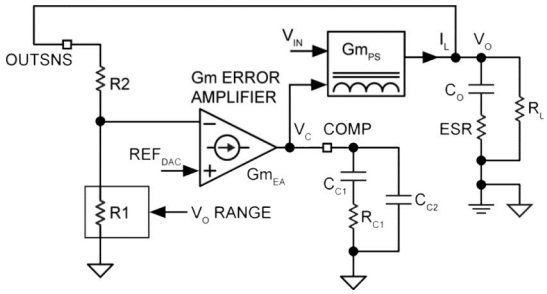


FIGURE 5-3: *Simplified Small-Signal Model of the Voltage Regulation Loop.*

This simplified approach disregards all issues related to the inner current loop, like its stability and bandwidth. This approximation is good enough for most operating scenarios, where the voltage-loop bandwidth is not pushed to aggressively high frequencies.

Based on the model shown in Figure 5-3, the control-to-output transfer function is:

EQUATION 5-14:

$$G_{CO(S)} = \frac{V_{O(S)}}{V_{C(S)}} = Gm_{PS} \times R_L \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)}$$

Where:

f_Z and f_P = The frequencies associated with the output capacitor ESR zero and with the load pole, respectively.

EQUATION 5-15:

$$f_Z = \frac{1}{2\pi \times C_O \times ESR}$$

EQUATION 5-16:

$$f_P = \frac{1}{2\pi \times C_O \times (ESR + R_L)}$$

The MIC24046 uses a transconductance (gm_{EA} = 1.5 mA/V) error amplifier. Frequency compensation is implemented with a Type-II network (R_{C1}, C_{C1}, and C_{C2}) connected from COMP to AGND.

The compensator transfer function consists of an integrator for zero DC (voltage regulation error), a zero to boost the phase margin of the overall loop gain around the crossover frequency, and an additional pole that can be used to cancel the output capacitor ESR zero, or to further attenuate switching frequency ripple.

In both cases, the additional pole makes the regulation loop less susceptible to switching frequency noise. The additional pole is created by capacitor C_{C2}. Equation 5-17 details the compensator transfer function $H_{C(S)}$ (from OUTSNS to COMP).

EQUATION 5-17:

$$H_{C(S)} = -\frac{R1}{R1+R2} \times Gm_{EA} \times \frac{1}{S \times (C_{C1}+C_{C2})} \times \frac{(1 \times S \times R_{C1} \times C_{C1})}{\left(1 + S \times R_{C1} \times \frac{C_{C1} \times C_{C2}}{C_{C1}+C_{C2}}\right)}$$

The overall voltage loop gain $T_{V(S)}$ is the product of the control-to-output and the compensator transfer functions:

EQUATION 5-18:

$$T_{V(S)} = G_{CO(S)} \times H_{C(S)}$$

The value of the attenuation ratio R1/(R1 + R2) depends on the output voltage selection, and can be retrieved as illustrated in Table 5-5:

TABLE 5-5: INTERNAL FEEDBACK DIVIDER ATTENUATION VALUES

V_O Range	R1/(R1 + R2)	A (A = 1 + R2/R1)
0.7V − 1.2V	1	1
1.5V − 1.8V	0.5	2
2.5V(2.49V) − 3.3V	0.333	3

The compensation design process is as follows:

1. Set the $T_{V(S)}$ loop gain crossover frequency f_{XO} in the range $f_S/20$ to $f_S/10$. Lower values of f_{XO} allow a more predictable and robust phase margin. Higher values of f_{XO} would involve additional considerations about the current loop bandwidth in order to achieve a robust phase margin. Taking a more conservative approach is highly recommended.

EQUATION 5-19:

$$f_{XO} = \frac{f_S}{20}$$

2. Select R_{C1} to achieve the target crossover frequency f_{XO} of the overall voltage loop. This typically happens where the power stage transfer function $G_{CO(S)}$ is rolling off at −20 dB/dec. The compensator transfer function $H_{C(S)}$ is in the so-called mid-band gain region where C_{C1} can be considered a DC-blocking short circuit while C_{C2} can still be considered as an open circuit, as calculated in Equation 5-20:

EQUATION 5-20:

$$R_{C1} = \left(\frac{R1+R2}{R1}\right) \cdot \frac{2\pi \times C_O \times f_{XO}}{Gm_{EA} \cdot Gm_{PS}}$$

3. Select capacitor C_{C1} to place the compensator zero at the load pole. The load pole moves around with load variations, so to calculate the load pole use as a load resistance R_L the value determined by the nominal output current I_O of the application, as shown in Equation 5-21 and Equation 5-22:

EQUATION 5-21:

$$R_L = \frac{V_O}{I_O}$$

EQUATION 5-22:

$$C_{C1} = \frac{C_O \times (ESR + R_L)}{R_{C1}}$$

4. Select capacitor C_{C2} to place the compensator pole at the point where the frequency of the output capacitor ESR is zero, or at ≥ 5 f_{XO}, whichever is lower.

The C_{C2} is intended for placing the compensator pole at the frequency of the output capacitor ESR zero, and/or achieve additional switching ripple/noise attenuation.

If the output capacitor is a polarized one, its ESR zero will typically occur at low enough frequencies to cause the loop gain to flatten out and not roll-off at a −20 dB/decade slope around or just after the crossover frequency f_{XO}. This causes undesirable scarce compensation design robustness and switching noise susceptibility. The compensator pole is then used to cancel the output capacitor ESR zero, and achieve a well-behaved roll-off of the loop gain above the crossover frequency.

If the output capacitors are only ceramic, then the ESR zero frequencies could be very high. In many cases, the frequencies could even be above the switching frequency itself. Loop gain roll-off at −20 dB/decade well beyond the crossover frequency is ensured, but even in this case, it is good practice to still make use of the compensator pole to further attenuate switching noise, while conserving phase margin at the crossover frequency.

For example, setting the compensator pole at 5 f_{XO}, will limit its associated phase loss at the crossover frequency to about 11°. Placement at even higher frequencies N × f_{XO} (N > 5) will reduce phase loss even further, at the expense of less noise/ripple attenuation at the switching frequency. Some attenuation of the switching frequency noise/ripple is achieved as long as N × f_{XO} < f_S.

For polarized output capacitor, compensator pole placement at the ESR zero frequency is achieved shown in Equation 5-23:

EQUATION 5-23:

$$C_{C2} = \frac{1}{\frac{R_{C1}}{C_O \times ESR} - \frac{1}{C_{C1}}}$$

For ceramic output capacitor, compensator pole placement at N × f_{XO} (N ≥ 5, N × f_{XO} < f_S) is achieved as detailed in Equation 5-24:

EQUATION 5-24:

$$C_{C2} = \frac{1}{2\pi \times R_{C1} \times N \times f_{XO} - \frac{1}{C_{C1}}}$$

5.9 Output Voltage Soft-Start Rate

The MIC24046 features internal analog soft-start, such that the output voltage can be smoothly increased to the target regulation voltage. The soft-start rate given in the Electrical Characteristics table is referred to the error amplifier reference, and therefore the effective soft-start rate value seen at the output of the module has to be scaled according to the internal feedback divider attenuation values listed in Table 5-5.

To calculate the effective output voltage soft-start slew rate SS_SR_{OUT} based on the particular output voltage setting and the reference soft-start slew rate SS_SR, use the following formula:

EQUATION 5-25:

$$SS\_SR_{OUT} = A \cdot SS\_SR$$

Where:

The value of A (amplification, A = 1 + R2/R1) is given in the right column of Table 5.

5.10 Operation from different supply rails for power and control

MIC24046 allows for a variety of applications by using the VIN and VINLDO pins together or separately.

For example, if an external 5V nominal (range: 4.5V-5.5V) bias voltage is available, the internal LDO regulator can also be bypassed and power can be directly fed to the analog and drivers supply pins (VDDA and VDDP), by connecting VINLDO and VDDA all together to the external 5V bias.

The VIN pins provide the input voltage to the switching power stage. If the VIN pins are connected to a separate supply from VINLDO, the VIN voltage range can be extended down to 2.5V.

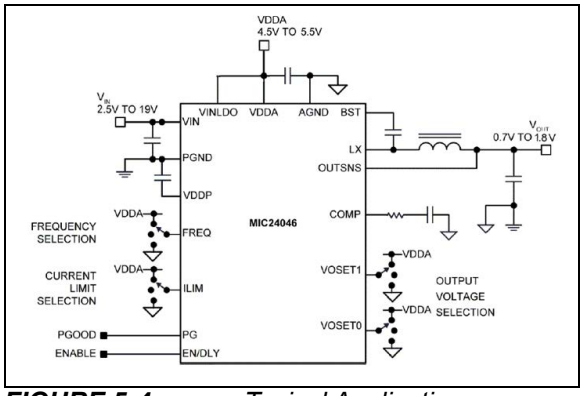


FIGURE 5-4: *Typical Application Schematic with VDDA Bias Externally Supplied.*

In this case, care must be taken in the sequencing of the VIN and VDDA voltage during start-up as the soft-start circuitry is initiated only by the trigger of the UVLO on the VDDA or by the EN signal.

In the situations where VDDA is the first voltage which is established, the start-up of the device must be initiated through the EN pin in order for the output voltage to follow the soft-start ramp.

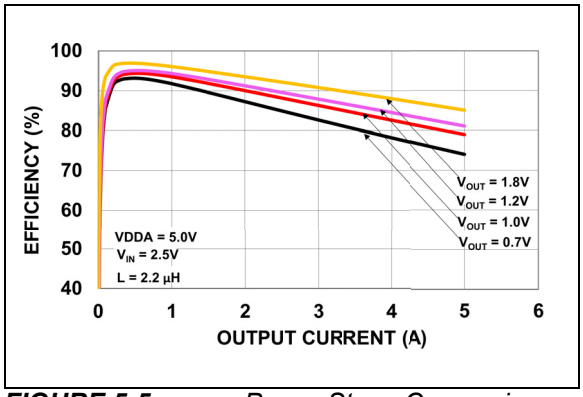


FIGURE 5-5: *Power Stage Conversion Efficiency (V_{IN} = 2.5V) vs. Output Current.*

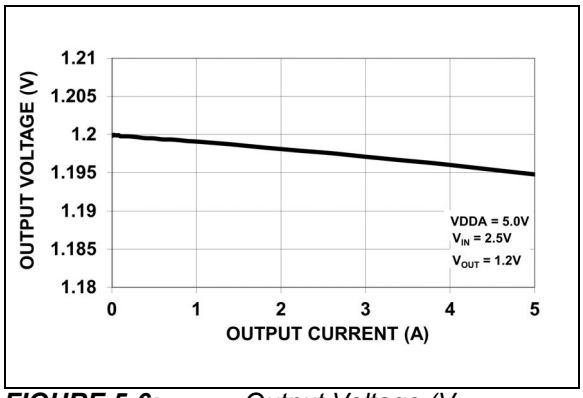


FIGURE 5-6: *Output Voltage (V_{OUT} = 1.2V) vs. Output Current.*

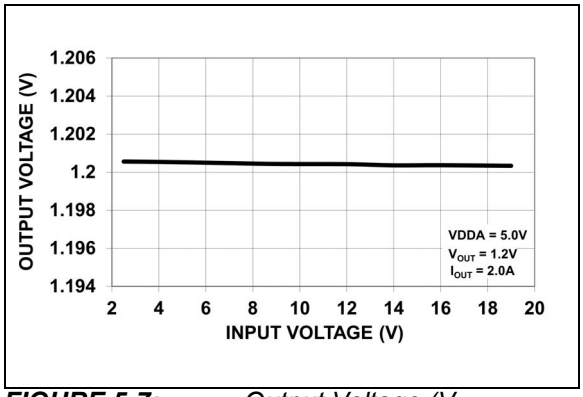


FIGURE 5-7: *Output Voltage (V_{OUT} = 1.2V) vs. Input Voltage (V_{IN}).*

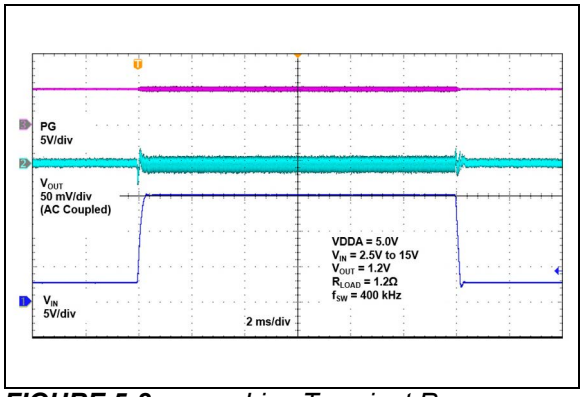


FIGURE 5-8: *Line Transient Response.*

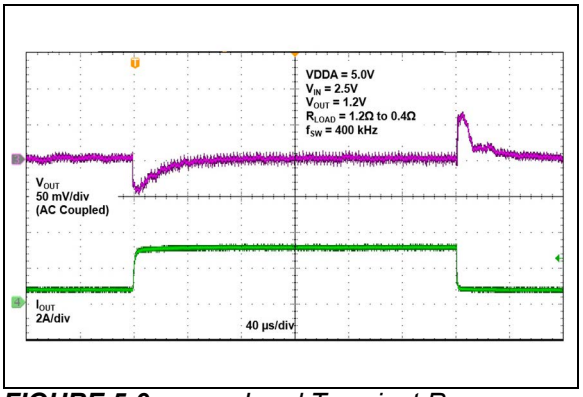
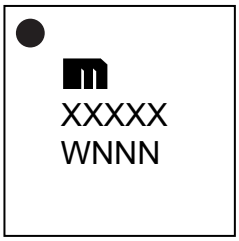


FIGURE 5-9: *Load Transient Response.*

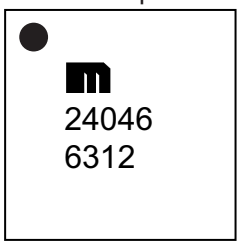
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

20-Lead VQFN*



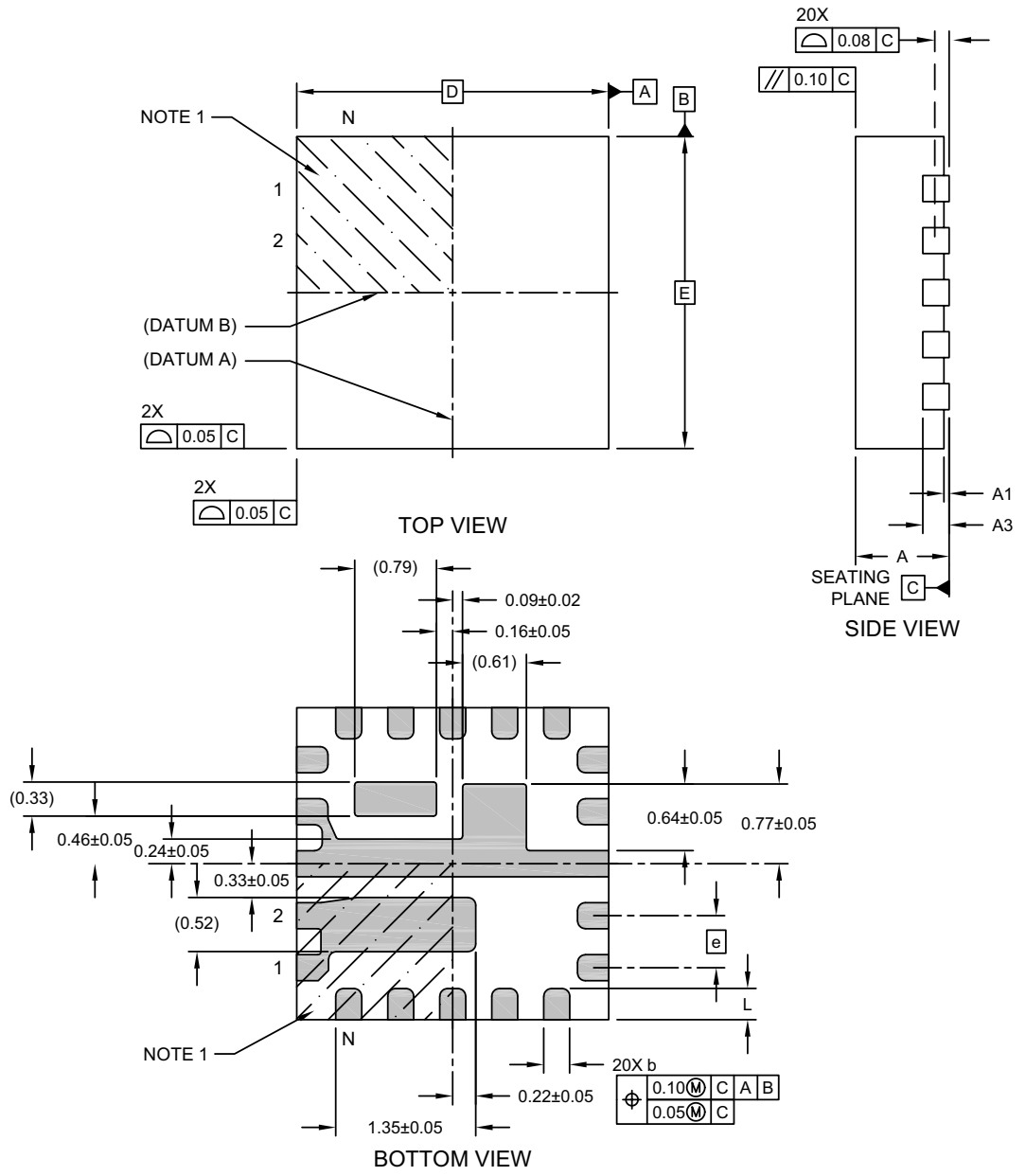
Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	W or WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N.

20-Lead VQFN 3 mm x 3 mm Package Outline and Recommended Land Pattern



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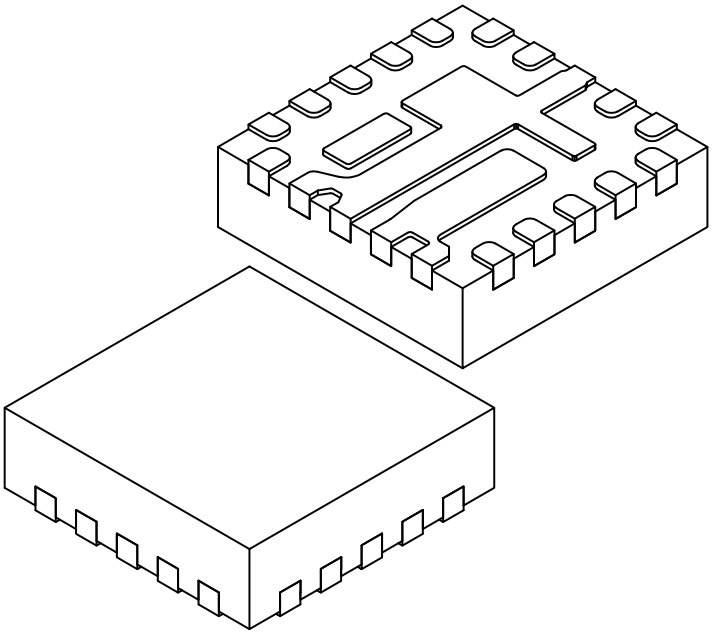


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Overall Width	E		3.00 BSC	
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.30	0.35

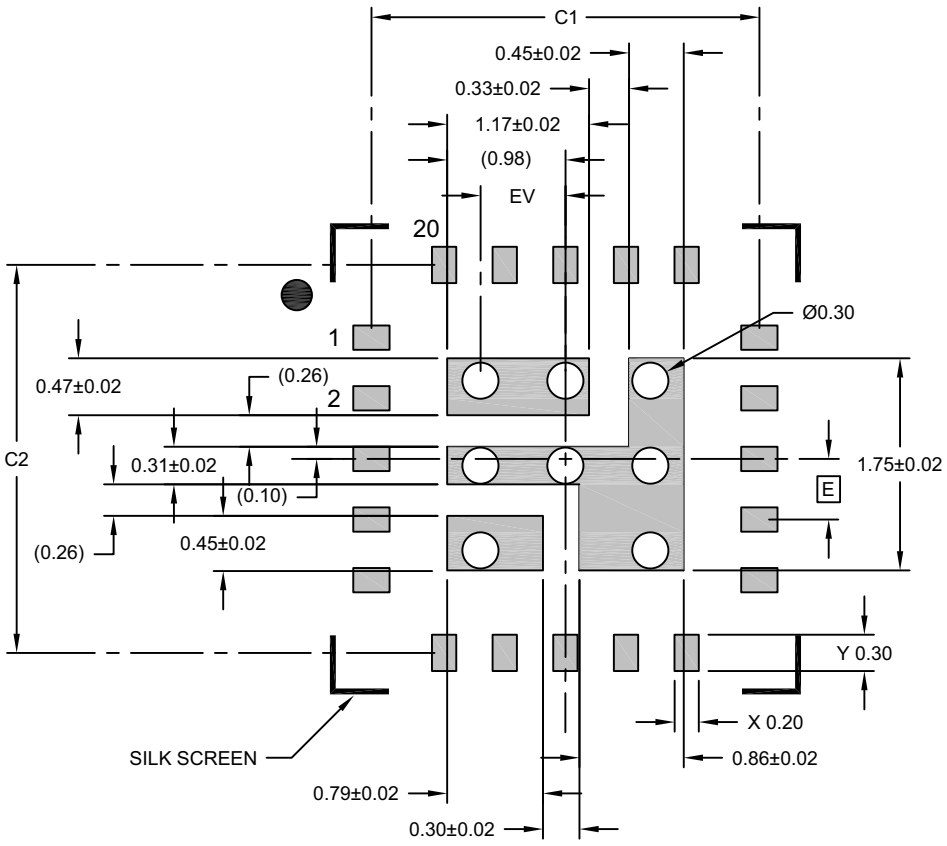
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1030 Rev A Sheet 2 of 2



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		3.20	
Contact Pad Spacing	C2		3.20	
Contact Pad Width (Xnn)	X			0.25
Contact Pad Length (Xnn)	Y			0.35
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		0.70	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3030 Rev A

APPENDIX A: REVISION HISTORY

Revision A (May 2022)

- Converted Micrel document MIC24046 to Microchip data sheet DS20006677A.
- Text corrections throughout as needed.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	X	XX	-XX
Device	Junction Temp. Range	Package	Media Type

Device:	MIC24046:	Pin-Programmable, 4.5V to 19V, 5A Step-Down Converter
Junction Temperature Range:	Y =	–40°C to +125°C
Package:	FL =	20-Lead 3 mm x 3 mm VQFN
Media Type:	TR =	5,000/Reel

Examples:

a) MIC24046YFL-TR: MIC24046, 4.5V - 19V, –40°C to +125°C Temp. Range, 20-Lead 3x3 VQFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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