BiCMOS Current-Mode PWM Controllers

Features

- Fast 40 ns Output Rise and 30 ns Output Fall Times
- –40°C to +85°C Ambient Temperature Range Meets UC284x Specifications
- · High-Performance, Low-Power BiCMOS Process
- Ultra-Low Start-Up Current (50 μA Typical)
- Low Quiescent Operating Current (4 mA Typical)
- · CMOS Outputs with Rail-to-Rail Swing
- · Up to 500 kHz Current-Mode Operation
- · Trimmed 5V Bandgap Reference
- Pin-for-Pin Compatible with UC3842/3843/3844/3845(A)
- Trimmed Oscillator Discharge Current
- · UVLO with Hysteresis
- · Low Cross-Conduction Currents

Applications

- Current-Mode, Offline, Switched-Mode Power Supplies
- · Current-Mode, DC-to-DC Converters
- · Step-Down Buck Regulators
- · Step-Up Boost Regulators
- · Flyback, Isolated Regulators
- · Forward Converters
- Synchronous FET Converters

General Description

The MIC38C4x are fixed-frequency, high performance, current-mode PWM controllers. Microchip's BiCMOS devices are pin compatible with 384x bipolar devices, but feature several improvements.

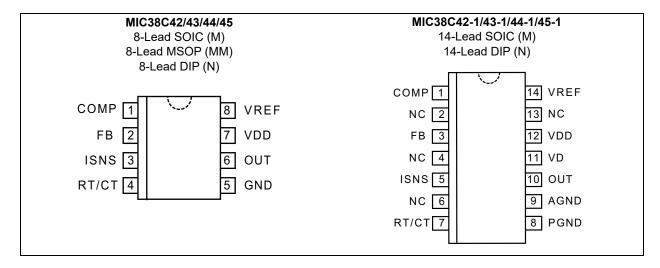
Undervoltage lockout circuitry allows the '42 and '44 versions to start up at 14.5V and operate down to 9V, and the '43 and '45 versions start at 8.4V with operation down to 7.6V. All versions operate up to 20V.

When compared to bipolar 384x devices operating from a 15V supply, start-up current has been reduced to 50 μ A typical and operating current has been reduced to 4.0 mA typical. Decreased output rise and fall times drive larger MOSFETs, and rail-to-rail output capability increases efficiency, especially at lower supply voltages. The MIC38C4x also features a trimmed oscillator discharge current and bandgap reference.

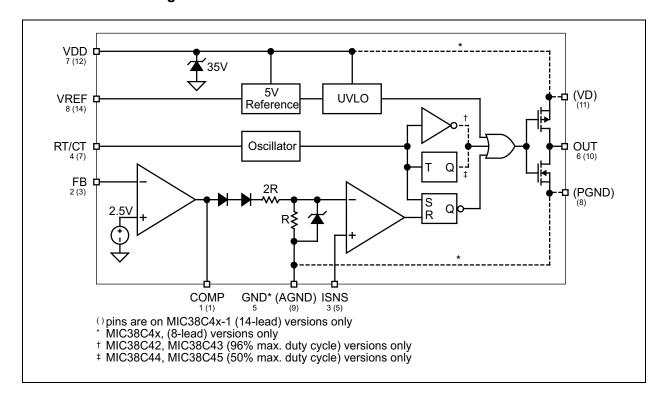
The MIC38C4x denotes 8-pin plastic DIP, SOIC, and MSOP packages. MIC38C4x-1 denotes 14-pin plastic DIP and SOIC packages. 8-pin devices feature small size, while 14-pin devices separate the analog and power connections for improved performance and power dissipation.

For fast rise and fall times and higher output drive, refer to the MIC38HC4x.

Package Types



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Zener Current (I _Z at VDD Pin)	30 mA
Operation at ≥ 18V may require special precautions. See Note 1.	
Supply Voltage (V _{DD} , Note 1)	+20V
Switch Supply Voltage (V _D)	+20V
Current Sense Voltage (V _{ISNS})	
Feedback Voltage (V _{FB})	
Output Current (I _{OUT})	0.5A

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: On the 8-pin version, 20V is the maximum input on Pin 7 because this is also the supply pin for the output stage. On the 14-pin version, 40V is the maximum for Pin 12 and 20V is the maximum for Pin 11.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 15V, Adjust V_{DD} above the start threshold before setting at 15V; R_T = 11.0 kΩ; C_T = 3.3 nF; -40° C ≤ T_A ≤ +85°C; unless noted. Note 1

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Reference			I .	I .		
Output Voltage	V_{REF}	4.90	5.00	5.10	V	T _A = +25°C, I _{VREF} = 1 mA
Line Regulation	$\Delta V_{REF(LINE)}$	_	2	20	mV	12V ≤ V _{DD} ≤ 18V, I _{VREF} = 5 μA, Note 6
Load Regulation	$\Delta V_{REF(LOAD)}$	_	1	25	mV	1 mA ≤ I _{VREF} ≤ 20 mA
Temperature Stability	TC _{VREF}	_	0.2		mV/°C	Note 2
Total Output Variation	$\Delta V_{REF(TOT)}$	4.82	_	5.18	V	Line, Load, Temperature, Note 2
Output Noise Voltage	V _{NOISE}	_	50		μV	10 Hz ≤ f ≤ 10 kHz, T _A = +25°C, Note 2
Long-Term Stability	$\Delta V_{REF(LT)}$		5	25	mV	T _A = +125°C, 1000 hours, Note 2
Output Short-Circuit	I _{VREF(SC)}	-30	-80	-180	mA	_
Oscillator	, , ,				•	
Initial Accuracy	$\Delta f_{OSC(INIT)}$	49	52	55	kHz	T _A = +25°C, Note 3
Voltage Stability	$\Delta f_{OSC(VS)}$	_	0.2	1.0	%	12V ≤ V _{DD} ≤ 18V, Note 6
Temperature Stability	TC _{FOSC}	_	0.04	_	%/°C	$T_{MIN} \le T_A \le T_{MAX}$, Note 2
Clock Ramp Reset		6.0	8.4	9.0	mA	T _A = +25°C, V _{RT/CT} = 2V
Current	IDISCHG	6.0	8.4	9.5	mA	$T_A = T_{MIN}$ to T_{MAX}
Amplitude	V_{AMP}	_	1.9	_	V_{PP}	V _{RT/CT} peak-to-peak
Error Amp						
Input Voltage	V _{IN(EA)}	2.42	2.50	2.58	V	V _{COMP} = 2.5V
Input Bias Current	I _{BIAS(EA)}	_	-0.1	-2	μA	V _{FB} = 5.0V
Open Loop Voltage Gain	A _{VOL}	65	90	_	dB	2V ≤ V _{COMP} ≤ 4V
Unity Gain Bandwidth	GBW	0.7	1.0	_	MHz	Note 2
Power Supply Rejection Ratio	PSRR _{EA}	60	_	_	dB	12V ≤ V _{DD} ≤ 18V
Output Sink Current	I _{COMP(SINK)}	2	14	_	mA	V _{FB} = 2.7V, V _{COMP} = 1.1V
Output Source Current	I _{COMP(SRC)}	-0.5	-1	_	mA	V _{FB} = 2.3V, V _{COMP} = 5V
COMP High Voltage	V _{COMP_H}	5	6.8		V	V_{FB} = 2.3V, R_{LOAD} = 15 kΩ to ground
COMP Low Voltage	V _{COMP_L}		0.1	1.1	V	V_{FB} = 2.7V, R_{LOAD} = 15 kΩ to V_{REF}
Current Sense	<u>-</u>					
Divider Gain Input-to-Output	A _{DIV}	2.85	3.0	3.15	V/V	Note 4, Note 5
Maximum Threshold	V _{TH(MAX)}	0.9	1	1.1	V	V _{COMP} = 5V, Note 4
Power Supply Rejection Ratio	PSRR _{CS}	_	70	_	dB	12V ≤ V _{DD} ≤ 18V, Note 4
Input Bias Current	I _{BIAS(CS)}	_	-0.1	-2	μΑ	_
Delay to Output	t _D	_	120	250	ns	_
Output						
R _{DS(ON)} Pull High	R _{DSON_H}	_	20	_	Ω	I _{SOURCE} = 200 mA
R _{DS(ON)} Pull Low	R _{DSON_L}	_	11	_	Ω	I _{SINK} = 200 mA
Rise Time	t _R	_	40	80	ns	T _A = +25°C, C _{LOAD} = 1 nF
Fall Time	t _F	_	30	60	ns	T _A = +25°C, C _{LOAD} = 1 nF

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 15V, Adjust V_{DD} above the start threshold before setting at 15V; R_T = 11.0 kΩ; C_T = 3.3 nF; $-40^{\circ}C \le T_A \le +85^{\circ}C$; unless noted. Note 1

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions	
Undervoltage Lockou	Undervoltage Lockout						
Start Threshold		13.5	14.5	15.5	V	MIC38C42/44	
Start Tilleshold	V _{TH(ST)}	7.8	8.4	9.0	V	MIC38C43/45	
Minimum Operating	V	8	9	10	V	MIC38C42/44	
Voltage	$V_{DD(MIN)}$	7.0	7.6	8.2	V	MIC38C43/45	
Pulse Width Modulato	or						
Maximum Duty Cycle	D	94	96	_	%	MIC38C42/43	
Maximum Duty Cycle	D _{MAX}	46	50	_	%	MIC38C44/45	
Minimum Duty Cycle	D _{MIN}	_	_	0	%	_	
Total Standby Current	t						
Start-Up Current			50	200	μA	V _{DD} = 13V for MIC38C42/44	
Start-Op Current	I _{DD(START)}	_	30			V _{DD} = 7.5V for MIC38C43/45	
Operating Supply Current	I _{DD(Q)}	_	4.0	6.0	mA	V _{FB} = V _{ISNS} = 0V	
Zener Voltage at VDD Pin	V _Z	30	37	_	V	I _{DD} = 25 mA, Note 6	

- Note 1: Specification for packaged product only.
 - 2: These parameters, although guaranteed, are not 100% tested in production.
 - **3:** Output frequency equals oscillator frequency for the MIC38C42 and MIC38C43. Output frequency for the MIC38C44 and MIC38C45 equals one-half the oscillator frequency.
 - **4:** Parameter measured at trip point of latch with $V_{FB} = 0V$.
 - 5: Gain defined as Equation 1-1; $0V \le V_{TH(ISNS)} \le 0.8V$.
 - **6:** On the 8-pin version, 20V is the maximum input on Pin 7 because this is also the supply pin for the output stage. On the 14-pin version, 40V is the maximum for Pin 12 and 20V is the maximum for Pin 11.

EQUATION 1-1:

$$A_{DIV} = \frac{\Delta V_{COMP}}{\Delta V_{TH(ISNS)}}$$

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T _S	-65	_	+150	°C	_
Operating Ambient Temperature Range	T_A	-40	_	+85	°C	_
Operating Junction Temperature Range	T_J	-4 0	_	+125	°C	_
Maximum Junction Temperature	$T_{J(MAX)}$	_	_	+150	°C	_
Package Thermal Resistance						
Thermal Resistance 8-Ld Plastic DIP	θ_{JA}	_	125	_	°C/W	_
Thermal Resistance 8-Ld MSOP	θ_{JA}	_	250	_	°C/W	_
Thermal Resistance 8-Ld SOIC	θ_{JA}	_	170	_	°C/W	_
Thermal Resistance 14-Ld Plastic DIP	θ_{JA}		90	_	°C/W	_
Thermal Resistance 14-Ld SOIC	θ_{JA}		145		°C/W	_

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note:

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

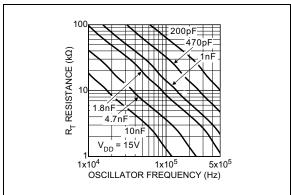


FIGURE 2-1: Oscillator Frequency Configuration.

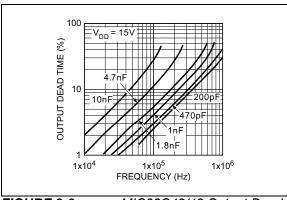


FIGURE 2-2: MIC38C42/43 Output Dead Time vs. Oscillator Frequency.

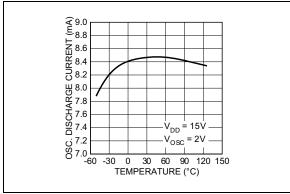


FIGURE 2-3: Oscillator Discharge Current vs. Temperature.

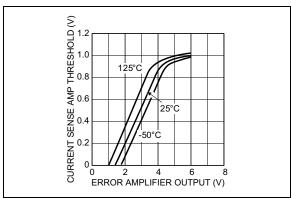


FIGURE 2-4: Current Sense Amplifier Threshold vs. Error Amplifier Output.

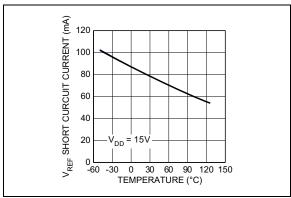


FIGURE 2-5: Short-Circuit Reference Current vs. Temperature.

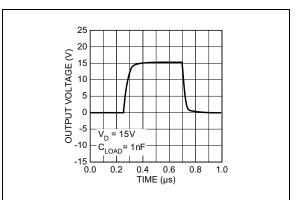


FIGURE 2-6: MIC38C4x Output Waveform.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number 8-Pin DIP, SOIC, MSOP	Pin Number 14-Pin DIP and SOIC	Pin Name	Description
1	1	COMP	Compensation: Connect external compensation network to modify the error amplifier output.
	2	NC	Not internally connected.
2	3	FB	Feedback (Input): Error amplifier input. Feedback is 2.5V at desired output voltage.
_	4	NC	Not internally connected.
3	5	ISNS	Current Sense (Input): Current sense comparator input. Connect to current sensing resistor or current transformer.
	6	NC	Not internally connected.
4	7	RT/CT	Timing Resistor/Timing Capacitor: Connect external RC network to select switching frequency.
5	_	GND	Ground: Combined analog and power ground.
_	8	PGND	Power Ground: N-channel driver transistor ground.
_	9	AGND	Analog Ground: Controller circuitry ground.
6	10	OUT	Gate Driver Output: Totem-pole output.
_	11	VD	Power Supply (Input): P-channel driver transistor supply input. Return to power ground (PGND).
7	12	VDD	Analog Supply (Input): Controller circuitry supply input. Return to analog ground (AGND).
	13	NC	Not internally connected.
8	14	VREF	5V Reference (Output): Connect external RC network.

4.0 FUNCTIONAL DESCRIPTION

Familiarity with 384x converter designs is assumed.

4.1 MIC38C4x Advantages

4.1.1 START-UP CURRENT

Start-up current has been reduced to an ultra-low $50 \,\mu\text{A}$ (typical) permitting higher-resistance, lower-wattage, start-up resistors (powers controller during power supply start-up). The reduced resistor wattage reduces cost and printed circuit space.

4.1.2 OPERATING CURRENT

Quiescent operating current has been reduced to 4 mA compared to 11 mA for a typical bipolar controller. The controller runs cooler and the V_{DD} hold-up capacitance required during start-up may be reduced.

4.1.3 OUTPUT DRIVER

Complementary internal P-channel and N-channel MOSFETs produce rail-to-rail output voltages for better performance driving external power MOSFETs. The driver transistor's low on resistance and high peak current capability can drive gate capacitances of greater than 1000 pF. The value of output capacitance which can be driven is determined only by the rise/fall time requirements. Within the restrictions of output capacity and controller power dissipation, maximum switching frequency can approach 500 kHz.

4.2 Design Precautions

When operating near 20V, circuit transients can easily exceed the 20V absolute maximum rating, permanently damaging the controller's CMOS construction. To reduce transients, connect a 0.1 μF low-ESR capacitor to next to the controller's supply V_{DD} (or V_{D} for '-1' versions) and ground connections. Film type capacitors, such as Wima MKS2, are recommended.

When designing high-frequency converters, avoid capacitive and inductive coupling of the switching waveform into high impedance circuitry such as the error amplifier, oscillator, and current sense amplifier. Avoid long printed-circuit traces and component leads. Locate oscillator and compensation circuitry near the IC. Use high frequency decoupling capacitors on $V_{\mbox{\scriptsize REF}},$ and if necessary, on $V_{\mbox{\scriptsize DD}}.$ Return high di/dt currents directly to their source and use large area ground planes.

4.3 Buck Converter

Refer to Figure 4-1. When at least 26V is applied to the input, C5 is charged through R2 until the voltage V_{DD} is greater than 14.5V (the undervoltage lockout value of the MIC38C42). Output switching begins when Q1 is

turned on by the gate drive transformer T1, charging the output filter capacitor C3 through L1. D5 supplies a regulated +12V to V_{DD} once the circuit is running.

Current sense transformer CT1 provides current feedback to ISNS for current-mode operation and cycle-by-cycle current limiting. This is more efficient than a high-power sense resistor and provides the required ground-referenced level shift.

When Q1 turns off, current flow continues from ground through D1 and L1 until Q1 is turned on again.

The 100V Schottky diode D1 reduces the forward voltage drop in the main current path, resulting in higher efficiency than could be accomplished using an ultra-fast-recovery diode. R1 and C2 suppress parasitic oscillations from D1.

Using a high-value inductance for L1 and a low-ESR capacitor for C3 permits small capacitance with minimum output ripple. This inductance value also improves circuit efficiency by reducing the flux swing in L1.

Magnetic components are carefully chosen for minimal loss at 500 kHz. CT1 and T1 are wound on Magnetics, Inc. P-type material toroids. L1 is wound on a Siemens N49 EFD core.

TABLE 4-1: MAGNETIC COMPONENTS

Symbol	Custom Coils (Note 1)	ETS (Note 2)
CT1	4923	ETS 92420
T1	4924	ETS 92419
L1	4925	ETS 92421

Note 1: Custom Coils, Alcester, SD. Tel: (605) 934-2460.

2: Energy Transformation Systems, Inc. Tel: (510) 656-2012.

TABLE 4-2: COMPONENT TEST RESULTS

Test	Conditions	Results
Line Regulation	$V_{IN} = 26V \text{ to } 80V,$ $V_{OUT} = 12V, I_{O} = 2A$	0.5%
Load Regulation	$V_{IN} = 48V, V_{OUT} = 12V,$ $I_{O} = 0.2A \text{ to } 2A$	0.6%
Efficiency	V _{IN} = 48V, V _{OUT} = 12V, I _O = 2A	90%
Output Ripple	V _{IN} = 48V, V _{OUT} = 12V, I _O = 2A (20 MHz BW)	100 mV

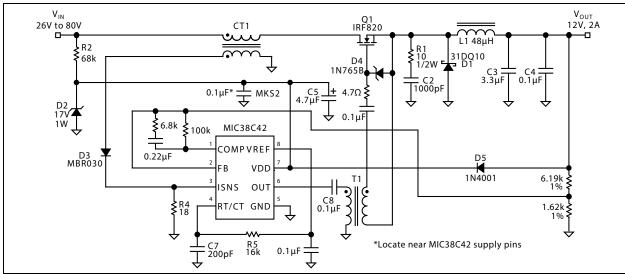


FIGURE 4-1: 500 kHz, 25W, Buck Converter.

4.4 Synchronous Buck Converter

Refer to Figure 4-2. This MIC38C43 synchronous buck converter uses an MIC5022 half-bridge driver to alternately drive the PWM switch MOSFET (driven by GATEH, or high-side output) and a MOSFET which functions as a synchronous rectifier (driven by the GATEL, or low-side output).

The low-side MOSFET turns on when the high-side MOSFET is off, allowing current to return from ground. Current flows through the low-side MOSFET in the source to drain direction.

The on-state voltage drop of the low-side MOSFET is lower than the forward voltage drop of an equivalent Schottky rectifier. This lower voltage drop results in higher efficiency.

A sense resistor (5 m Ω) is connected to the driver's high-side current sense inputs to provide overcurrent protection. Refer to the MIC5020, MIC5021, and MIC5022 data sheets for more information.

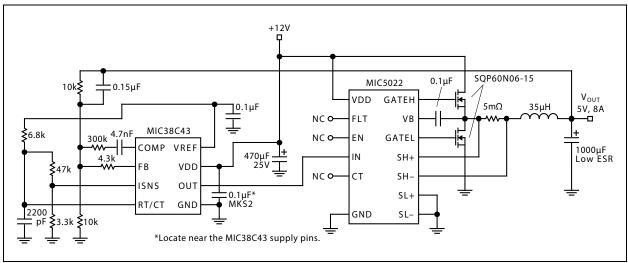
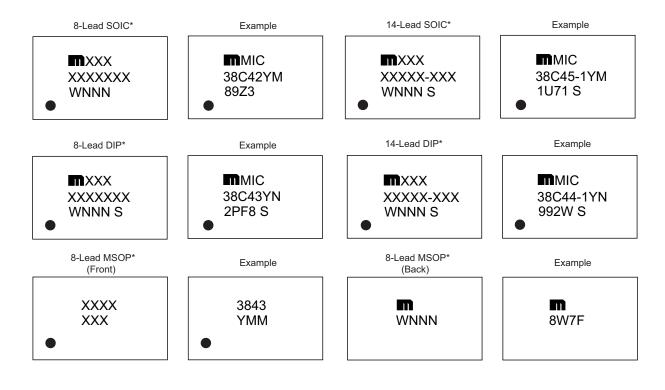


FIGURE 4-2: 100 kHz Synchronous Buck Converter.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information



Legend: XX...X Product code or customer-specific information Year code (last digit of calendar year) Υ ΥY Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') WW NNN Alphanumeric traceability code Pb-free JEDEC® designator for Matte Tin (Sn) (e3) This package is Pb-free. The Pb-free JEDEC designator (@3) can be found on the outer packaging for this package. •, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include

the corporate logo.

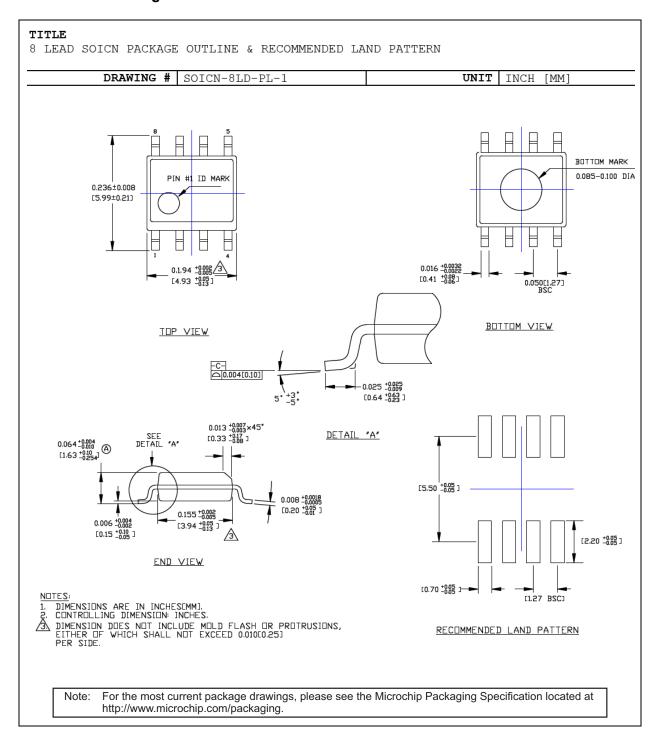
Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:

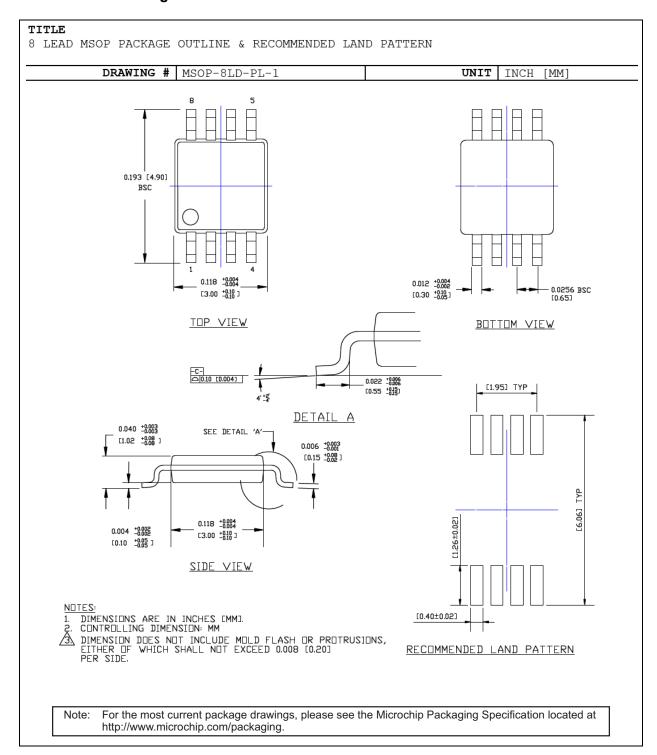
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;

2 Characters = NN: 1 Character = N

8-Lead SOIC Package Outline and Recommended Land Pattern



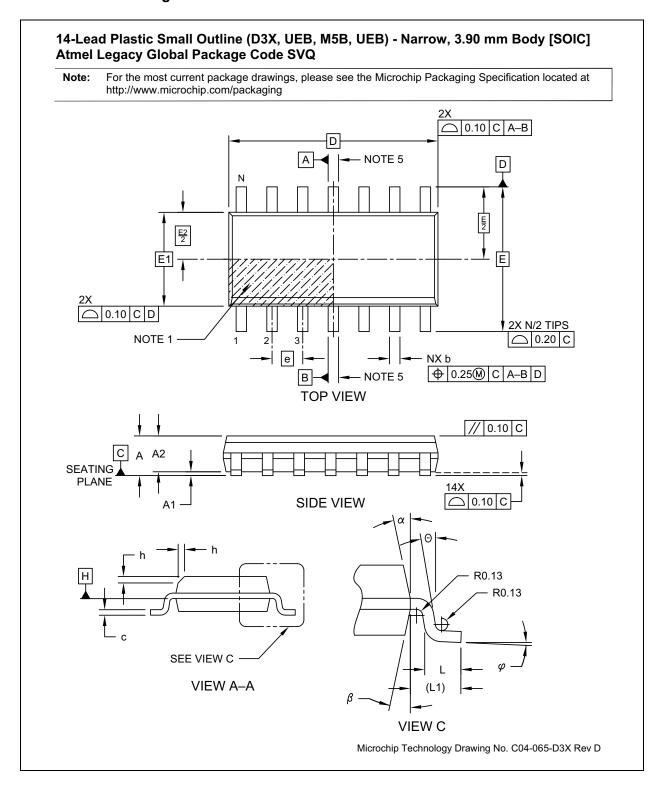
8-Lead MSOP Package Outline and Recommended Land Pattern



8-Lead DIP Package Outline and Recommended Land Pattern

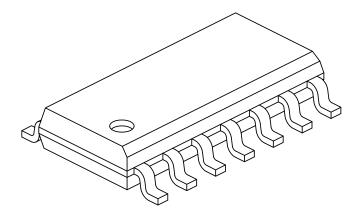
TITLE 8 LEAD PDIP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN DRAWING # PDIP-8LD-PL-1 UNIT INCH Lead Frame Copper Lead Finish Matte Tin .375±.010 GAGE PLANE .015 .010 TYP R.010 MAX .0285±.005 310 + 015 .120 MIN -TOP VIEW END VIEW 7° TYP .014 BASE MATERIAL SECTION A-A 350 ₽¥ 125 150 **⊕** .010**⊌** C .100 .045 MIN .065 MAX .018 TYP △ .010 C SIDE VIEW Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

14-Lead SOIC Package Outline and Recommended Land Pattern



14-Lead Plastic Small Outline (D3X, UEB, M5B, UEB) - Narrow, 3.90 mm Body [SOIC] Atmel Legacy Global Package Code SVQ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimensior	MIN	NOM	MAX	
Number of Pins	N		14	
Pitch	е		1.27 BSC	
Overall Height	Α	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	Е		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

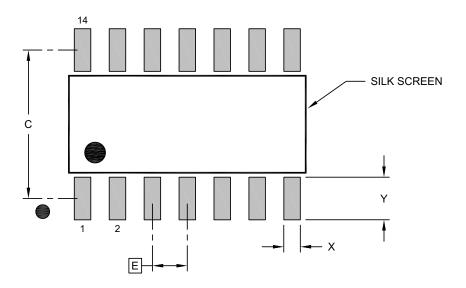
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - $\label{eq:REF:Reference Dimension, usually without tolerance, for information purposes only. \\$
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-D3X Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (D3X, UEB, M5B, UEB) - Narrow, 3.90 mm Body [SOIC] Atmel Legacy Global Package Code SVQ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	IILLIMETER:	S	
Dimension	MIN	NOM	MAX	
Contact Pitch	Е		1.27 BSC	
Contact Pad Spacing	С		5.40	
Contact Pad Width (X14)	Х			0.60
Contact Pad Length (X14)	Υ			1.55

Notes

Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-D3X Rev D

14-Lead DIP Package Outline and Recommended Land Pattern

TITLE 14 LEAD PDIP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN DRAWING # PDIP-14LD-PL-1 UNIT INCH LEAD FRAME Copper LEAD FINISH Matte Tin .060±.010 PIN#1 ø.080±.005 0.013DP MAX (3 PLACES) .005 MIN .130±.008 .085±.020 MAX BASE MATERIAL 125 SECTION A-A △ .010**⊗** C .050 TYF

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (October 2020)

- Converted Micrel document MIC38C42/43/44/45 to Microchip data sheet DS20006436A.
- Minor text changes throughout.

Revision B (February 2022)

- Updated the Package Marking Information drawing with the most current marking information.
- Updated the 14-Lead SOIC Package Outline and Recommended Land Pattern drawing with the most current file.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Device</u>	[- <u>X</u>]	<u>x</u>	<u> </u>	[- <u>XX]</u>	Examples
Part No.	Product Feature	Temp. Range	Package	Media Type	a) MIC38
Device:	MIC38C4x:		rrent-Mode PW on Guide Belov ail)		MIC38C42
	MIC38C42:		uty Cycle, UVL		MIC38C42- MIC38C42
	MIC38C43:	96% Max. D	V, Min. Operation	O Threshold	MIC38C42- MIC38C42
	MIC38C44:	50% Max. D	, Min. Operating	O Threshold	MIC38C42
	MIC38C45:	50% Max. D	V, Min. Operation uty Cycle, UVL , Min. Operating	O Threshold	MIC38C42- MIC38C42\ b) MIC380
Product Feature:		Lead I-Lead			
Junction Temperature Range:	Y =	40°C to +125°C,	RoHS-Complia	nt	MIC38C43\ MIC38C43\ MIC38C43\
Package:	MM = M	OIC Package SOP Package IP Package			MIC38C43- MIC38C43\ MIC38C43\ MIC38C43-
Media Type:	 	600/Reel 6/Tube for 8-Lead 00/Tube for MM P 0/Tube for 8-Lead 6/Tube for 14-Lea 1/Tube for 14-Lea	ackage N Package d N Package		MIC38C43Y
Selection G	Guide				MIC38C44\\ MIC38C44\

Duty Cycle	UVLO Thresholds				
_	Start-Up 8.4V Min. Operating 7.6V	Start-Up 14.5V Min. Operating 9V			
0% to 96%	MIC38C43	MIC38C42			
0% to 50%	MIC38C45	MIC38C44			

Examples:	
a) MIC38C42:	BiCMOS Current-Mode PWM
	Controller, 96% Max. Duty

Cycle, UVLO Threshold Startup 14.5V, Min. Operating 9V, -40°C to +125°C Junction Temperature

Range

8-Lead SOIC, 95/Tube /M: 1YM 14-Lead SOIC, 54/Tube /M-TR: 8-Lead SOIC, 2,500/Reel 1YM-TR 14-Lead SOIC, 2,500/Reel 'MM: 8-Lead MSOP, 100/Tube /MM-TR: 8-Lead MSOP, 2,500/Reel 14-Lead DIP, 25/Tube 1YN /N 8-Lead DIP, 50/Tube

C43: BiCMOS Current-Mode PWM Controller, 96% Max. Duty

> Cycle, UVLO Threshold Startup 8.4V, Min. Operating 7.6V, -40°C to +125°C Junction Temperature Range 8-Lead SOIC, 95/Tube

/M: 1YM 14-Lead SOIC, 54/Tube /M-TR· 8-Lead SOIC, 2,500/Reel 1YM-TR 14-Lead SOIC, 2,500/Reel /MM: 8-Lead MSOP, 100/Tube /MM-TR: 8-Lead MSOP, 2,500/Reel 1YN 14-Lead DIP, 25/Tube 8-Lead DIP, 50/Tube /N

C44: BiCMOS Current-Mode PWM

Controller, 50% Max. Duty Cycle, UVLO Threshold Startup 14.5V, Min. Operating 9V, -40°C to +125°C Junction Temperature

Range

/M: 8-Lead SOIC, 95/Tube -1YM 14-Lead SOIC. 54/Tube MIC38C44YM-TR: 8-Lead SOIC, 2,500/Reel 14-Lead SOIC, 2,500/Reel MIC38C44-1YM-TR MIC38C44YMM: 8-Lead MSOP, 100/Tube MIC38C44YMM-TR: 8-Lead MSOP, 2,500/Reel MIC38C44-1YN 14-Lead DIP. 25/Tube MIC38C44YN 8-Lead DIP, 50/Tube

d) MIC38C45: BiCMOS Current-Mode PWM Controller, 50% Max. Duty

Cycle, UVLO Threshold Startup 8.4V, Min. Operating 7.6V, -40°C to +125°C Junction Temperature Range

MIC38C45YM: 8-Lead SOIC, 95/Tube MIC38C45-1YM 14-Lead SOIC, 54/Tube 8-Lead SOIC, 2,500/Reel MIC38C45YM-TR: MIC38C45-1YM-TR 14-Lead SOIC, 2,500/Reel MIC38C45YMM: 8-Lead MSOP, 100/Tube MIC38C45YMM-TR: 8-Lead MSOP, 2,500/Reel MIC38C45-1YN 14-Lead DIP, 25/Tube MIC38C45YN 8-Lead DIP. 50/Tube

Note 1:

Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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