

## 100V Half-Bridge MOSFET Drivers

### Features

- Bootstrap Supply Voltage to 118V DC
- Supply Voltage up to 16V
- Drives High- and Low-Side N-Channel MOSFETs with Independent Inputs
- CMOS Input Thresholds (MIC4100)
- TTL Input Thresholds (MIC4101)
- On-Chip Bootstrap Diode
- Fast 30 ns Propagation Times
- Drives 1000 pF Load with 10 ns Rise and Fall Times
- Low Power Consumption
- Supply Undervoltage Protection
- 3Ω Pull-Up, 3Ω Pull-Down Output Resistance
- Space Saving 8-Lead SOIC Package
- -40°C to +125°C Junction Temperature Range

### Applications

- High Voltage Buck Converters
- Push-Pull Converters
- Full- and Half-Bridge Converters
- Active Clamp Forward Converters

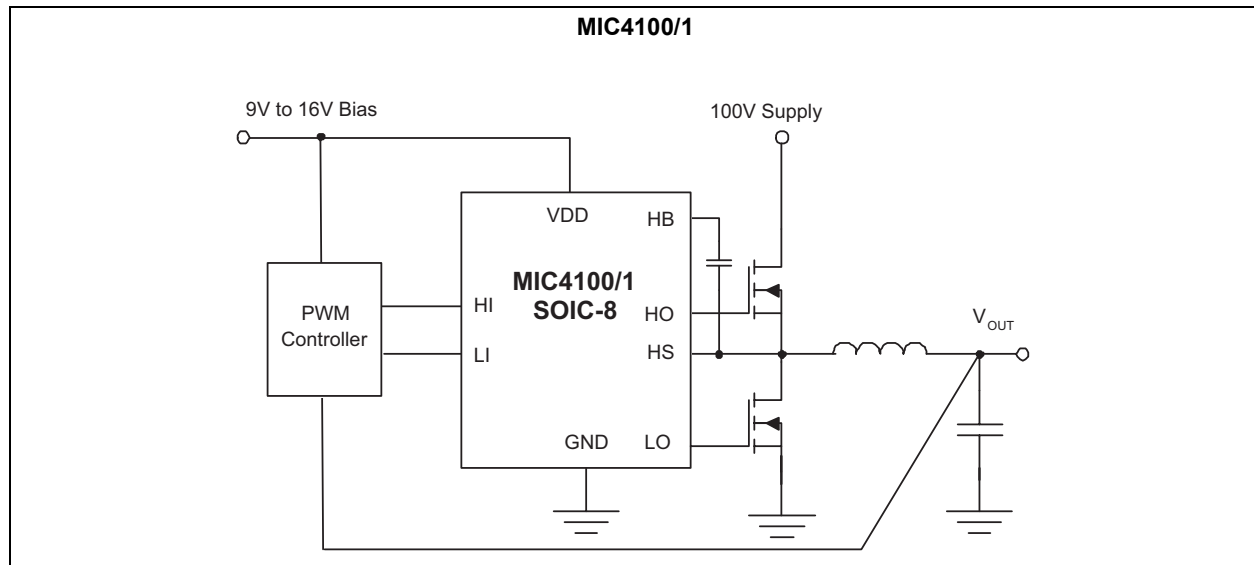
### General Description

The MIC4100 and MIC4101 are high frequency, 100V half-bridge MOSFET driver ICs that feature fast 30 ns propagation delay times. The low-side and high-side gate drivers are independently controlled and matched to within 3 ns typical. The MIC4100 has CMOS input thresholds and the MIC4101 has TTL input thresholds. The MIC4100/1 include a high voltage internal diode that charges the high-side gate drive bootstrap capacitor.

A robust, high-speed, and low-power level shifter provides clean level transitions to the high-side output. The robust operation of the MIC4100/1 ensure the outputs are not affected by supply glitches, HS ringing below ground, or HS slewing with high speed voltage transitions. Undervoltage protection is provided on both the low-side and high-side drivers.

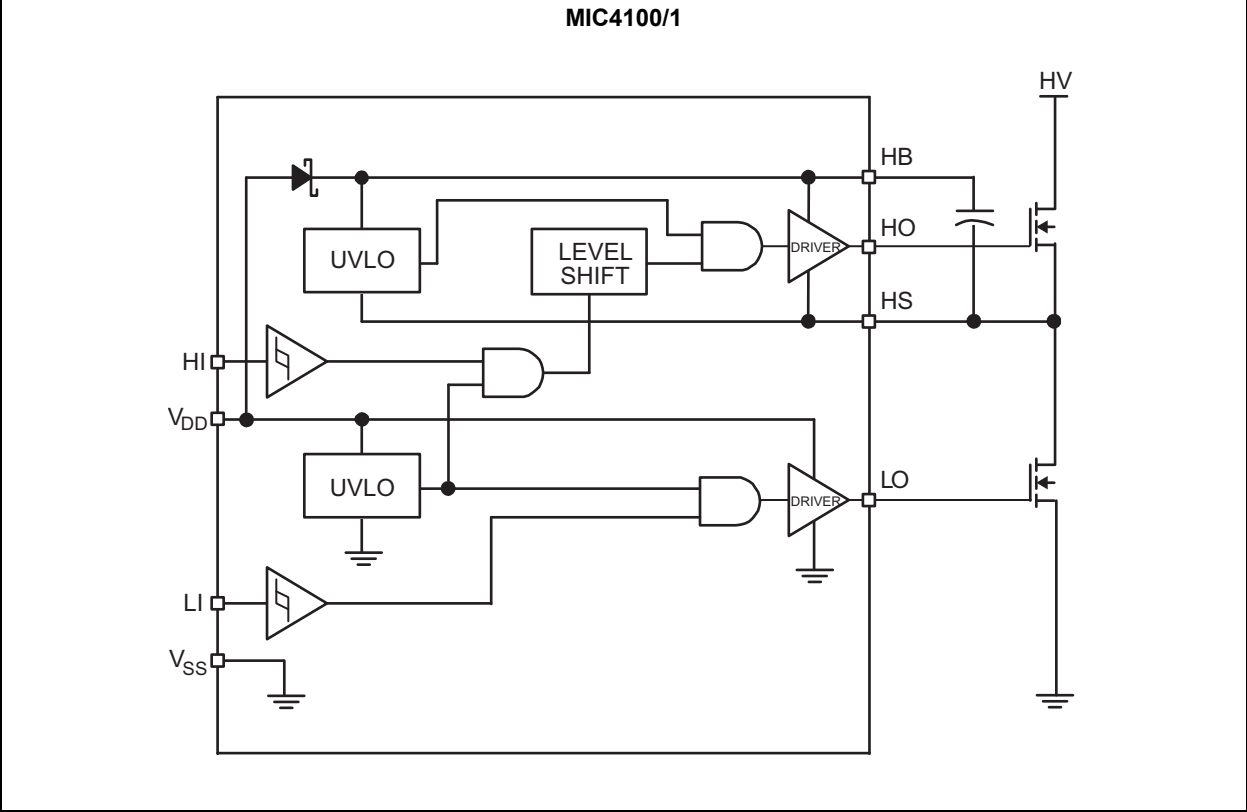
The MIC4100/1 is available in the 8-lead SOIC package with a junction operating range from -40°C to +125°C.

### Typical Application Schematic



# MIC4100/1

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage ( $V_{DD}$ , $V_{HB} - V_{HS}$ ) .....	-0.3V to +18V
Input Voltages ( $V_{LI}$ , $V_{HI}$ ) .....	-0.3V to $V_{DD} + 0.3V$
Voltage on LO ( $V_{LO}$ ) .....	-0.3V to $V_{DD} + 0.3V$
Voltage on HO ( $V_{HO}$ ) .....	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
Voltage on HS (Continuous) .....	-1V to +110V
Voltage on HB .....	+118V
Average Current in $V_{DD}$ to HB Diode .....	100 mA
ESD Rating .....	Note 1

### Operating Ratings ‡

Supply Voltage ( $V_{DD}$ ) .....	+9V to +16V
Voltage on HS .....	-1V to +100V
Voltage on HS (Repetitive Transient) .....	-5V to +105V
HS Slew Rate .....	50 V/ns
Voltage on HB .....	$V_{HS} + 8V$ to $V_{HS} + 16V$
and .....	$V_{DD} - 1V$ to $V_{DD} + 100V$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

**Note 1:** Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 k $\Omega$  in series with 100 pF.

# MIC4100/1

## ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:**  $V_{DD} = V_{HB} = 12V$ ;  $V_{SS} = V_{HS} = 0V$ ; No load on LO or HO;  $T_A = +25^\circ C$ ; unless noted. **Bold** values are valid for  $-40^\circ C \leq T_J \leq +125^\circ C$ . (**Note 1**).

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>Supply Current</b>						
$V_{DD}$ Quiescent Current	$I_{DD}$	—	40	150	$\mu A$	LI = HI = 0V
		—	—	<b>200</b>		
$V_{DD}$ Operating Current	$I_{DDO}$	—	2.5	<b>3.4</b>	mA	f = 500 kHz
Total HB Quiescent Current	$I_{HB}$	—	25	150	$\mu A$	LI = HI = 0V
		—	—	<b>200</b>		
Total HB Operating Current	$I_{HBO}$	—	1.4	2.5	mA	f = 500 kHz
		—	—	<b>3</b>		
HB to $V_{SS}$ Quiescent Current	$I_{HBS}$	—	0.05	1	$\mu A$	$V_{HS} = V_{HB} = 110V$
HB to $V_{SS}$ Operating Current	$I_{HBSO}$	—	10	—	$\mu A$	f = 500 kHz
<b>Input Pins: MIC4100 (CMOS Input)</b>						
Low Level Input Voltage Threshold	$V_{IL}$	4	5.3	—	V	—
		<b>3</b>	—	—		
High Level Input Voltage Threshold	$V_{IH}$	—	5.7	7	V	—
		—	—	<b>8</b>		
Input Voltage Hysteresis	$V_{IHYS}$	—	0.4	—	V	—
Input Pull-Down Resistance	$R_I$	<b>100</b>	200	<b>500</b>	k $\Omega$	—
<b>Input Pins: MIC4101 (TTL Input)</b>						
Low Level Input Voltage Threshold	$V_{IL}$	<b>0.8</b>	1.5	—	V	—
High Level Input Voltage Threshold	$V_{IH}$	—	1.5	<b>2.2</b>	V	—
Input Pull-Down Resistance	$R_I$	<b>100</b>	200	<b>500</b>	k $\Omega$	—
<b>Undervoltage Protection</b>						
$V_{DD}$ Rising Threshold	$V_{DDR}$	<b>6.5</b>	7.4	<b>8.0</b>	V	—
$V_{DD}$ Threshold Hysteresis	$V_{DDH}$	—	0.5	—	V	—
HB Rising Threshold	$V_{HBR}$	<b>6.0</b>	7.0	<b>8.0</b>	V	—
HB Threshold Hysteresis	$V_{HBH}$	—	0.4	—	V	—
<b>Bootstrap Diode</b>						
Low-Current Forward Voltage	$V_{DL}$	—	0.4	0.55	V	$I_{VDD-HB} = 100 \mu A$
		—	—	<b>0.70</b>		
High-Current Forward Voltage	$V_{DH}$	—	0.7	0.8	V	$I_{VDD-HB} = 100 mA$
		—	—	<b>1.0</b>		
Dynamic Resistance	$R_D$	—	1.0	1.5	$\Omega$	$I_{VDD-HB} = 100 mA$
		—	—	<b>2.0</b>		

**Note 1:** Specification for packaged product only.

**2:** Ensured by design. Not production tested.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics:**  $V_{DD} = V_{HB} = 12V$ ;  $V_{SS} = V_{HS} = 0V$ ; No load on LO or HO;  $T_A = +25^\circ C$ ; unless noted. **Bold** values are valid for  $-40^\circ C \leq T_J \leq +125^\circ C$ . (**Note 1**).

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>LO Gate Driver</b>						
Low Level Output Voltage	$V_{OLL}$	—	0.22	0.3	V	$I_{LO} = 100 \text{ mA}$
		—	—	<b>0.4</b>		
High Level Output Voltage	$V_{OHL}$	—	0.25	0.3	V	$I_{LO} = -100 \text{ mA}$ , $V_{OHL} = V_{DD} - V_{LO}$
		—	—	<b>0.45</b>		
Peak Sink Current	$I_{OHL}$	—	2	—	A	$V_{LO} = 0V$
Peak Source Current	$I_{OLL}$	—	2	—	A	$V_{LO} = 12V$
<b>HO Gate Driver</b>						
Low Level Output Voltage	$V_{OLH}$	—	0.22	0.3	V	$I_{HO} = 100 \text{ mA}$
		—	—	<b>0.4</b>		
High Level Output Voltage	$V_{OHH}$	—	0.25	0.3	V	$I_{HO} = -100 \text{ mA}$ , $V_{OHH} = V_{HB} - V_{HO}$
		—	—	<b>0.45</b>		
Peak Sink Current	$I_{OHH}$	—	2	—	A	$V_{HO} = 0V$
Peak Source Current	$I_{OLH}$	—	2	—	A	$V_{HO} = 12V$
<b>Switching Specifications</b>						
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	$t_{LPHL}$	—	27	<b>45</b>	ns	(MIC4100)
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	$t_{HPHL}$	—	27	<b>45</b>	ns	(MIC4100)
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	$t_{LPLH}$	—	27	<b>45</b>	ns	(MIC4100)
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	$t_{HPLH}$	—	27	<b>45</b>	ns	(MIC4100)
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	$t_{LPHL}$	—	31	<b>55</b>	ns	(MIC4101)
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	$t_{HPHL}$	—	31	<b>55</b>	ns	(MIC4101)
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	$t_{LPLH}$	—	31	<b>55</b>	ns	(MIC4101)
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	$t_{HPLH}$	—	31	<b>55</b>	ns	(MIC4101)
Delay Matching: Lower Turn-On and Upper Turn-Off	$t_{M(ON)}$	—	3	8	ns	—
		—	—	<b>10</b>	ns	
Delay Matching: Lower Turn-Off and Upper Turn-On	$t_{M(OFF)}$	—	3	8	ns	—
		—	—	<b>10</b>	ns	
Either Output Rise/Fall Time	$t_{RC}/t_{FC}$	—	10	—	ns	$C_L = 1000 \text{ pF}$

**Note 1:** Specification for packaged product only.

**2:** Ensured by design. Not production tested.

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## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics:**  $V_{DD} = V_{HB} = 12V$ ;  $V_{SS} = V_{HS} = 0V$ ; No load on LO or HO;  $T_A = +25^\circ C$ ; unless noted. **Bold** values are valid for  $-40^\circ C \leq T_J \leq +125^\circ C$ . (**Note 1**).

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Either Output Rise/Fall Time (3V to 9V)	$t_R/t_F$	—	0.4	0.6	$\mu s$	$C_L = 0.1 \mu F$
		—	—	<b>0.8</b>		
Minimum Input Pulse Width that changes the output	$t_{PW}$	—	—	<b>50</b>	ns	Note 2
Bootstrap Diode Turn-On or Turn-Off Time	$t_{BS}$	—	10	—	ns	—

**Note 1:** Specification for packaged product only.

**2:** Ensured by design. Not production tested.

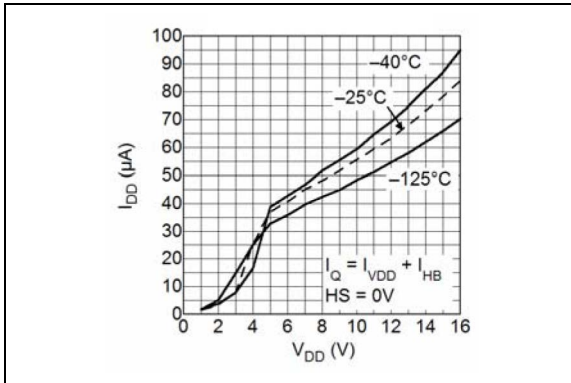
## TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Max. Junction Temperature Range	$T_J$	-55	—	+150	$^\circ C$	Note 1
Storage Temperature Range	$T_S$	-60	—	+150	$^\circ C$	—
Operating Junction Temperature Range	$T_J$	-40	—	+125	$^\circ C$	—
<b>Package Thermal Resistances</b>						
Thermal Resistance, SOIC-8Ld	$\theta_{JA}$	—	140	—	$^\circ C/W$	—

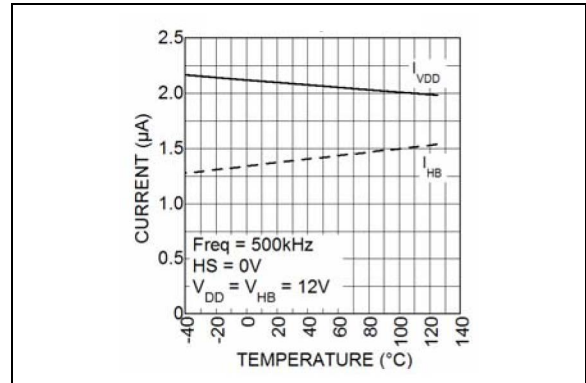
**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e.,  $T_A$ ,  $T_J$ ,  $\theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125 $^\circ C$  rating. Sustained junction temperatures above +125 $^\circ C$  can impact the device reliability.

## 2.0 TYPICAL PERFORMANCE CURVES

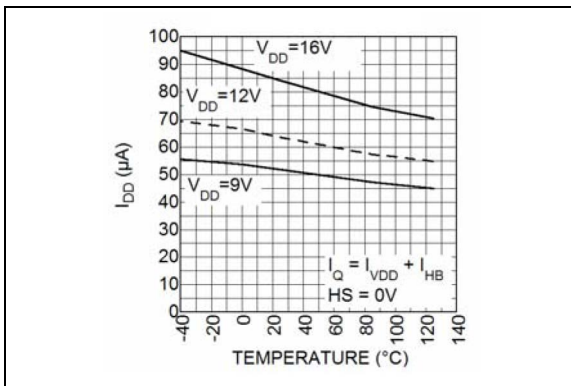
**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.



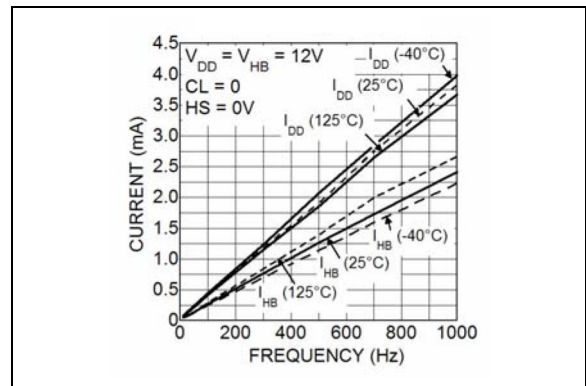
**FIGURE 2-1:** Quiescent Current vs. Supply Voltage.



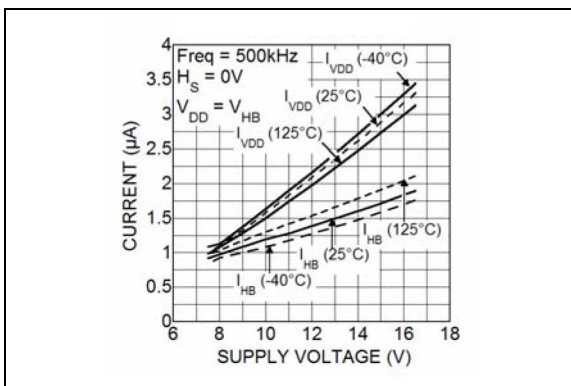
**FIGURE 2-4:** Operating Current vs. Temperature.



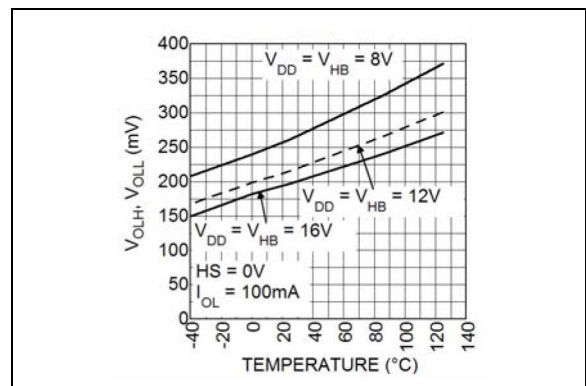
**FIGURE 2-2:** Quiescent Current vs. Temperature.



**FIGURE 2-5:** Operating Current vs. Frequency.

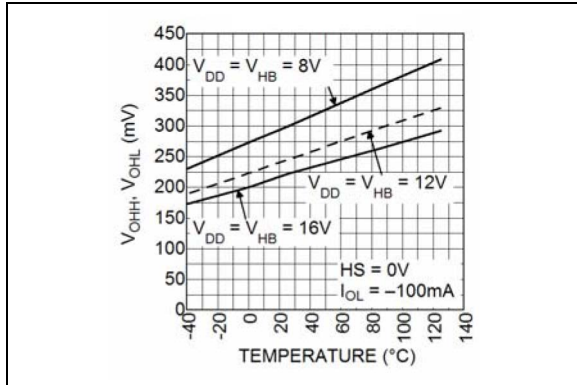


**FIGURE 2-3:** Operating Current vs. Supply Voltage.

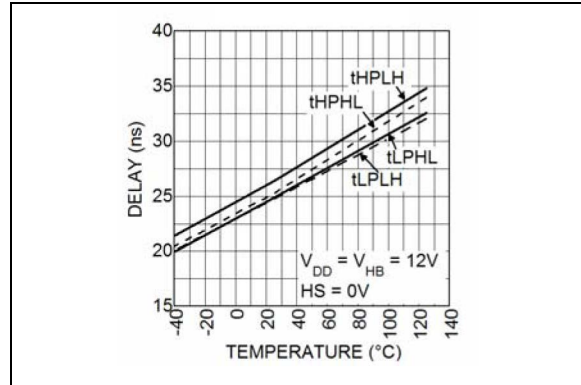


**FIGURE 2-6:** Low Level Output Voltage vs. Temperature.

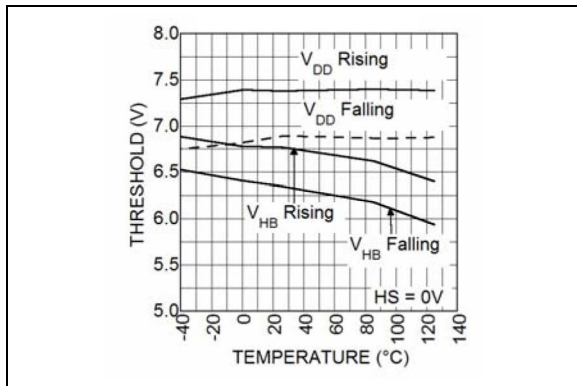
# MIC4100/1



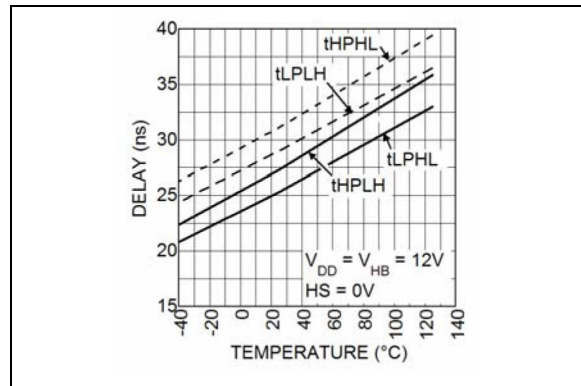
**FIGURE 2-7:** High Level Output Voltage vs. Temperature.



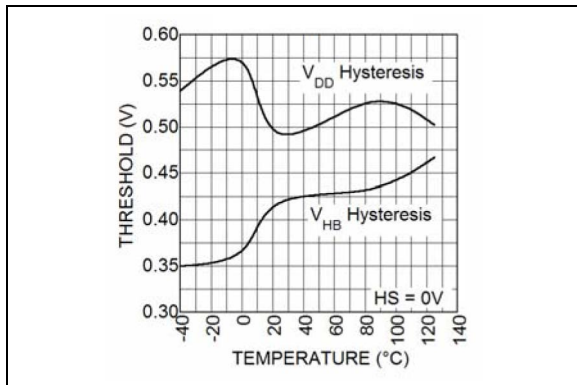
**FIGURE 2-10:** MIC4100 Propagation Delay vs. Temperature.



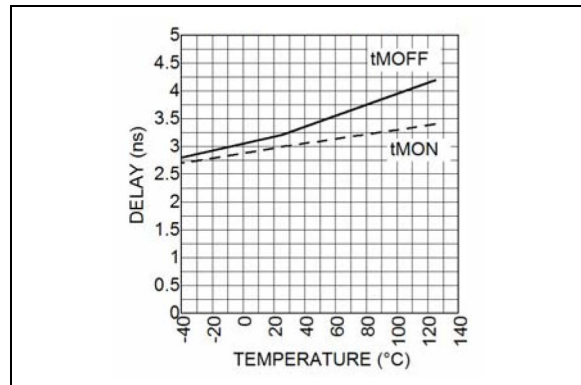
**FIGURE 2-8:** UVLO Thresholds vs. Temperature.



**FIGURE 2-11:** MIC4101 Propagation Delay vs. Temperature.

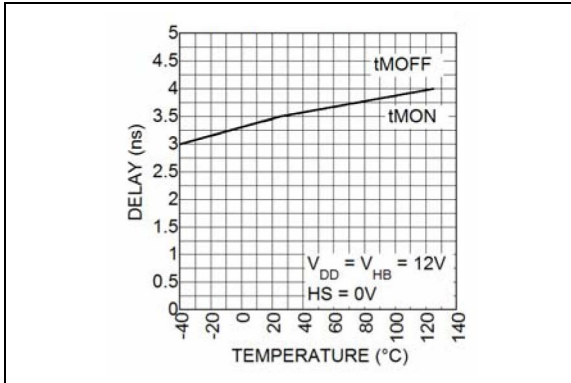


**FIGURE 2-9:** UVLO Thresholds vs. Temperature.

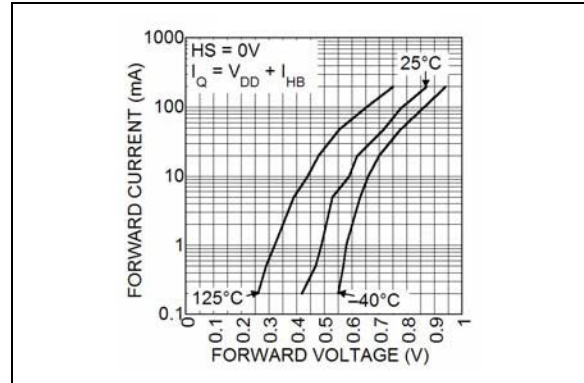


**FIGURE 2-12:** MIC4100 Propagation Delay Matching vs. Temperature.

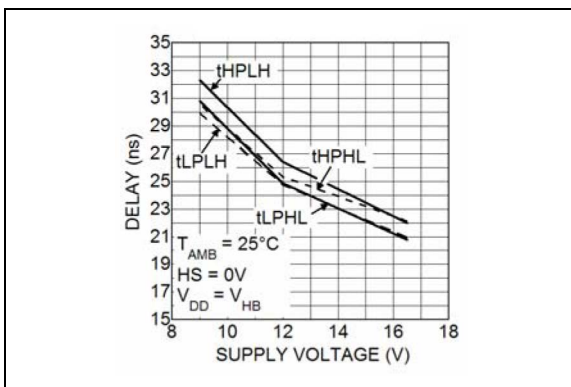




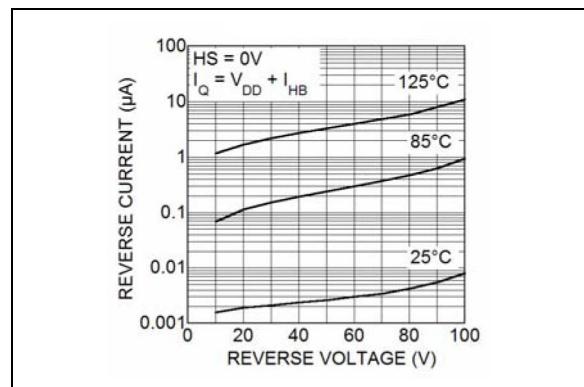
**FIGURE 2-13:** MIC4101 Propagation Delay Matching vs. Temperature.



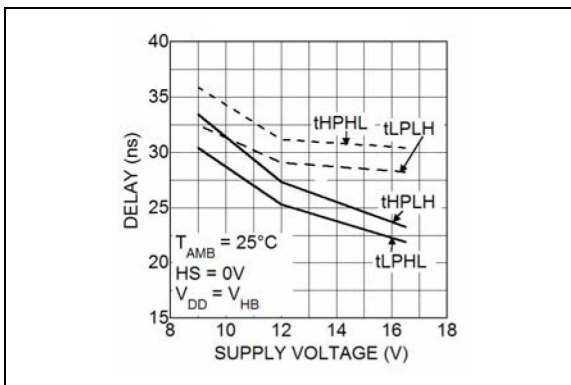
**FIGURE 2-16:** Bootstrap Diode I-V Characteristics.



**FIGURE 2-14:** MIC4100 Propagation Delay vs. Supply Voltage.



**FIGURE 2-17:** Bootstrap Diode Reverse Current.



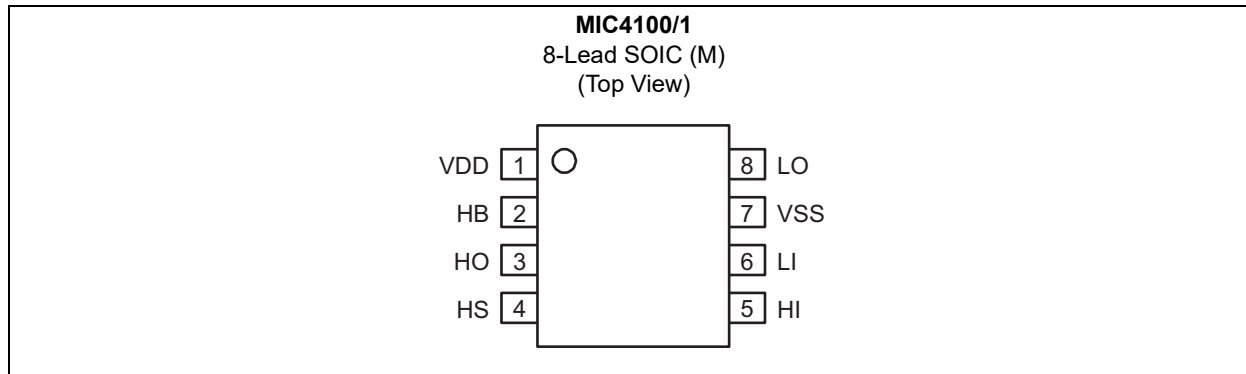
**FIGURE 2-15:** MIC4101 Propagation Delay vs. Supply Voltage.

# MIC4100/1

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

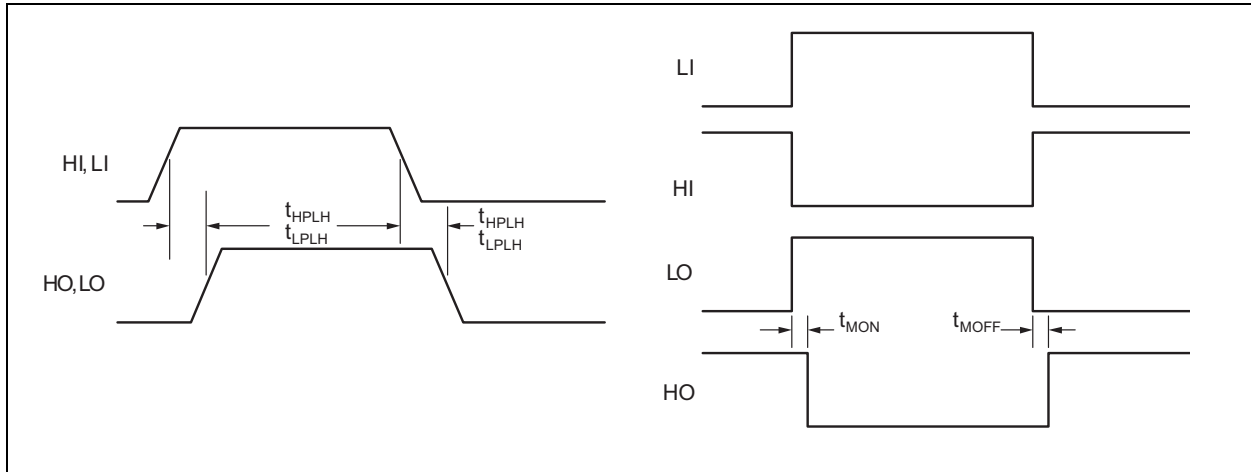
### Package Type



**TABLE 3-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	VDD	Positive supply to lower gate drivers. Decouple this pin to VSS (Pin 7). Bootstrap diode connected to HB (Pin 2).
2	HB	High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
3	HO	High-Side Output. Connect to gate of high-side power MOSFET.
4	HS	High-Side Source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	HI	High-Side Input.
6	LI	Low-Side Input.
7	VSS	Chip negative supply. Generally, this will be grounded.
8	LO	Low-Side Output. Connect to gate of low-side power MOSFET.

## 4.0 TIMING DIAGRAM



**FIGURE 4-1:** MIC4100/1 Timing Diagram.

**Note:** All propagation delays are measured from the 50% voltage level.

# MIC4100/1

## 5.0 FUNCTIONAL DESCRIPTION

The MIC4100 is a high voltage, non-inverting, synchronous MOSFET driver that has independent high-side and low-side PWM input pins that drive both high-side and low-side N-Channel MOSFETs. Refer to the [Functional Block Diagram](#).

Both drivers contain an input buffer with hysteresis, a UVLO circuit and an output buffer. The high-side output buffer includes a high speed level shifting circuit that is referenced to the HS pin. An internal diode is used as part of a bootstrap circuit to provide the drive voltage for the high-side output.

### 5.1 Startup and UVLO

The UVLO circuit forces both driver outputs low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuit monitors the voltage between the HB and HS pins. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on.

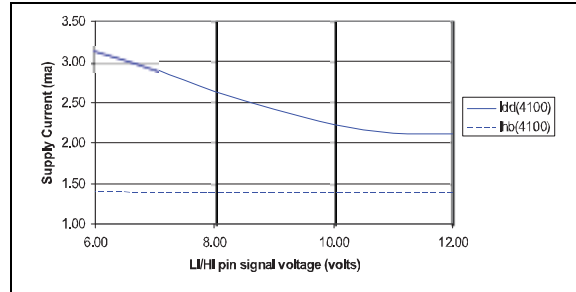
### 5.2 Input Stage

The MIC4100 and MIC4101 have different input stages, which lets these parts cover a wide range of driver applications. Both the HI and LI pins are referenced to the VSS pin. The voltage state of the input signal does not change the quiescent current draw of the driver.

The MIC4100 has a high impedance, CMOS compatible input range and is recommended for applications where the input signal is noisy or where the input signal swings the full range of voltage (from V<sub>DD</sub> to GND). There is typically 400 mV of hysteresis on the input pins throughout the V<sub>DD</sub> range. The hysteresis improves noise immunity and prevents input signals with slow rise times from falsely triggering the output. The threshold voltage of the MIC4100 varies proportionally with the V<sub>DD</sub> supply voltage.

The amplitude of the input signal affects the V<sub>DD</sub> supply current. Vin voltages that are a diode drop less than the V<sub>DD</sub> supply voltage will cause an increase in the V<sub>DD</sub> pin current. The graph in [Figure 5-1](#) shows the typical dependence between I<sub>VDD</sub> and V<sub>IN</sub> for V<sub>DD</sub> = 12V.

The MIC4101 has a TTL compatible input range and is recommended for use with inputs signals whose amplitude is less than the supply voltage. The threshold level is independent of the V<sub>DD</sub> supply voltage and there is no dependence between I<sub>VDD</sub> and the input signal amplitude with the MIC4101. This feature makes the MIC4101 an excellent level translator that will drive high threshold MOSFETs from a low voltage PWM IC.

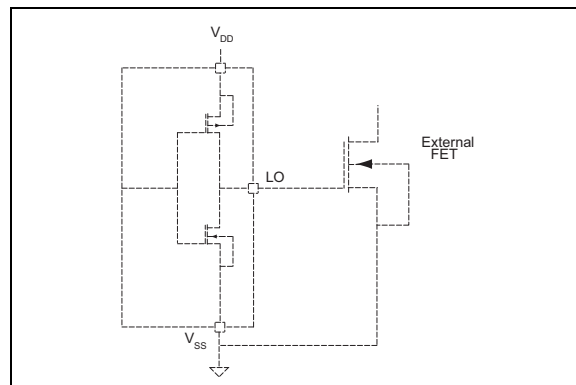


**FIGURE 5-1:** Supply Current vs. Input Voltage.

### 5.3 Low-Side Driver

A block diagram of the low-side driver is shown in [Figure 5-2](#). The low-side driver is designed to drive a ground (VSS pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low R<sub>DS(ON)</sub> from the external MOSFET.

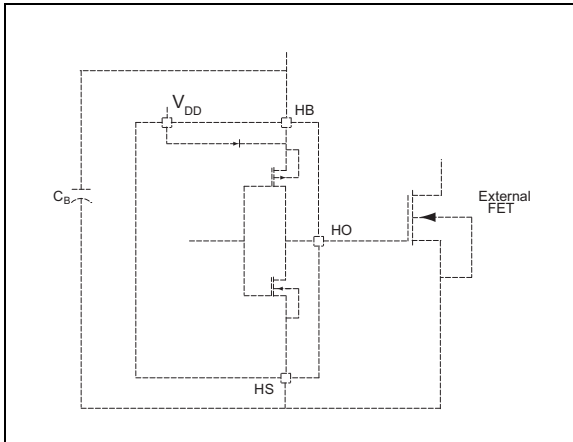
A high level applied to LI pin causes the upper driver FET to turn on and V<sub>DD</sub> voltage is applied to the gate of the external MOSFET. A low level on the LI pin turns off the upper driver and turns on the low side driver to ground the gate of the external MOSFET.



**FIGURE 5-2:** Low-Side Driver Block Diagram.

## 5.4 High-Side Driver and Bootstrap Circuit

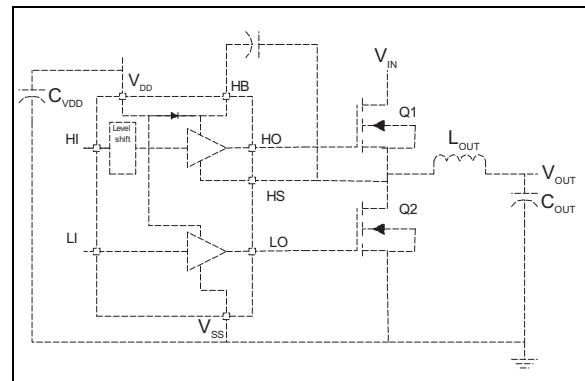
A block diagram of the high-side driver and bootstrap circuit is shown in Figure 5-3. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.



**FIGURE 5-3:** High-Side Driver Block Diagram.

A low-power, high-speed, level-shifting circuit isolates the low-side ( $V_{SS}$  pin) referenced circuitry from the high-side (HS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap circuit while the voltage level of the HS pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor,  $C_B$ . In a typical application, such as the synchronous buck converter shown in Figure 5-4, the HS pin is at ground potential while the low-side MOSFET is on. The internal diode allows capacitor  $C_B$  to charge up to  $V_{DD} - V_D$  during this time (where  $V_D$  is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the HO pin turns on, the voltage across capacitor  $C_B$  is applied to the gate of the upper external MOSFET. As the upper MOSFET turns on, voltage on the HS pin rises with the source of the high-side MOSFET until it reaches  $V_{IN}$ . As the HS and HB pin rise, the internal diode is reverse-biased, preventing capacitor  $C_B$  from discharging.



**FIGURE 5-4:** High-Side Driver and Bootstrap Circuit.

## 6.0 APPLICATION INFORMATION

### 6.1 Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

### 6.2 Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the  $C_B$  capacitor times the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by:

#### EQUATION 6-1:

$$I_{F(AVE)} = Q_{gate} \times f_S$$

Where:

$Q_{gate}$  = Total Gate Charge at  $V_{HB}$   
 $f_S$  = Gate Drive Switching Frequency

The average power dissipated by the forward voltage drop of the diode equals:

#### EQUATION 6-2:

$$P_{diode_{fwd}} = I_{F(AVE)} \times V_F$$

Where:

$V_F$  = Diode Forward Voltage Drop

The value of  $V_F$  should be taken at the peak current through the diode. However, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of  $V_F$  at the average current can be used and will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 11  $\mu A$  at a reverse voltage of 100V and 125°C. Power dissipation due to reverse leakage is typically much less than 1 mW and can be ignored.

Reverse recovery time is the time required for the injected minority carriers to be swept away from the depletion region during turn-off of the diode. Power dissipation due to reverse recovery can be calculated

by computing the average reverse current due to reverse recovery charge multiplied by the reverse voltage across the diode. The average reverse current and power dissipation due to reverse recovery can be estimated by:

#### EQUATION 6-3:

$$I_{RR(AVE)} = 0.5 \times I_{RRM} \times t_{RR} \times f_S$$

$$P_{diode_{RR}} = I_{RR(AVE)} \times V_{REV}$$

Where:

$I_{RRM}$  = Peak Reverse Recovery Current  
 $t_{RR}$  = Reverse Recovery Time

The total diode power dissipation is:

#### EQUATION 6-4:

$$P_{diode_{total}} = P_{diode_{fwd}} + P_{diode_{RR}}$$

An optional external bootstrap diode may be used instead of the internal diode (Figure 6-1). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the  $V_{DD}$  supply voltage. A 100V Schottky diode will work for most 72V input telecom applications. The equations above can be used to calculate power dissipation in the external diode. However, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as:

#### EQUATION 6-5:

$$P_{diode_{REV}} = I_R \times V_{REV} \times (1 - D)$$

Where:

$I_R$  = Reverse Current Flow at  $V_{REV}$  &  $T_J$   
 $V_{REV}$  = Diode Reverse Voltage  
 $D$  = Duty Cycle =  $t_{ON}/f_S$   
 $f_S$  = Switching Frequency of Power Supply



# MIC4100/1

The same energy is dissipated by  $R_{OFF}$ ,  $R_G$ , and  $R_{G\_FET}$  when the driver IC turns the MOSFET off. Assuming  $R_{ON}$  is approximately equal to  $R_{OFF}$ , the total energy and power dissipated by the resistive drive elements is:

## EQUATION 6-9:

$$E_{driver} = Q_G \times V_{GS}$$

Where:

$E_{driver}$  = Energy Dissipated per Switching Cycle

and

## EQUATION 6-10:

$$P_{driver} = Q_G \times V_{GS} \times f_S$$

Where:

$P_{driver}$  = Power Dissipated by Switching the MOSFET On and Off

$Q_G$  = Total Gate Charge at  $V_{GS}$

$V_{GS}$  = Gate-to-Source Voltage on the MOSFET

$f_S$  = Switching Frequency of the Gate Drive Circuit

The power dissipated inside the MIC4100/1 equals the ratio of  $R_{ON}$  and  $R_{OFF}$  to the external resistive losses in  $R_G$  and  $R_{G\_FET}$ . Letting  $R_{ON} = R_{OFF}$ , the power dissipated in the MIC4100 due to driving the external MOSFET is:

## EQUATION 6-11:

$$P_{diss\_drive} = P_{driver} \times \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}}$$

## 6.4 Supply Current Power Dissipation

Power is dissipated in the MIC4100 even if there is nothing being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The supply current is proportional to operating frequency and the  $V_{DD}$  and  $V_{HB}$  voltages. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4100 due to supply current is:

## EQUATION 6-12:

$$P_{diss\_supply} = V_{DD} \times I_{DD} + V_{HB} \times I_{HB}$$

## 6.5 Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4100 or MIC4101 equals the power dissipation caused by driving the external MOSFETs, the supply current, and the internal bootstrap diode.

## EQUATION 6-13:

$$P_{diss\_total} = P_{diss\_supply} + P_{diss\_drive} + P_{diode\_total}$$

The die temperature may be calculated once the total power dissipation is known.

## EQUATION 6-14:

$$T_J = T_A + P_{diss\_total} \times \theta_{JA}$$

Where:

$T_J$  = Junction Temperature ( $^{\circ}\text{C}$ )

$T_A$  = Maximum Ambient Temperature

$P_{diss\_total}$  = Power Dissipation of the MIC4100/1

$\theta_{JA}$  = Thermal Resistance from Junction to Ambient Air ( $^{\circ}\text{C}/\text{W}$ )

## 6.6 Propagation Delay, and Delay Matching and Other Timing Considerations

Propagation delay and signal timing is an important consideration in a high performance power supply. The MIC4100 is designed not only to minimize propagation delay but to minimize the mismatch in delay between the high-side and low-side drivers.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Many power supply topologies use two switching MOSFETs operating  $180^{\circ}$  out of phase from each other. These MOSFETs must not be on at the same time or a short circuit will occur, causing high peak



currents and higher power dissipation in the MOSFETs. The MIC4100 and MIC4101 output gate drivers are not designed with anti shoot through protection circuitry. The output drives signals simply follow the inputs. The power supply design must include timing delays (dead time) between the input signals to prevent shoot-through. The MIC4100 and MIC4101 drivers specify delay matching between the two drivers to help improve power supply performance by reducing the amount of dead time required between the input signals.

Care must be taken to insure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the  $C_B$  capacitor to charge during the off-time. Adequate time must be allowed for the  $C_B$  capacitor to charge up before the high-side driver is turned on.

## 6.7 Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low-side ( $V_{DD}$ ) and high-side (HB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs as well as minimize the voltage ripple on these pins. The capacitor from HB to HS serves double duty by providing decoupling for the high-side circuitry as well as providing current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended due to the large change in capacitance over temperature and voltage. A minimum value of 0.1  $\mu\text{F}$  is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature, and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for  $V_{DD}$  should be placed as close as possible between the  $V_{DD}$  and  $V_{SS}$  pins. The bypass capacitor ( $C_B$ ) for the HB supply pin must be located as close as possible between the HB and HS pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection

impedance is recommended. Refer to the [Grounding, Component Placement, and Circuit Layout](#) section for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge vs.  $V_{GS}$  voltage. Based on this information and a recommended  $\Delta V_{HB}$  of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

### EQUATION 6-15:

$$C_B \geq \frac{Q_G}{\Delta V_{HB}}$$

Where:

$Q_{GATE}$  = Total Gate Charge at  $V_{HB}$   
 $\Delta V_{HB}$  = Voltage Drop at the HB Pin

The decoupling capacitor for the  $V_{DD}$  input may be calculated in with the same formula; however, the two capacitors are usually equal in value.

## 6.8 Grounding, Component Placement, and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around MIC4100 and MIC4101 driver require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

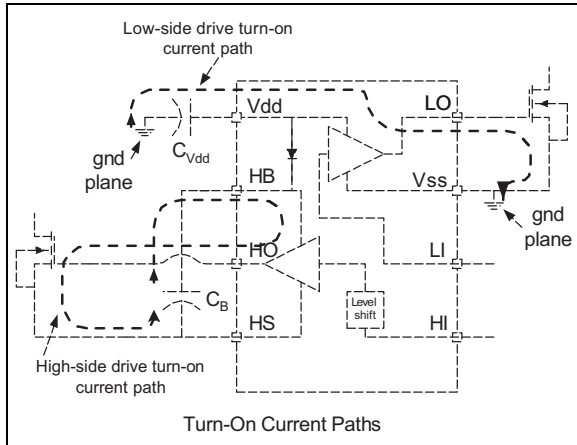
Figure 6-4 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also shows the need for a low impedance ground plane. The charge needed to turn-on the MOSFET gates comes from the decoupling capacitors  $C_{VDD}$  and  $C_B$ . Current in the low-side gate driver flows from  $C_{VDD}$  through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate voltage and can either slow down or turn off the MOSFET during the period where it should be turned on.

Current in the high-side driver is sourced from capacitor  $C_B$ , flows into the HB pin, and out the HO pin, into the gate of the high-side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor  $C_B$ . The high-side circuit return path usually does not have a low impedance ground plane, so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the

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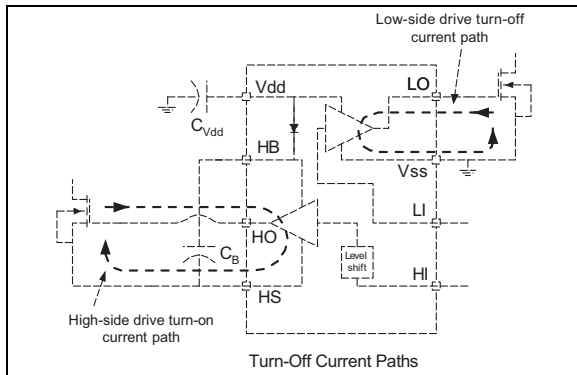
MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor  $C_B$  must be placed close to the HB and HS pins. This capacitor not only provides all the energy for turn-on, but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.



**FIGURE 6-4:** Turn-On Current Paths.

Figure 6-5 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor,  $C_B$ .



**FIGURE 6-5:** Turn-Off Current Paths.

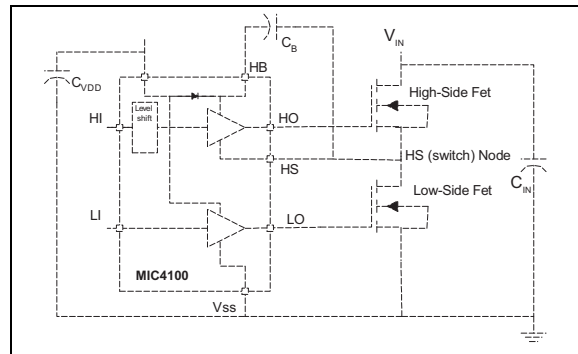
The following circuit guidelines should be adhered to for optimum circuit performance:

- The  $V_{DD}$  and HB bypass capacitors must be placed close to the supply and ground pins. It is critical that the etch length between the high side decoupling capacitor ( $C_B$ ) and the HB and HS pins be minimized to reduce lead inductance.
- A ground plane should be used to minimize parasitic inductance and impedance of the return paths. The MIC4100 is capable of greater than 2A peak currents. Any impedance between the

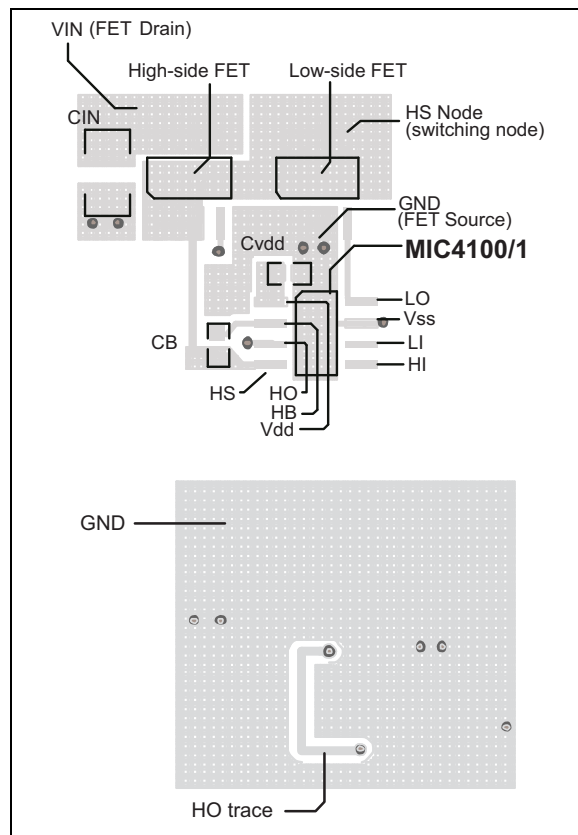
MIC4100, the decoupling capacitors, and the external MOSFET will degrade the performance of the driver.

- Trace out the high  $d_i/d_t$  and  $d_v/d_t$  paths, as shown in Figure 6-4 and Figure 6-5 to minimize the etch length and loop area for these connections. Minimizing these parameters decreases the parasitic inductance and the radiated EMI generated by fast rise and fall times.

A typical layout of a synchronous buck converter power stage using the MIC4100 (Figure 6-6) is shown in Figure 6-7.



**FIGURE 6-6:** Typical Converter Power Stage.



**FIGURE 6-7:** Typical Layout of a Synchronous Buck Converter Power Stage.

The circuit is configured as a synchronous buck power stage. The high-side MOSFET drain connects to the input supply voltage (drain) and the source connects to the switching node. The low-side MOSFET drain connects to the switching node and its source is connected to ground. The buck converter output inductor (not shown) would connect to the switching node. The high-side drive trace, HO, is routed on top of its return trace, HS, to minimize loop area and parasitic inductance. The low-side drive trace, LO, is routed over the ground plane and minimizes the impedance of that current path. The decoupling capacitors,  $C_B$  and  $C_{VDD}$ , are placed to minimize etch length between the capacitors and their respective pins. This close placement is necessary to efficiently charge capacitor  $C_B$  when the HS node is low. All traces are 0.025" wide or greater to reduce impedance.  $C_{IN}$  is used to decouple the high current path through the MOSFETs.

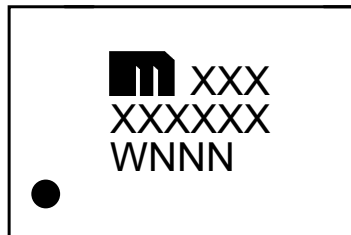
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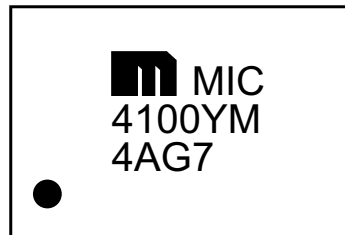
## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information

8-Lead SOIC\*



Example



<b>Legend:</b>	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar ( _ ) symbol may not be to scale.	

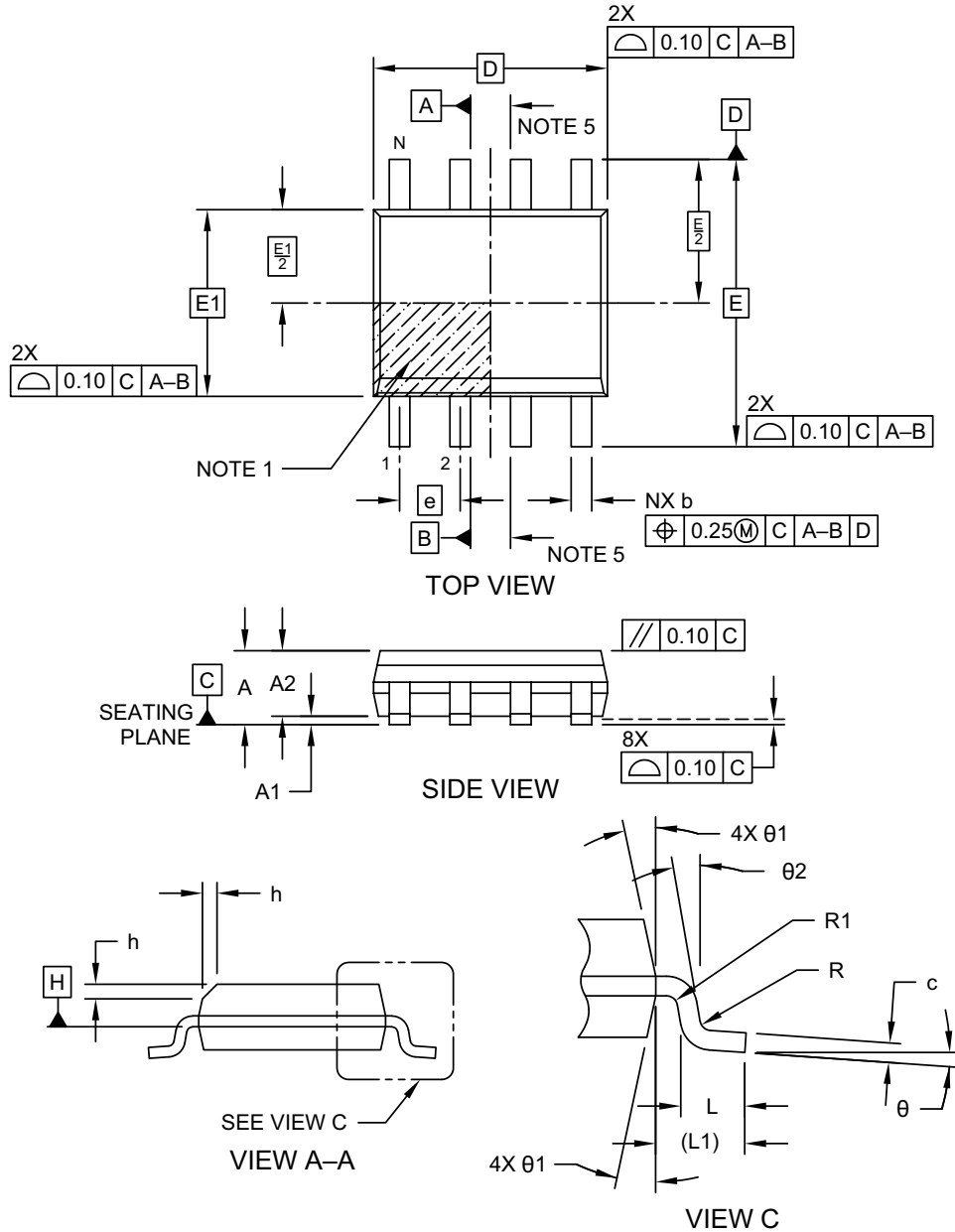
**Note:** If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:

6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;

2 Characters = NN; 1 Character = N

## 8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

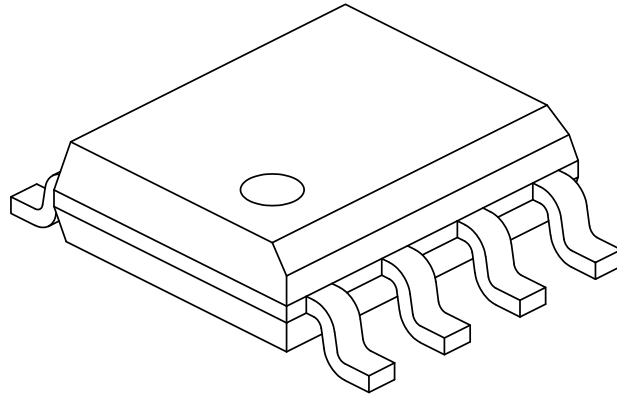


Microchip Technology Drawing No. C04-057-3BX Rev J Sheet 1 of 2

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## 8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

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Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	8°

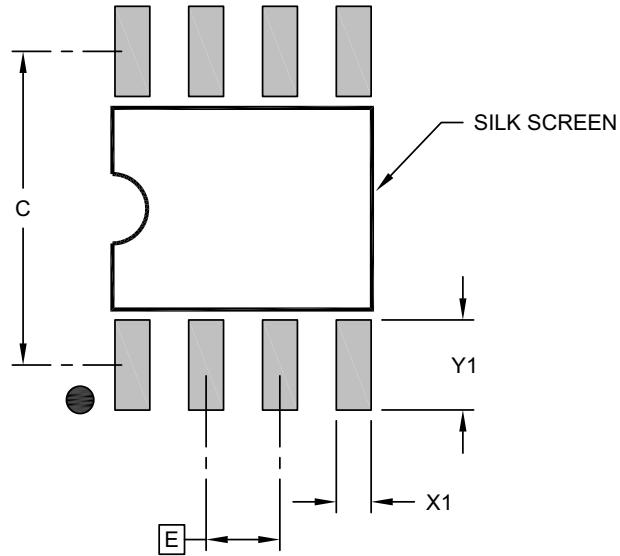
**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-3BX Rev J Sheet 2 of 2

## 8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

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RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C	5.40		
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-3BX Rev J

# MIC4100/1

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NOTES:



## APPENDIX A: REVISION HISTORY

### Revision A (July 2022)

- Converted Micrel document MIC4100/1 to Microchip data sheet DS20006699A.
- Minor text changes throughout.

# MIC4100/1

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>		X	X	-XX
Device	Junction Temperature Range	Package	Media Type	
<b>Device:</b>	MIC4100:	100V Half-Bridge MOSFET Driver 2A Source/Sink Current, CMOS Input		
	MIC4101:	100V Half-Bridge MOSFET Driver 2A Source/Sink Current, TTL Input		
<b>Temperature:</b>	Y =	-40°C to +125°C (RoHS Compliant)		
<b>Package:</b>	M =	8-Lead SOIC		
<b>Media Type:</b>	(blank) =	95/Tube		
	TR =	2,500/Reel		

<b>Examples:</b>	
a) MIC4100YM:	100V Half-Bridge MOSFET Driver 2A Source/Sink Current, CMOS Input, -40°C to +125°C Junction Temperature Range, 8-Lead SOIC, 95/Tube
b) MIC4100YM-TR:	100V Half-Bridge MOSFET Driver 2A Source/Sink Current, CMOS Input, -40°C to +125°C Junction Temperature Range, 8-Lead SOIC, 2,500/Reel
c) MIC4101YM:	100V Half-Bridge MOSFET Driver 2A Source/Sink Current, TTL Input, -40°C to +125°C Junction Temperature Range, 8-Lead SOIC, 95/Tube
b) MIC4101YM-TR:	100V Half-Bridge MOSFET Driver 2A Source/Sink Current, TTL Input, -40°C to +125°C Junction Temperature Range, 8-Lead SOIC, 2,500/Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

# MIC4100/1

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#### India - Pune

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#### Japan - Tokyo

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#### Philippines - Manila

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