PIC18F24/25K42

28-Pin, Low-Power High-Performance High-Temperature Microcontrollers

Description

The PIC18F24/25K42 microcontrollers are available in 28-pin devices. These devices feature a 12-bit ADC with Computation (ADC^2) automating Capacitive Voltage Divider (CVD) techniques for advanced touch sensing, averaging, filtering, oversampling and threshold comparison, Temperature Sensor, Vectored Interrupt Controller with fixed latency for handling interrupts, System Bus Arbiter, Direct Memory Access capabilities, UART with support for Asynchronous, DMX, DALI and LIN transmissions, SPI, I^2C, memory features like Memory Access Partition (MAP) to support customers in data protection and bootloader applications, and Device Information Area (DIA) which stores factory calibration values to help improve temperature sensor accuracy.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - Up to 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Two Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User-programmable source and destination sizes
  - Hardware and software-triggered data transfers
- System Bus Arbiter with User-Configurable Priorities for Scanner and DMA1/DMA2 with Respect to the Main Line and Interrupt Execution
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed interrupt latency
  - Programmable vector table base address
- 31-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - Configurable in hardware or software

Memory

- Up to 128 KB Flash Program Memory
- Up to 8 KB Data SRAM Memory
- Up to 1 KB Data EEPROM
- Memory Access Partition (MAP):
  - Configurable boot and app region sizes with individual write-protections
- Programmable Code Protection
- Device Information Area (DIA) stores:
  - Unique IDs and Device IDs
  - Temp Sensor factory-calibrated data
  - Fixed Voltage Reference calibrated data
- Device Configuration Information (DCI) Stores:
  - Erase row size
  - Number of write latches per row
  - Number of user rows
  - Data EEPROM memory size
  - Pin count

Operating Characteristics

- Operating Voltage Range:
  - 2.7V to 5.5V
- Temperature Range:
  - High-Temp: -40°C to 150°C

Power-Saving Functionality

- Doze mode: Ability to run CPU core slower than the system clock
- Idle mode: Ability to halt CPU core while internal peripherals continue operating
- Sleep mode: Lowest power consumption
- Peripheral Module Disable (PMD):
  - Ability to disable unused peripherals to minimize power consumption

Digital Peripherals

- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT):
  - Hardware monitoring and Fault detection
- Four 16-Bit Timers (TMR0/1/3/5)
- Four Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Three Complementary Waveform Generators (CWGs):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Four Capture/Compare/PWM (CCP) Modules
- Four 10-Bit Pulse-Width Modulators (PWMs)
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control
  - High resolution using 20-bit accumulator and 20-bit increment values
- DSM: Data Signal Modulator:
  - Multiplex two carrier clocks, with glitch prevention feature
  - Multiple sources for each carrier
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for fail-safe operation (e.g., Class B)
  - Calculate CRC over any portion of program memory or data EEPROM
- Two UART Modules:
  - Modules are asynchronous and compatible with RS-232 and RS-485
  - One of the UART modules supports LIN master and slave, DMX-512 mode, DALI gear and device protocols
  - Automatic and user-timed BREAK period generation
  - DMA compatible
  - Automatic checksums
  - Programmable 1, 1.5, and 2 Stop bits
  - Wake-up on BREAK reception
- One SPI Module:
  - Configurable length bytes
  - Configurable length data packets
  - Receive-without-transmit option
  - Transmit-without-receive option
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- Two I^2C Modules, SMBus, PMBus™ Compatible:
  - Supports Standard-mode (100 kHz), Fast-mode (400 kHz) and Fast-mode plus (1 MHz) modes of operation
  - Dedicated address, transmit and receive buffers
  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - Multi-Master mode
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
  - I^2C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
- Device I/O Port Features:
  - 24 I/O pins
  - One input-only pin (RE3)
  - Individually programmable I/O direction, open-drain, slew rate, weak pull-up control
  - Interrupt-on-change (on up to 25 I/O pins)
  - Three external interrupt pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Signal Measurement Timer (SMT):
  - 24-bit timer/counter with prescaler

Analog Peripherals

- Analog-to-Digital Converter with Computation (ADC^2):
  - 12-bit with up to 35 external channels
  - Automated post-processing
  - Automated math functions on input signals: averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
  - Integrated charge pump for improved low-voltage operation
- Hardware Capacitive Voltage Divider (CVD):
  - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
  - Adjustable sample and hold capacitor array
  - Two guard ring output drives
- Temperature Sensor:
  - Internal connection to ADC
  - Can be calibrated for improved accuracy
- Two Comparators:
  - Low-Power/High-Speed mode
  - Fixed Voltage Reference at noninverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 64 MHz
  - ±1% at calibration (nominal)
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External Oscillator Block with:
  - x4 PLL with external sources
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator sources

Note: This document is supplemented by the "*PIC18(L)F24/25K42 Low-Power High Performance Microcontrollers with XLP" Data Sheet* (DS40001869). See Section 1.0, Device Overview.

PIC18(L)F24/25K42 FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (KB)	Data EEPROM (B)	Data SRAM (bytes)	I/O Pins	12-Bit ADC[2] (ch)	5-Bit DAC	Comparator	8-Bit/ (with HLT) /16-Bit Timer	Window Watchdog Timer (WWDT)	Signal Measurement Timer (SMT)	CCP/10-Bit PWM	CWG	NCO	CLC	Zero-Cross Detect	Direct Memory Access (DMA) (ch)	Memory Access Partition	Vectored Interrupts	UART	I^2C/SPI	Peripheral Pin Select	Peripheral Module Disable	Debug (1)
PIC18(L)F24K42	A	16	256	1024	25	24	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I
PIC18(L)F25K42	A	32	256	2048	25	24	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I
PIC18(L)F26K42	B	64	1024	4096	25	24	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I
PIC18(L)F27K42	B	128	1024	8192	25	24	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I
PIC18(L)F45K42	B	32	256	2048	36	35	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I
PIC18(L)F46K42	B	64	1024	4096	36	35	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I
PIC18(L)F47K42	B	128	1024	8192	36	35	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I
PIC18(L)F55K42	B	32	256	2048	44	43	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I
PIC18(L)F56K42	B	64	1024	4096	44	43	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I
PIC18(L)F57K42	B	128	1024	8192	44	43	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	2	2/1	Y	Y	I

Note 1: I – Debugging integrated on chip.

Data Sheet Index:

Unshaded devices are described in this document.

A: DS40001869 PIC18(L)F24/25K42 Data Sheet, 28-Pin

B: DS40001919 PIC18(L)F26/27/45/46/47/55/56/57K42 Data Sheet, 28/40/44/48-Pin

Note: For other small form-factor package availability and marking information, visit **http://www.microchip.com/packaging** or contact your local sales office.

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices, operating in an ambient temperature range between -40°C and 150°C:

- PIC18F24K42
- PIC18F25K42

Note: This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the non-specialty PIC18(L)F24/25K42 devices. For information on the features and specifications shared by this document's high-temperature devices and the non-specialty devices, see the *"PIC18(L)F24/25K42 28-Pin, Low-Power High Performance Microcontrollers with XLP Technology" Data Sheet* (DS40001869).

The PIC18F24/25K42 devices offer the advantages of all PIC18 microcontrollers, namely high computational performance at an economical price, with the addition of high-endurance Program Flash Memory, Universal Asynchronous Receiver Transmitter (UART), Serial Peripheral Interface (SPI), Inter-integrated Circuit (I^2C), Direct Memory Access (DMA), Configurable Logic Cells (CLC), Signal Measurement Timer (SMT), Numerically Controlled Oscillator (NCO), and Analog-to-Digital Converter with Computation (ADC^2).

The primary differentiating features and specifications of the high-temperature PIC18F24/25K42 devices are:

- Above 125°C, the number of program Flash memory and EEPROM programming cycles are significantly reduced (see **Section 2.0 "Electrical Characteristics"**)
- All AC timing specifications are increased by 30%

  This derating factor includes parameters, such as TPWRT
- Maximum HS+PLL frequency of operation (See Table 2-1)

Note 1: The test duration for AEC-Q100 reliability testing for devices operating at 150°C is 1,000 hours. Any design operating at 125°C to 150°C for longer than that period is not warranted without prior written approval from Microchip Technology Inc.

2: Writes are not allowed for Flash program memory above 125°C.

3: The low voltage versions of these devices, PIC18LF24/25K42, are not released for operation above +125°C.

4: Errata Sheet DS80000724 lists various mask revisions. 150°C operation applies only to revisions A4 and later.

2.0 ELECTRICAL CHARACTERISTICS

Note: Other than some basic data, this section documents only the high-temperature PIC18F24/25K42 devices' specifications that differ from those of the non-specialty PIC18F24/25K42 devices. For detailed information on the electrical specifications shared by the high-temperature and non-specialty devices, see the *"*PIC18(L)F24/25K42 *28-Pin, Low-Power High Performance Microcontrollers with XLP Technology" Data Sheet* (DS40001869).

2.1 Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +150°C
Storage temperature ..... -65°C to +155°C
Maximum junction temperature ..... 155°C
Voltage on pins with respect to V_{SS}
- on V_{DD} pin
  - PIC18F24/25K42 ..... -0.3V to +6.5V
  - on $\overline{MCLR}$ pin ..... -0.3V to + 9.0V
  - on all other pins ..... -0.3V to (V_{DD} + 0.3V)

Maximum current
- on V_{SS} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 350 mA
  - 85°C < T_A ≤ +125°C ..... 120 mA
  - 125°C ≤ T_A ≤ +150°C ..... 24 mA
- on V_{DD} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 250 mA
  - 85°C < T_A ≤ +125°C ..... 85 mA
  - 125°C ≤ T_A ≤ +150°C ..... 24 mA
- on any I/O pin ..... ±5 mA

Clamp current, I_K (V_{PIN} < V_{SS} or V_{PIN} > V_{DD}) ..... ±20 mA
Total power dissipation(2) ..... 800 mW

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table XX-Y to calculate device specifications.

2: Power dissipation is calculated as follows:

$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

2.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \le V_{DD} \le V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \le T_A \le T_{A\_MAX}$

V_{DD} — Operating Supply Voltage(1)

PIC18F24/25K42

V_{DDMIN} (Fosc ≤ 32 MHz) ..... +2.7V
V_{DDMIN} (Fosc > 32 MHz) ..... +3.0V
V_{DDMAX} ..... +5.5V

T_A — Operating Ambient Temperature Range

High Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +150°C

Note 1: See Parameter Supply Voltage, DC Characteristics: Supply Voltage (High Temperature).

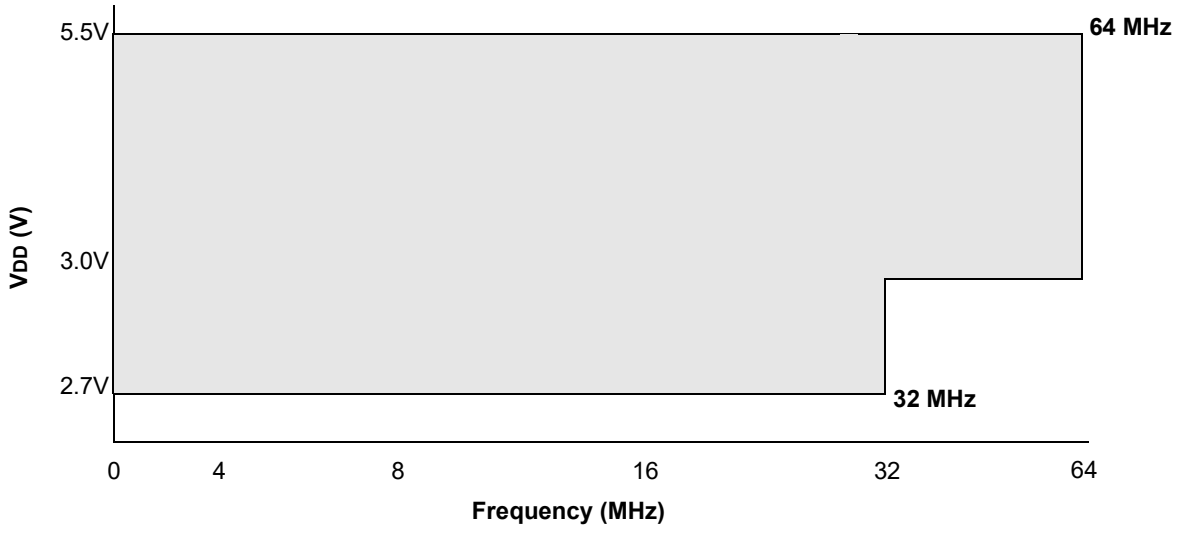
2.3 DC Characteristics

TABLE 2-1: SUPPLY VOLTAGE (HIGH TEMPERATURE)

PIC18F24/25K42			Standard Operating Conditions (unless otherwise stated)				
Param No.	**Symbol**	**Characteristic**	**Min. +150°C**	**Typ.†**	**Max. +150°C**	**Units**	**Conditions**
Supply Voltage							
D002	V_{DD}		2.7 3.0	— —	5.5 5.5	V	$F_{OSC} \le 32$ MHz $F_{OSC} > 32$ MHz

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 2-1: VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +150°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

TABLE 2-2: DC CHARACTERISTICS: SUPPLY CURRENT (I_{DD})(1,2)

PIC18F24/25K42			Standard Operating Conditions (unless otherwise stated)			
			Max. +150°C	Units	Conditions	
Param No.	Symbol	Device Characteristic			V_{DD}	Notes
D100	IDD_{XT4}	XT = 4 MHz	1400	uA	3.0V	
D101	IDD_{HFO16}	HFINTOSC = 16 MHz	4.5	mA	3.0V	
D102	IDD_{HFOPLL}	HFINTOSC = 64 MHz	16.3	mA	3.0V	
D103	$IDD_{HSPLL64}$	HS+PLL = 64 MHz	15.3	mA	3.0V	
D104	IDD_{IDLE}	Idle mode, HFINTOSC = 16 MHz	3.5	mA	3.0V	

Note 1: The test conditions for all I_{DD} measurements in Active-Operation mode are: OSC1: external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; $\overline{MCLR}$=V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

TABLE 2-3: DC CHARACTERISTICS: POWER-DOWN CURRENTS (I_{PD})(1,2,3)

PIC18F24/25K42			Standard Operating Conditions (unless otherwise stated) VREPGM = 1			
			Max. +150°C	Units	Conditions	
Param No.	Symbol	Device Characteristic			V_{DD}	Notes
D200	I_{PD}	I_{PD} Base	39.0	uA	3.0V	
D200A			71.0	uA	3.0V	VREGPM=0
D201	I_{PD_WDT}	Low Frequency Internal Oscillator/ WDT	40.0	uA	3.0V	
D202	I_{PD_SOSC}	Secondary Oscillator (SOSC)	41.0	uA	3.0V	
D203	I_{PD_FVR}	FVR	96.0	uA	3.0V	
D204	I_{PD_BOR}	Brown-out Reset (BOR)	48.0	uA	3.0V	
D206	I_{PD_HLVD}	High/Low-Voltage Detect (HLVD)	48.0	uA	3.0V	
D207	I_{PD_ADCA}	ADC – Non-converting	39.0	uA	3.0V	ADC not converting(4)
D208	I_{PD_CMP}	Comparator	76.0	uA	3.0V	High-powering mode

Note 1: The peripheral current is the sum of the base I_{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by substracting the base I_{DD} or I_{PD} current from this limit. Max. values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.

4: ADC clock source is ADCRC.

TABLE 2-4: MEMORY SPECIFICATIONS (150°C)

Param. No.	Sym.	Characteristic	Min. +150°C	Typ.†	Max. +150°C	Units	Conditions
Data EEPROM Memory Specifications							
MEM20	E_D	DataEE Byte Endurance	1k	—	—	E/W	$125°C \leq T_A \leq 150°C$
Program Flash Memory Specifications							
MEM30	E_P	Flash Memory Cell Endurance	100	—	—	E/W	$125°C \leq T_A \leq 150°C$

† Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2.4 AC Characteristics

TABLE 2-5: INTERNAL OSCILLATOR PARAMETERS(1)

PIC18F24/25K42			Standard Operating Conditions (unless otherwise stated)				
Param No.	Symbol	Device Characteristic	Min. +150°C	Typ.†	Max. +150°C	Units	Conditions
OS50	FHFOSC	Precision Calibrated HFINTOSC Frequency	— — — — — —	4 8 12 16 48 64	— — — — — —	MHz	See Figure 3-2
OS51	FHFOSCLP	Low-Power Optimized HFINTOSC Frequency	0.85 1.70	1 2	1.15 2.30	MHz	-40°C to 150°C
OS53*	FLFOSC	Internal LFINTOSC Frequency	23.25	31	38.75	kHz	-40°C to 150°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

FIGURE 3-2: PRECISION-CALIBRATED HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE

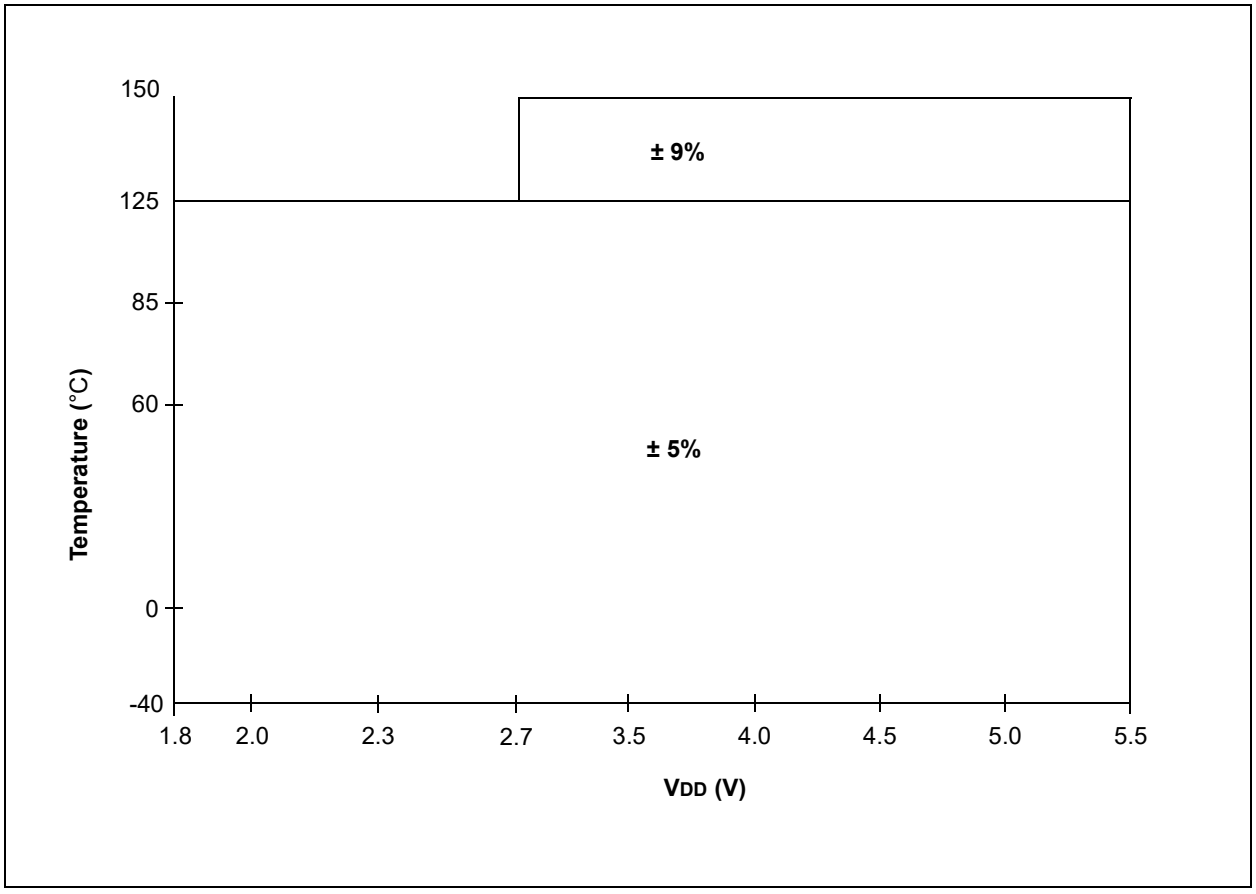


TABLE 2-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT TIMER AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

PIC18F24/25K42			Standard Operating Conditions (unless otherwise stated)				
Param No.	Symbol	Device Characteristic	Min. +150°C	Typ.†	Max. +150°C	Units	Conditions(1)
RST06	VBOR	Brown-out Reset Voltage	2.56 2.43	2.85 2.7	3.14 2.97	V	BORV = 00 BORV = 01

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Do not use BORV = 10 and 11 for High-Temperature operation (125°C ≤ TA ≤ 150°C).

TABLE 2-7: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Param. No.	Sym.	Characteristic	Min. +150°C	Typ.†	Max. +150°C	Units	Conditions(1)
HLVD01	VDET	Voltage Detection	2.45	2.75	3.05	V	HLVDSEL[3:0] = 0101
			2.58	2.90	3.22	V	HLVDSEL[3:0] = 0110
			2.80	3.15	3.50	V	HLVDSEL[3:0] = 0111
			2.98	3.35	3.72	V	HLVDSEL[3:0] = 1000
			3.20	3.60	4.00	V	HLVDSEL[3:0] = 1001
			3.34	3.75	4.16	V	HLVDSEL[3:0] = 1010
			3.56	4.00	4.44	V	HLVDSEL[3:0] = 1011
			3.74	4.20	4.66	V	HLVDSEL[3:0] = 1100
			3.87	4.35	4.83	V	HLVDSEL[3:0] = 1101
			4.14	4.65	5.16	V	HLVDSEL[3:0] = 1110

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Do not use HLVDSEL[3:0] = 0000 through 0100 for High-Temperature operation (125°C ≤ TA ≤ 150°C).

TABLE 2-8: FIXED VOLTAGE REFERENCE (FVR) SPECIFICATIONS

PIC18F24/25K42			Standard Operating Conditions (unless otherwise stated)				
Param. No.	Symbol	Characteristic	Min. +150°C	Typ.†	Max. +150°C	Units	Conditions
FVR01	VFVR1	1x Gain (1.024V)	-9	—	+9	%	VDD ≥ 2.7V, -40°C to 150°C
FVR02	VFVR2	2x Gain (2.048V)	-9	—	+9	%	VDD ≥ 2.7V, -40°C to 150°C
FVR03	VFVR4	4x Gain (4.096V)	-9	—	+9	%	VDD ≥ 4.75V, -40°C to 150°C

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

APPENDIX A: REVISION HISTORY

Revision A (02/2020)

Original mini data sheet for the high-temperature devices in the PIC18F24/25K42 devices.

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Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX	XXX
Device	Tape and Reel Option	Temperature Range	Package	Pattern

Device:	PIC18F24K42 PIC18F25K42	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	H	= -40°C to +150°C (High Temperature)
Package:	SS 5N	= SSOP = VQFN with Wettable Flanks
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC18F25K42-H/P: Part number: PIC18F25K42, Tape and Reel Option: Blank, Temperature Range: H, Package: P, Pattern: Blank

b) PIC18F25K42T-H/ST: Part number: PIC18F25K42, Tape and Reel Option: T, Temperature Range: H, Package: ST, Pattern: Blank

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

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