SST49LF008A

8-Mbit Firmware Hub

Features

- Firmware Hub for Intel 8xx Chipsets
- 8-Mbit SuperFlash® Memory Array for Code/Data Storage:
  - 1024K x 8
- Flexible Erase Capability:
  - Uniform 4-KByte sectors
  - Uniform 64-KByte overlay blocks
  - 64-KByte top boot block protection
  - Chip Erase for PP mode only
- • Single 3.0V-3.6V Read and Write Operations
- Superior Reliability:
  - Endurance: 100,000 cycles (typical)
  - Greater than 100 years data retention
- Low-Power Consumption:
  - Active Read current: 6 mA (typical)
  - Standby current: 10 µA (typical)
- Fast Sector Erase/Byte Program Operation:
  - Sector Erase time: 18 ms (typical)
  - Block Erase time: 18 ms (typical)
  - Chip Erase time: 70 ms (typical)
  - Byte Program time: 14 µs (typical)
  - Chip Rewrite time: 15 seconds (typical)
  - Single-pulse program or erase
  - Internal timing generation
- Two Operational Modes:
  - Firmware Hub Interface (FWH) mode for In-System operation
  - Parallel Programming (PP) mode for fast production programming
- Firmware Hub Hardware Interface Mode:
  - Five-signal communication interface supporting byte read and write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write-protect for entire chip and/or top Boot Block
  - Block Locking Register for all blocks
  - Standard SDP Command set
  - Data# Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
  - 4 ID pins for multichip selection
- Parallel Programming (PP) Mode:
  - 11-pin multiplexed address and 8-pin data I/O interface
  - Supports fast In-System or PROM programming for manufacturing
- CMOS and PCI I/O Compatibility
- All Non-Pb (lead-free) Devices are RoHS Compliant

Packages

- 32-Lead PLCC
- 32-Lead TSOP (8 mm x 14 mm)
- Non-Pb (Lead-Free) Packages Available

Product Description

The SST49LF008A Flash memory devices are designed to be read compatible with the Intel® 82802 Firmware Hub (FWH) device for PC BIOS application. These devices provide protection for the storage and update of code and data in addition to adding system design flexibility through five general purpose inputs. Two interface modes are supported by the SST49LF008A:

- Firmware Hub (FWH) Interface mode for in-system programming
- Parallel Programming (PP) mode for fast factory programming of PC BIOS applications

The SST49LF008A Flash memory devices are manufactured with Microhip's proprietary, high-performance SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST49LF008A devices significantly improve performance and reliability, while lowering power consumption.

The SST49LF008A devices write (Program or Erase) with a single 3.0V-3.6V power supply. They use less energy during Erase and Program than alternative Flash memory technologies. The total energy consumed is a function of the applied voltage, current and time of application.

Since for any given voltage range, the SuperFlash® technology uses less current to program and has a shorter erase time, the total energy consumed during any erase or program operation is less than alternative Flash memory technologies.

The SST49LF008A products provide a maximum Byte Program time of 20 µsec. The entire memory can be erased and programmed byte-by-byte, typically in 15 seconds when using status detection features such as Toggle Bit or Data# Polling to indicate the completion of Program operation.

The SuperFlash® technology provides fixed erase and program times independent of the number of erase/program cycles performed. Therefore, the system software or hardware does not have to be calibrated or correlated to the cumulated number of erase/program cycles as is necessary with alternative Flash memory technologies, whose erase and program time increase with accumulated erase/program cycles.

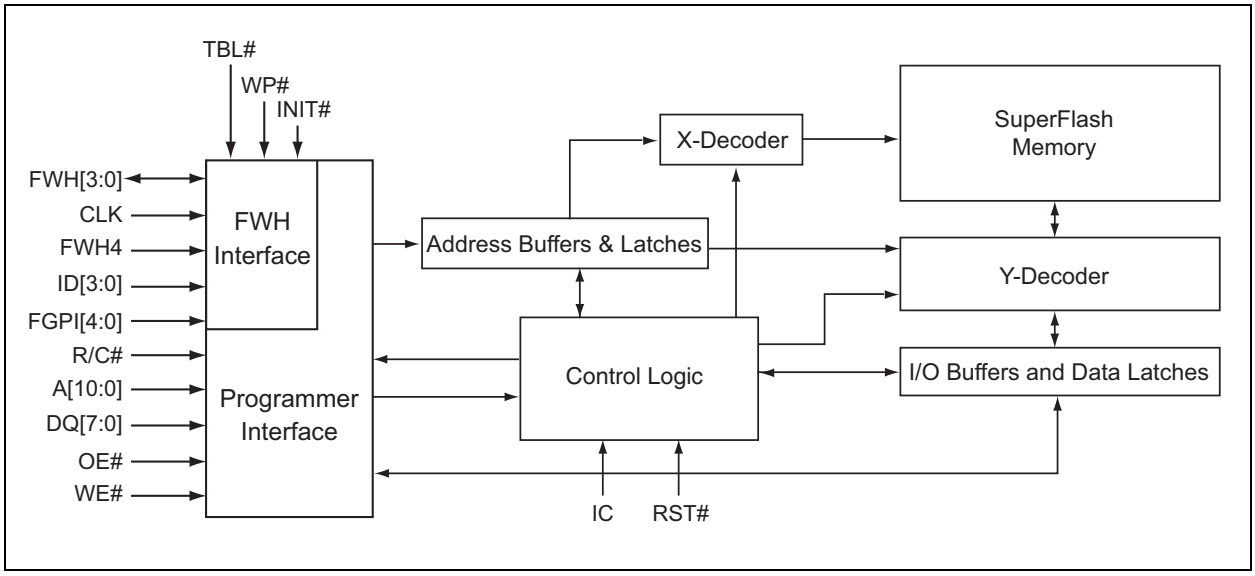
To protect against inadvertent write, the SST49LF008A devices employ hardware and software data (SDP) protection schemes. It is offered with typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

To meet high-density, surface mount requirements, the SST49LF008A devices are offered in 32-lead PLCC and 32-lead TSOP packages.

See Figure 2-1 for pin assignments and Table 2-1 for pin descriptions.

1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: PIN DESCRIPTIONS

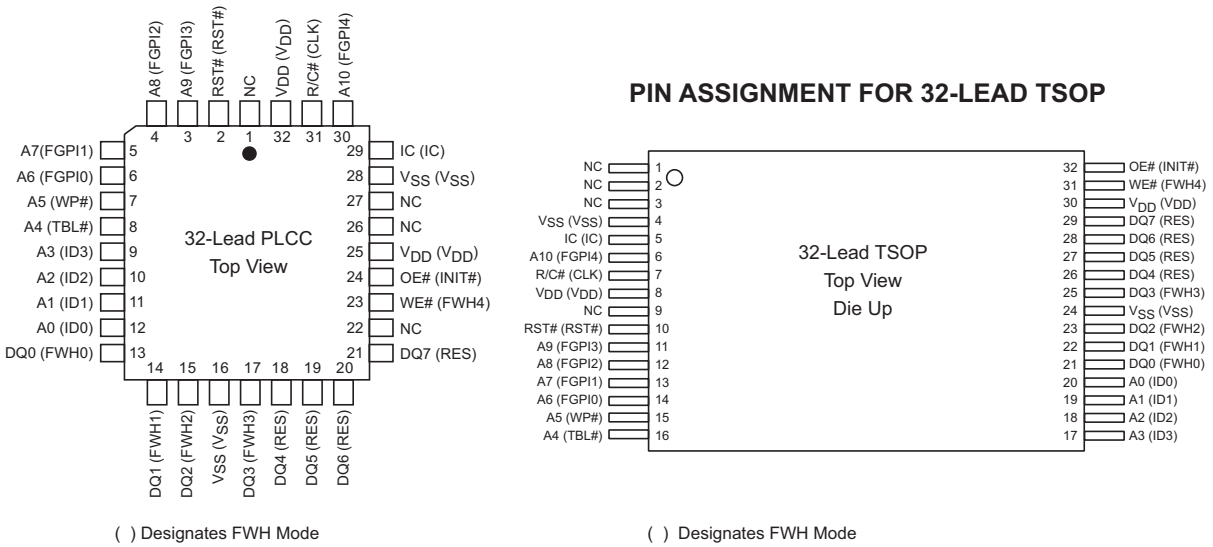


TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	32-Lead PLCC	32-Lead TSOP	Type[1]	Interface		Functions
					PP	FWH	
NC	No Connection	1	1	I	X	X	Unconnected pins
RST# (RST#)	Reset	2	10	I	X	X	Reset the operation of the device
A9 (FGPI3)	Address	3	11	I	X		Input for low-order addresses during read and write operations. Addresses are internally latched during a write cycle. For the programming interface, these addresses are latched by R/C# and share the same pins as the high-order address inputs.
A8 (FGPI2)		4	12				
A7 (FGPI1)		5	13				
A6 (FGPI0)		6	14				
A5 (WP#)		7	15				
A4 (TBL#)		8	16				
A3 (ID3)		9	17				
A2 (ID2)		10	18				
A1 (ID1)		11	19				
A0 (ID0)		12	20				

Note 1: I = Input, O = Output

TABLE 2-1: PIN DESCRIPTION (CONTINUED)

Symbol	Pin Name	32-Lead PLCC	32-Lead TSOP	Type[1]	Interface		Functions
					PP	FWH	
DQ0 (FWH0)	Data	13	21	I/O	X		Output data during read cycles and receive input data during write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# is high.
DQ1 (FWH1)		14	22				
DQ2 (FWH2)		15	23				
VSS (VSS)	Ground	16	4	PWR	X	X	Circuit ground (OV reference). All VSS pins must be grounded.
DQ3 (FWH3)	Data	17	25	I/O	X		Output data during read cycles and receive input data during write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# is high.
DQ4 (RES)		18	26				
DQ5 (RES)		19	27				
DQ6 (RES)		20	28				
DQ7 (RES)		21	29				
NC	No Connection	22	2	I	X	X	Unconnected pins
WE# (FWH4)	FWH Input	23	31	I		X	Input communications
OE# (INIT#)	Initialize	24	32	I		X	This is the second RESET pin for in-system use. This pin is internally combined with the RST# pin. If this pin or RST# pin is driven low, identical operation is exhibited.
VDD (VDD)	Power Supply	25	8	PWR	X	X	Provide power supply (3.0V-3.6V)
NC	No Connection	26	3	I	X	X	Unconnected pins
NC		27	9				
VSS (VSS)	Ground	28	24	PWR	X	X	Circuit ground (OV reference). All VSS pins must be grounded.
IC (IC)	Interface Configuration Pin	29	5	I	X	X	This pin determines which interface is operational. When held high, Programmer mode is enabled and when held low, FWH mode is enabled. This pin must be setup at power-up or before return from Reset and not change during device operation. This pin is internally pulled down with a resistor between 20 kΩ-100 kΩ.
A10 (FGPI4)	Address	30	6	I	X		Input for low-order addresses during read and write operations. Addresses are internally latched during a write cycle. For the programming interface, these addresses are latched by R/C# and share the same pins as the high-order address inputs.

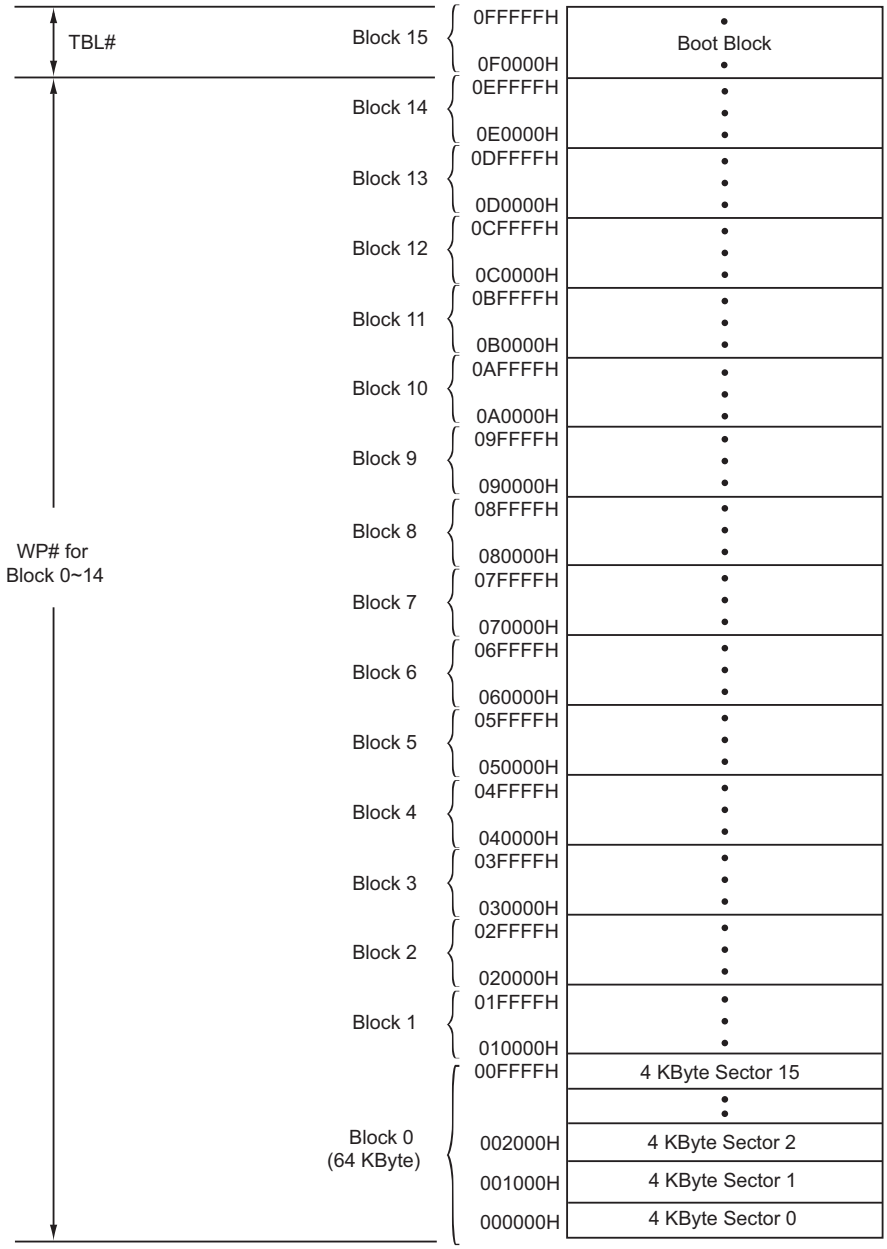
Note 1: I = Input, O = Output

TABLE 2-1: PIN DESCRIPTION (CONTINUED)

Symbol	Pin Name	32-Lead PLCC	32-Lead TSOP	Type[1]	Interface		Functions
					PP	FWH	
R/C# (CLK)	Row/Column Select	31	7	I	X		Select for the programming interface, this pin determines whether the address pins are pointing to the row addresses or to the column addresses.
VDD (VDD)	Power Supply	32	30	PWR	X	X	Provide power supply (3.0V-3.6V)

Note 1: I = Input, O = Output

Device Memory Map



3.0 DESIGN CONSIDERATIONS

Microchip recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} less than 1 cm away from the V_{DD} pin of the device. Additionally, a low-frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 1 cm of the V_{DD} pin. If you use a socket for programming purposes, add an additional 1 µF-10 µF next to each socket.

The RST# pin must remain stable at V_{IH} for the entire duration of an erase operation. WP# must remain stable at V_{IH} for the entire duration of the erase and program operations for non-Boot Block sectors. To write data to the top Boot Block sectors, the TBL# pin must also remain stable at V_{IH} for the entire duration of the erase and program operations.

4.0 PRODUCT IDENTIFICATION

The product identification mode identifies the device as the SST49LF008A and manufacturer as Microchip.

TABLE 4-1: PRODUCT IDENTIFICATION

	Byte	Data	JEDEC ID Address Location
Manufacturer's ID	0000H	BFH	FFBC0000H
Device ID	0001H	5AH	FFBC0001H

5.0 MODE SELECTION

The SST49LF008A Flash memory devices can operate in two distinct interface modes:

- Firmware Hub Interface (FWH) mode
- Parallel Programming (PP) mode

The Interface Configuration (IC) pin is used to set the Interface mode selection. If the IC pin is set to logic high, the device is in PP mode; if the IC pin is set to low, the device is in the FWH mode. The IC selection pin must be configured prior to device operation. The IC pin is internally pulled down if the pin is not connected.

In FWH mode, the device is configured to interface with its host using Intel® Firmware Hub proprietary protocol. Communication between Host and the SST49LF008A occurs via the 4-bit I/O communication signals, FWH[3:0] and the FWH4.

In PP mode, the device is programmed via an 11-bit address and an 8-bit data I/O parallel signals. The address inputs are multiplexed in row and column selected by control signal R/C# pin. The column addresses are mapped to the higher internal addresses and the row addresses are mapped to the lower internal addresses. See Device Memory Map for address assignments.

6.0 FIRMWARE HUB (FWH) MODE

6.1 Device Operation

The FWH mode uses a 5-signal communication interface, FWH[3:0] and FWH4, to control operations of the SST49LF008A. Operations such as Memory Read and Memory Write uses Intel® FWH proprietary protocol. JEDEC® Standard Software Data Protection (SDP) Byte Program, Sector Erase and Block Erase command sequences are incorporated into the FWH memory cycles. Chip Erase is only available in PP mode.

The device enters Standby mode when FWH4 is high and no internal operation is in progress. The device is in ready mode when FWH4 is low and no activity is on the FWH bus.

6.2 Firmware Hub Interface Cycles

Addresses and data are transferred to and from the SST49LF008A by a series of "fields" where each field contains 4 bits of data. SST49LF008A supports only single-byte read and write and all fields are one-clock cycle in length. Field sequences and contents are strictly defined for read and write operations.

Addresses in this section refer to addresses as seen from the SST49LF008A's "point of view," some calculation will be required to translate these to the actual locations in the memory map (and vice versa) if multiple memory devices are used on the bus. Table 6-1 and Table 6-2 list the field sequences for read and write cycles.

TABLE 6-1: FWH READ CYCLE

Clock Cycle	Field Name	Field Contents FWH[3:0](1)	FWH[3:0] Direction	Comments
1	START	1101	IN	FWH4 must be active (low) for the part to respond. Only the last start field (before FWH4 transitions high) should be recognized. The START field contents indicate a FWH memory Read cycle.
2	IDSEL	0000 to 1111	IN	Indicates which FWH device should respond. If the to IDSEL (ID select) field matches the value ID[3:0], then that particular device will respond to the whole bus cycle.
3-9	IMADDR	YYYY	IN	These seven clock cycles make up the 28-bit memory address. YYYY is one nibble of the entire address. Addresses are transferred most significant nibble first.
10	IMSIZE	0000 (1 byte)	IN	A field of this size indicates how many bytes will be or transferred during multi-byte operations. The SST49LF008A will only support single-byte operation. IMSIZE = 0000b
11	TAR0	1111	IN then Float	In this clock cycle, the master (Intel ICH) has driven the bus then float to all '1's and then floats the bus, prior to the next clock cycle. This is the first part of the bus "turnaround cycle".
12	TAR1	1111 (float)	Float then OUT	The SST49LF008A takes control of the bus during this cycle. During the next clock cycle, it will be driving "sync data".
13	RSYNC	0000 (READY)	OUT	During this clock cycle, the FWH will generate a "ready-sync" (RSYNC) indicating that the least significant nibble of the least significant byte will be available during the next clock cycle.
14	DATA	YYYY	OUT	YYYY is the least significant nibble of the least significant data byte.
15	DATA	YYYY	OUT	YYYY is the most significant nibble of the least significant data byte.
16	TAR0	1111	OUT then Float	In this clock cycle, the SST49LF008A has driven the bus to all ones and then floats the bus prior to the next clock cycle. This is the first part of the bus "turnaround cycle".
17	TAR1	1111 (float)	Float then IN	The master (Intel ICH) resumes control of the bus during this cycle.

Note 1: Field contents are valid on the rising edge of the present clock cycle.

FIGURE 6-1: SINGLE BYTE READ WAVEFORMS

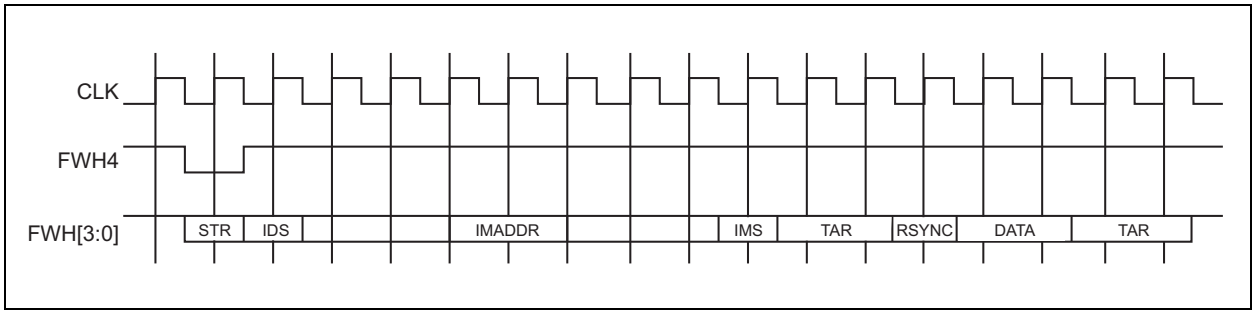
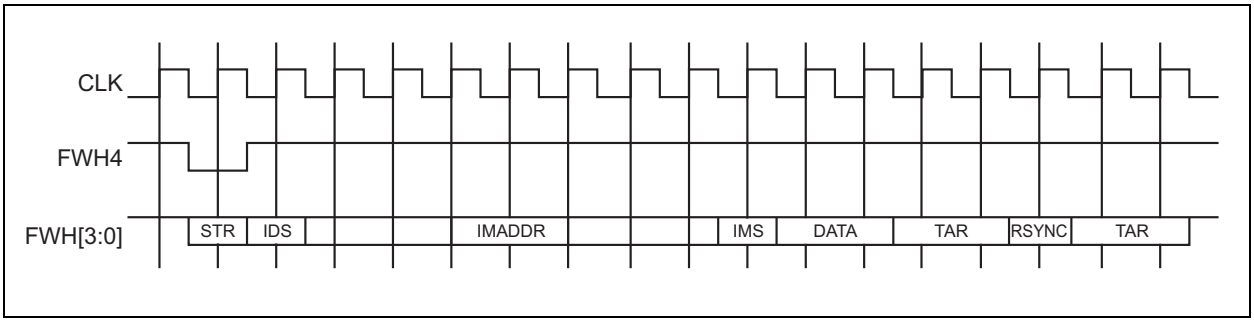


TABLE 6-2: FWH WRITE CYCLE

Clock Cycle	Field Name	Field Contents FWH[3:0](1)	FWH[3:0] Direction	Comments
1	START	1110	IN	FWH4 must be active (low) for the part to respond. Only the last start field (before FWH4 transitions high) should be recognized. The START field contents indicate a FWH memory Read cycle.
2	IDSEL	0000 to 1111	IN	Indicates which SST49LF008A device should respond. If the IDSEL (ID select) field matches the value ID[3:0], then that particular device will respond to the whole bus cycle.
3-9	IMADDR	YYYY	IN	These seven clock cycles make up the 28-bit memory address. YYYY is one nibble of the entire address. Addresses are transferred most significant nibble first.
10	IMSIZE	0000 (1 byte)	IN	This size field indicates how many bytes will be transferred during multibyte operations. The FWH only supports single byte writes. IMSIZE = 0000b
11	DATA	YYYY	IN	This field is the least significant nibble of the data byte. This data is either the data to be programmed into the Flash memory or any valid Flash command.
12	DATA	YYYY	IN	This field is the most significant nibble of the data byte.
13	TAR0	1111	IN then Float	In this clock cycle, the master (Intel ICH) has driven the bus then float to all '1's and then floats the bus, prior to the next clock cycle. This is the first part of the bus "turnaround cycle".
14	TAR1	1111 (float)	Float then OUT	The SST49LF008A takes control of the bus during this cycle. During the next clock cycle it will be driving the "sync" data.
15	RSYNC	0000	OUT	The SST49LF008A outputs the values 0000, indicating that it has received data or a Flash command.
16	TAR0	1111	OUT then Float	In this clock cycle, the SST49LF008A has driven the bus to all ones and then floats the bus prior to the next clock cycle. This is the first part of the bus "turnaround cycle".
17	TAR1	1111 (float)	Float then IN	The master (Intel ICH) resumes control of the bus during this cycle.

Note 1: Field contents are valid on the rising edge of the present clock cycle.

FIGURE 6-2: WRITE WAVEFORMS



6.3 Abort Mechanism

If FWH4 is driven low for one or more clock cycles during a FWH cycle, the cycle will be terminated and the device will wait for the ABORT command. The host may drive the FWH[3:0] with '1111b' (ABORT command) to return the device to Ready mode.

If abort occurs during a write operation, the data may be incorrectly altered.

6.4 Response to Invalid Fields

During FWH operations, the FWH will not explicitly indicate that it has received invalid field sequences.
The response to specific invalid fields or sequences is as follows:

Address out of range:

The FWH address sequence is 7-field long (28 bits), but only the last five address fields (20 bits) will be decoded by SST49LF008A. Address A_{22} has the special function of directing reads and writes to the Flash core (A_{22} = 1) or to the register space (A_{22} = 0).

Invalid IMSIZE field:

If the FWH receives an invalid size field during a read or write operation, the device will reset and no operation will be attempted. The SST49LF008A will not generate any kind of response in this situation. Invalid-size fields for a Read/Write cycle are anything but 0000b.

6.5 Device Memory Hardware Write Protection

The Top Boot Lock (TBL#) and Write-Protect (WP#) pins are provided for hardware write protection of device memory in the SST49LF008A. The TBL# pin is used to write protect 16 boot sectors (64 Kbyte) at the highest Flash memory address range for the SST49LF008A. WP# pin write protects the remaining sectors in the Flash memory.

An active-low signal at the TBL# pin prevents program and erase operations of the top boot sectors. When TBL# pin is held high, write protection of the top boot sectors is then determined by the Boot Block Locking register. The WP# pin serves the same function for the remaining sectors of the device memory. The TBL# and WP# pins write protection functions operate independently of one another.

Both TBL# and WP# pins must be set to their required protection states prior to starting a program or erase operation. A logic level change occurring at the TBL# or WP# pin during a program or erase operation could cause unpredictable results. TBL# and WP# pins cannot be left unconnected.

TBL# is internally OR'ed with the top Boot Block Locking register. When TBL# is low, the top Boot Block is hardware write-protected regardless of the state of the Write Lock bit for the Boot Block Locking register. Clearing the Write-Protect bit in the register when TBL# is low will have no functional effect, even though the register may indicate that the block is no longer locked.

WP# is internally OR'ed with the Block Locking register. When WP# is low, the blocks are hardware write-protected regardless of the state of the Write Lock bit for the corresponding Block Locking registers. Clearing the Write-Protect bit in any register when WP# is low will have no functional effect, even though the register may indicate that the block is no longer locked.

6.6 Reset

A V_{IL} on INIT# or RST# pin initiates a device Reset. INIT# and RST# pins have the same function internally. It is required to drive INIT# or RST# pins low during a system Reset to ensure proper CPU initialization. During a read operation, driving INIT# or RST# pins low deselects the device and places the output drivers, FWH[3:0], in a high-impedance state. The Reset signal must be held low for a minimal duration of time T_{RSTP}. A Reset latency will occur if a Reset procedure is performed during a program or erase operation (see Table 10-10 for more information). A device Reset during an active program or erase will abort the operation and memory contents may become invalid due to data being altered or corrupted from an incomplete erase or program operation.

6.7 Write Operation Status Detection

The SST49LF008A device provides two software means to detect the completion of a write (program or erase) cycle, in order to optimize the system write cycle time. The software detection includes two STATUS bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6).

The End-of-Write detection mode is incorporated into the FWH Read cycle. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

6.8 Data# Polling (DQ_7)

When the SST49LF008A device is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal write operation, the remaining data outputs may still be invalid; valid data on the entire data bus will appear in subsequent successive read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. Proper status will not be given using Data# Polling if the address is in the invalid range.

6.9 Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating '0's and '1's, i.e., toggling between '0' and '1'. When the internal Program or Erase operation is completed, the toggling will stop.

6.10 Multiple Device Selection

The four ID pins, ID[3:0], allow multiple devices to be attached to the same bus by using different ID strapping in a system. When the SST49LF008A is used as a boot device, ID[3:0] must be strapped as 0000; all subsequent devices should use a sequential up-count strapping (i.e. 0001, 0010, 0011 etc.).

The SST49LF008A will compare the strapping values; if there is a mismatch, the device will ignore the remainder of the cycle and go into Standby mode. For further information regarding FWH device mapping and paging, refer to the Intel® 82801(ICH) I/O Controller Hub documentation. Since there is no ID support in PP mode, to program multiple devices a stand-alone PROM programmer is recommended.

7.0 REGISTERS

There are three types of registers available on the SST49LF008A: the General Purpose Inputs register, Block Locking registers and the JEDEC ID registers. These registers appear at their respective address location in the 4 GB system memory map. Unused register locations will read as 00H. Attempts to read or write to any registers during internal write operations will be ignored.

7.1 General Purpose Inputs Register

The General Purpose Inputs register (GPI_REG) passes the state of FGPI[4:0] pins at power-up on the SST49LF008A. It is recommended that the FGPI[4:0] pins are in the desired state before FWH4 is brought low for the beginning of the bus cycle and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. The GPI register for the boot device appears at FFBC0100H in the 4 GB system memory map and will appear elsewhere if the device is not the boot device. Register is not available for read when the device is in erase/program operation. See Table 7-1 for the GPI_REG bits and function.

TABLE 7-1: GENERAL PURPOSE INPUTS REGISTER

Bit	Function	Pin #	
		32-LD PLCC	32-LD TSOP
7:5	Reserved	—	—
4	FGPI[4] Reads status of general purpose input pin	30	6
3	FGPI[3] Reads status of general purpose input pin	3	11
2	FGPI[2] Reads status of general purpose input pin	4	12
1	FGPI[1] Reads status of general purpose input pin	5	13
0	FGPI[0] Reads status of general purpose input pin	6	14

7.2 Block Locking Registers

SST49LF008A provides software controlled lock protection through a set of Block Locking registers.

The Block Locking registers are read/write registers and it is accessible through standard addressable memory locations specified in Table 7-2. Unused register locations will read as 00H.

TABLE 7-2: BLOCK LOCKING REGISTERS FOR SST49LF008A(1)

Register	Block Size	Protected Memory Address Range	Memory Map Register Address
T_BLOCK_LK	64K	0FFFFFH-0F0000H	FFBF0002H
T_MINUS01_LK	64K	0EFFFFH-0E0000H	FFBE0002H
T_MINUS02_LK	64K	0DFFFFH-0D0000H	FFBD0002H
T_MINUS03_LK	64K	0CFFFFH-0C0000H	FFBC0002H
T_MINUS04_LK	64K	0BFFFFH-0B0000H	FFBB0002H
T_MINUS05_LK	64K	0AFFFFH-0A0000H	FFBA0002H
T_MINUS06_LK	64K	09FFFFH-090000H	FFB90002H
T_MINUS07_LK	64K	08FFFFH-080000H	FFB80002H
T_MINUS08_LK	64K	07FFFFH-070000H	FFB70002H
T_MINUS09_LK	64K	06FFFFH-060000H	FFB60002H

Note 1: Default value at power up is 01H.

TABLE 7-2: BLOCK LOCKING REGISTERS FOR SST49LF008A[1] (Continued)

Register	Block Size	Protected Memory Address Range	Memory Map Register Address
T_MINUS10_LK	64K	05FFFFH-050000H	FFB50002H
T_MINUS11_LK	64K	04FFFFH-040000H	FFB40002H
T_MINUS12_LK	64K	03FFFFH-030000H	FFB30002H
T_MINUS13_LK	64K	02FFFFH-020000H	FFB20002H
T_MINUS14_LK	64K	01FFFFH-010000H	FFB10002H
T_MINUS15_LK	64K	00FFFFH-000000H	FFB00002H

Note 1: Default value at power up is 01H.

TABLE 7-3: BLOCK LOCKING REGISTER BITS

Reserved Bit[7...2]	Lock-Down Bit[1]	Write Lock Bit	Lock Status
000000	0	0	Full Access
000000	0	1	Write Locked (Default State at Power-Up)
000000	1	0	Locked Open (Full Access Locked Down)
000000	1	1	Write Locked Down

7.3 Write Lock

The Write Lock bit, bit 0, controls the lock state described in Table 7-3. The default Write status of all blocks after power-up is write locked. When bit 0 of the Block Locking register is set, Program and Erase operations for the corresponding block are prevented. Clearing the Write Lock bit will unprotect the block. The Write Lock bit must be cleared prior to starting a program or erase operation since it is sampled at the beginning of the operation.

The Write Lock bit functions in conjunction with the hardware Write Lock pin TBL# for the top Boot Block. When TBL# is low, it overrides the software locking scheme. The top Boot Block Locking register does not indicate the state of the TBL# pin.

The Write Lock bit functions in conjunction with the hardware WP# pin for blocks 0 to 6. When WP# is low, it overrides the software locking scheme. The Block Locking register does not indicate the state of the WP# pin.

7.4 Lock Down

The Lock Down bit, bit 1, controls the Block Locking register as described in Table 7-3. When in the FWH interface mode, the default Lock Down status of all blocks upon power-up is not locked down. Once the Lock Down bit is set, any future attempted changes to that Block Locking register will be ignored. The Lock Down bit is only cleared upon a device Reset with RST# or INIT# or power down. Current Lock Down status of a particular block can be determined by reading the corresponding Lock-Down bit.

Once a block's Lock Down bit is set, the Write Lock bits for that block can no longer be modified and the block is locked down in its current state of write accessibility.

7.5 JEDEC ID Registers

The JEDEC ID registers for the boot device appear at FFBC0000H and FFBC0001H in the 4 GB system memory map and will appear elsewhere if the device is not the boot device. Register is not available for read when the device is in Erase/Program operation. Unused register location will read as 00H. Refer to the relevant application note for details. See Table 4-1 for the device ID code.

8.0 PARALLEL PROGRAMMING MODE

8.1 Device Operation

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#. During the software command sequence the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#.

8.2 Reset

A V_{IL} on RST# pin initiates a device Reset.

8.3 Read

The Read operation of the SST49LF008A device is controlled by OE#. OE# is the output control and is used to gate data from the output pins. Refer to Figure 10-6 for further details.

8.4 Byte Program Operation

The SST49LF008A device is programmed on a byte-by-byte basis. Before programming, one must ensure that the sector in which the byte which is being programmed exists is fully erased. The Byte Program operation is initiated by executing a four-byte command load sequence for Software Data Protection with address (BA) and data in the last byte sequence. During the Byte Program operation, the row address (A_{10}-A_0) is latched on the falling edge of R/C# and the column Address (A_{21}-A_{11}) is latched on the rising edge of R/C#. The data bus is latched in the rising edge of WE#. The Program operation, once initiated, will be completed within 20 µs. See Figure 10-7 for Program operation timing diagram, Figure 10-10 for timing waveforms and Figure 10-18 for its flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

8.5 Sector Erase Operation

The Sector Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 Kbytes. The Sector Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector Erase command (30H) and sector address (SA) in the last bus cycle. The internal Erase operation begins after the sixth WE# pulse.

The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods (see Figure 10-11 for Sector Erase timing waveforms). Any commands written during the Sector Erase operation will be ignored.

8.6 Block Erase Operation

The Block Erase operation allows the system to erase the device in 64 KByte uniform block size for the SST49LF008A. The Block Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Block Erase command (50H) and block address. The internal Block Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods (see Figure 10-12 for timing waveforms). Any commands written during the Block Erase operation will be ignored.

8.7 Chip Erase

The SST49LF008A device provides a Chip Erase operation only in PP mode, which allows the user to erase the entire memory array to the '1's state. This is useful when the entire device must be quickly erased.

The Chip Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE#. During the internal Erase operation, the only valid read is Toggle bit or Data# Polling. See Table 9-1 for the command sequence, Figure 10-13 for timing diagram and Figure 10-21 for the flowchart. Any commands written during the Chip Erase operation will be ignored.

8.8 Write Operation Status Detection

The SST49LF008A device provides two software means to detect the completion of a write (program or erase) cycle, in order to optimize the system Write cycle time. The software detection includes two STATUS bits: Data# Polling (DQ_7) and Toggle bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

8.9 Data# Polling (DQ_7)

When the SST49LF008A device is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid; valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# pulse for Program operation. For Sector or Chip Erase, the Data# Polling is valid after the rising edge of sixth WE# pulse.

See Figure 10-8 for Data# Polling timing diagram and Figure 10-19 for a flowchart. Proper status will not be given using Data# Polling if the address is in the invalid range.

8.10 Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle bit is valid after the rising edge of fourth WE# pulse for Program operation. For Sector, Block or Chip Erase, the Toggle bit is valid after the rising edge of sixth WE# pulse. See Figure 10-9 for Toggle Bit timing diagram and Figure 10-19 for a flowchart.

TABLE 8-1: OPERATION MODES SELECTION (PP MODE)

Mode	RST#	OE#	WE#	DQ	Address
Read	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Program	V_{IH}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Erase	V_{IH}	V_{IH}	V_{IL}	X(1)	Sector or Block Address, XXH for Chip Erase
Reset	V_{IL}	X	X	High-Z	X
Write Inhibit	V_{IH}	V_{IL}	X	High-Z/D_{OUT}	X
	X	X	V_{IH}	High-Z/D_{OUT}	X
Product Identification	V_{IH}	V_{IL}	V_{IH}	Manufacturer's ID (BFH) Device ID(2)	A18 - A1 = V_{IL}, A0 = V_{IL} A18 - A1 = V_{IL}, A0 = V_{IH}

Note 1: X can be V_{IL} or V_{IH}, but no other value.

2: Device ID = 5AH for SST49LF008A.

9.0 DATA PROTECTION

The SST49LF008A device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

9.1 Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a write cycle.

VDD Power-Up/Power-Down Detection: The Write operation is inhibited when VDD is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

9.2 Software Data Protection (SDP)

SST49LF008A provides the JEDEC® approved Software Data Protection scheme for all data alteration operation, i.e., Program and Erase. Any program operation requires the inclusion of a series of three-byte sequences. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down.

Any erase operation requires the inclusion of a six-byte load sequence. The SST49LF008A device is shipped with the Software Data Protection permanently enabled. See Table 9-1 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode, within TRC.

TABLE 9-1: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Write Cycle[1]		2nd Write Cycle[1]		3rd Write Cycle[1]		4th Write Cycle[1]		5th Write Cycle[1]		6th Write Cycle[1]	
	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA[3]	Data	—	—	—	—
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SAx[4]	30H
Block Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BAx[5]	50H
Chip Erase[6]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[7,8]	5555H	AAH	2AAAH	55H	5555H	90H	—	—	—	—	—	—
Software ID Exit[9]	XXH	F0H	—	—	—	—	—	—	—	—	—	—
Software ID Exit[9]	5555H	AAH	2AAAH	55H	5555H	F0H	—	—	—	—	—	—

Note 1: FWH mode uses consecutive write cycles to complete a command sequence; PP mode uses consecutive bus cycles to complete a command sequence.

2: Address format A_{14}-A_0 (Hex), Addresses A_{21}-A_{15} can be VIL or VIH, but no other value, for the Command sequence in PP mode.

3: BA = Program Byte Address

4: SAx for Sector Erase Address

5: BAx for Block Erase Address

6: Chip Erase is supported in PP mode only.

7: Manufacturer's ID = BFH is read with A_0 = 0,
With A_{19}-A_1 = 0; 49LF008A Device ID = 5AH is read with A_0 = 1.

8: The device does not remain in Software Product ID mode if powered down.

9: Both Software ID Exit operations are equivalent.

10.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

DC voltage on any pin to ground potential ..... -0.5V to V_{DD} + 0.5V

Transient voltage (<20 ns) on any pin to ground potential(1) ..... -2.0V to V_{DD} + 2.0V

Package power dissipation capability (T_A = +25°C) 1.0W

Surface mount solder reflow temperature(2) ..... +260°C for 10 seconds

Output short circuit current(3) ..... 50 mA

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Do not violate processor or chipset limitations on the INIT# pin.

2: Excluding certain with-Pb 32-PLCC units, all packages are +260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of +240°C for 10 seconds (contact the factory for the latest information).

3: Output shorted for no more than one second. No more than one output shorted at a time. This note applies to non-PCI outputs.

The AC and DC specifications for the FWH Interface signals (FWH[3:0], CLK, FWH4 and RST#) as defined in Section 4.2.2 of the ***PCI Local Bus Specification, Rev. 2.1***. Refer to Table 10-3 for the DC voltage and current specifications.

Refer to the tables in **Section 10.0 "Electrical Specifications"** for the AC timing specifications for Clock, Read/Write and Reset operations.

TABLE 10-1: OPERATING RANGE

Range	Ambient Temp.	V_{DD}
Commercial	0°C to +85°C	3.0V-3.6V

TABLE 10-2: AC CONDITIONS OF TEST(1,2)

Input Rise/Fall Time	Output Load
3 ns	C_L = 30 pF

Note 1: See Figures 10-16 and 10-17.

2: FWH interface signals use PCI load test conditions.

TABLE 10-3: DC OPERATING CHARACTERISTICS (ALL INTERFACES)(1)

Symbol	Parameter	Limits		Unit	Test Conditions(1)
		Min.	Max.		
I_{DD}	Active V_{DD} Current	—	—		LCLK (FWH mode) and Address Input (PP mode) = V_{ILT}/V_{IHT} at f = 33 MHz (FWH mode) or 1/T_{RC} MIN (PP Mode) All other inputs = V_{IL} or V_{IH}
	Read	—	12	mA	All outputs = open, V_{DD} = V_{DD} maximum
	Write(2)	—	24	mA	**Note 3**

TABLE 10-3: DC OPERATING CHARACTERISTICS (ALL INTERFACES)(1) (Continued)

Symbol	Parameter	Limits		Unit	Test Conditions(1)
		Min.	Max.		
I_{SB}	Standby V_{DD} Current (FWH Interface)	—	100	µA	LCLK (FWH mode) and Address Input (PP mode) = V_{ILT}/V_{IHT} at f = 33 MHz (FWH mode) or 1/$T_{RC\ MIN}$ (PP Mode) LFRAME# = 0.9 V_{DD}, f = 33 MHz, CE# = 0.9 V_{DD}, V_{DD} = V_{DD} maximum All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_{RY}(4)	Ready Mode V_{DD} Current (FWH Interface)	—	10	mA	LCLK (FWH mode) and Address Input (PP mode) = V_{ILT}/V_{IHT} at f = 33 MHz (FWH mode) or 1/$T_{RC\ MIN}$ (PP Mode) LFRAME# = V_{IL}, f = 33 MHz, V_{DD} = V_{DD} maximum All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_I	Input Current for IC, ID [3:0] Pins	—	200	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} maximum
I_{LI}	Input Leakage Current	—	1	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} maximum
I_{LO}	Output Leakage Current	—	1	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} maximum
I_{IHI}(5)	INIT# Input High Voltage	1.0	V_{DD} + 0.5	V	V_{DD} = V_{DD} maximum
I_{ILI}(5)	INIT# Input Low Voltage	-0.5	0.4	V	V_{DD} = V_{DD} minimum
I_{IL}	Input Low Voltage	-0.5	0.3 V_{DD}	V	V_{DD} = V_{DD} minimum
I_{IH}	Input High Voltage	0.5 V_{DD}	V_{DD} + 0.5	V	V_{DD} = V_{DD} minimum
I_{OL}	Output Low Voltage	—	0.1 V_{DD}	V	I_{OL} = 1500 µA, V_{DD} = V_{DD} minimum
I_{OH}	Output High Voltage	0.9 V_{DD}	—	V	I_{OH} = 500 µA, V_{DD} = V_{DD} minimum

Note 1: Test conditions apply to PP mode.

2: I_{DD} active while Erase or Program is in progress.

3: For PP Mode: OE# = WE# = V_{IH}; For FWH mode: f = 1/$T_{RC\ MIN}$, LFRAME# = V_{IH}, CE# = V_{IL}.

4: The device is in Ready Mode when no activity is on the FWH bus.

5: Do not violate processor or chipset specification regarding INIT# voltage.

TABLE 10-4: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU\text{-}READ}$(1)	Power-Up to Read Operation	100	µs
$T_{PU\text{-}WRITE}$(1)	Power-Up to Write Operation	100	µs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10-5: PIN IMPEDANCE(1)

Parameter	Description	Test Condition	Units
$C_{I/O}$(2)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	12 pF
L_{PIN}(3)	Pin Inductance	—	20 nH

Note 1: V_{DD} = 3.3V, T_A = +25°C, f = 1 MHz, other pins open.

2: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

3: Refer to PCI specifications.

TABLE 10-6: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Unit	Test Method
N_{END}(1)	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard A78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10-7: CLOCK TIMING PARAMETERS

Symbol	Parameter	Minimum	Maximum	Units
T_{CYC}	CLK Cycle Time	30	—	ns
T_{HIGH}	CLK High Time	11	—	ns
I_{LOW}	CLK Low Time	11	—	ns
	CLK Slew Rate (peak-to-peak)	1	4	V/ns
	RST# or INIT# Slew Rate	50	—	mV/ns

FIGURE 10-1: CLK WAVEFORM

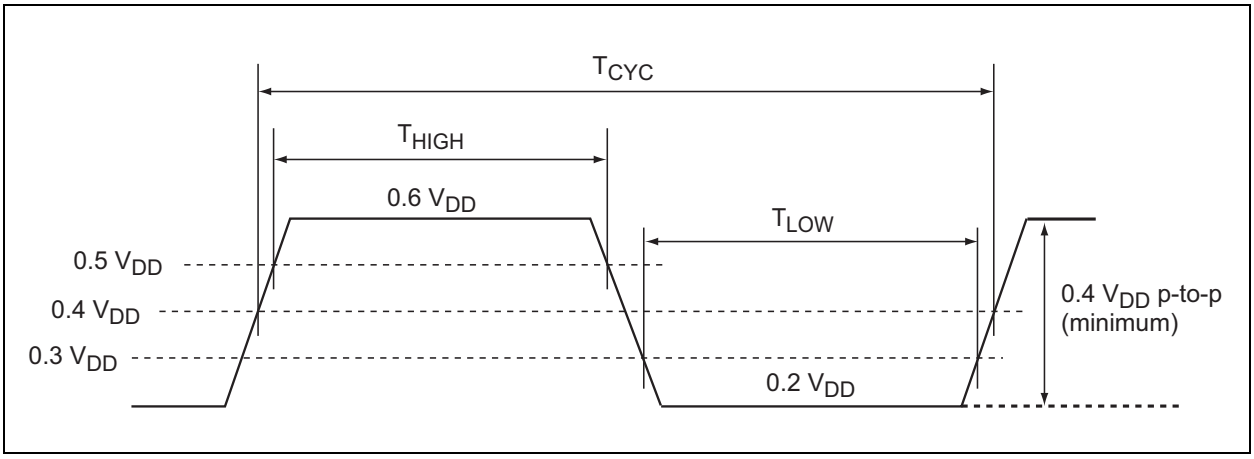


TABLE 10-8: AC OPERATING CHARACTERISTICS (FWH MODE)

Symbol	Parameter	Minimum	Maximum	Units
T_{CYC}	Clock Cycle Time	30	—	ns
T_{SU}	Data Set-Up Time to Clock Rising	7	—	ns
T_{DH}	Clock Rising to Data Hold Time	0	—	ns
T_{VAL}(1)	Clock Rising to Data Valid	2	11	ns
T_{BP}	Byte Programming Time	—	20	µs
T_{SE}	Sector Erase Time	—	25	ms
T_{BE}	Block Erase Time	—	25	ms
T_{SCE}	Chip Erase Time	—	100	ms
T_{ON}	Clock Rising to Active (Float to Active Delay)	2	—	ns
T_{OFF}	Clock Rising to Inactive (Active to Float Delay)	—	28	ns

Note 1: Minimum and maximum times have different loads. See PCI specifications.

TABLE 10-9: AC INPUT/OUTPUT SPECIFICATIONS (FWH MODE)(1)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{OH}(AC)	Switching Current High	-12 V_{DD}	—	mA	0 < V_{OUT} ≤ 0.3 V_{DD}
		-17.1 (V_{DD} - V_{OUT})	—	mA	0.3 V_{DD} < V_{OUT} < 0.9 V_{DD}
		—	Equation C(2)	—	0.7 V_{DD} < V_{OUT} < V_{DD}
	(Test Point)	—	-32 V_{DD}	mA	V_{OUT} = 0.7 V_{DD}
I_{OL}(AC)	Switching Current Low	16 V_{DD}	Equation C(2)	mA	V_{DD} > V_{OUT} ≥ 0.6 V_{DD}
		26.7 V_{OUT}	—	mA	0.6 V_{DD} > V_{OUT} > 0.1 V_{DD}
		—	—	—	0.18 V_{DD} > V_{OUT} > 0
	(Test Point)	—	38 V_{DD}	mA	V_{OUT} = 0.18 V_{DD}
I_{CL}	Low Clamp Current	-25 + (V_{IN} + 1)/0.015	—	mA	-3 < V_{IN} ≤ -1
I_{CH}	High Clamp Current	25 + (V_{IN} - V_{DD} - 1)/0.015	—	mA	V_{DD} + 4 > V_{IN} ≤ V_{DD} +1
slewr(3)	Output Rise Slew Rate	1	4	V/ns	0.2 V_{DD} - 0.6 V_{DD} load
slewr(3)	Output Fall Slew Rate	1	4	V/ns	0.6 V_{DD} - 0.2 V_{DD} load

Note 1: V_{DD} = 3.0V-3.6V

2: See PCI specifications.

3: PCI specification output load is used.

TABLE 10-10: RESET TIMING PARAMETERS (FWH MODE)(1)

Symbol	Parameter	Min.	Max.	Units
T_{PRST}	V_{DD} Stable to Reset Low	1	—	ms
T_{KRST}	Clock Stable to Reset Low	100	—	µs
T_{RSTP}	RST# Pulse Width	100	—	ns
T_{RSTF}	RST# Low to Output Float	—	48	ns
T_{RST}(2)	RST# High to FWH4 Low	1	—	µs
T_{RSTE}	RST# Low to Reset during Sector/Block Erase or Program	—	10	µs

Note 1: V_{DD} = 3.0V-3.6V

2: There will be a latency of T_{RSTE} if a Reset procedure is performed during a program or erase operation.

FIGURE 10-2: RESET TIMING DIAGRAM

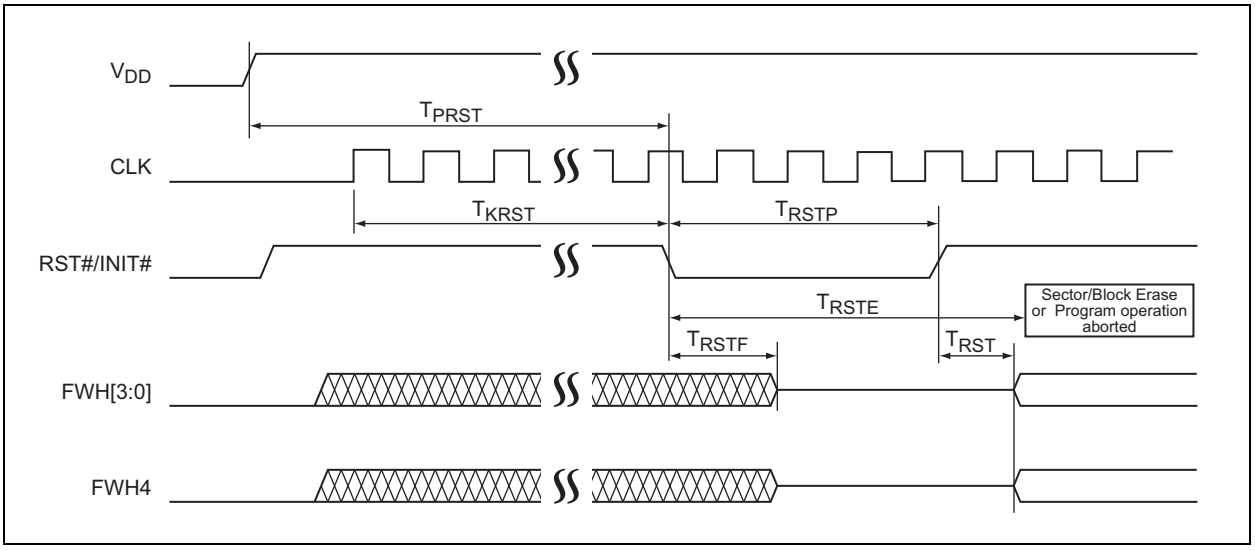


FIGURE 10-3: OUTPUT TIMING PARAMETERS

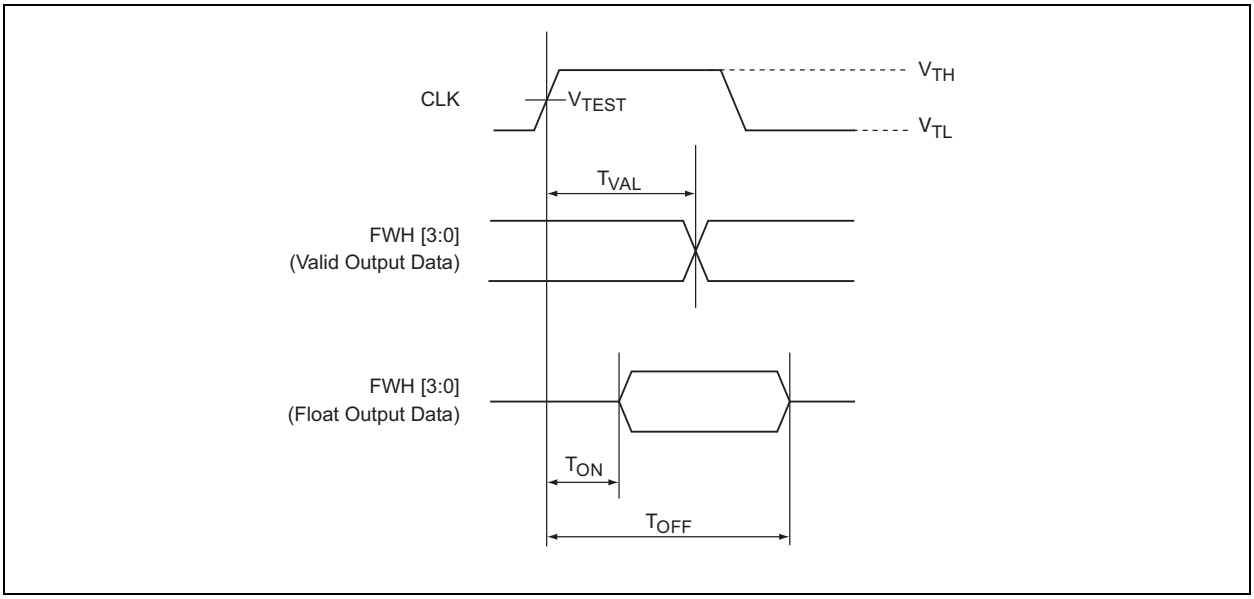


FIGURE 10-4: INPUT TIMING PARAMETERS

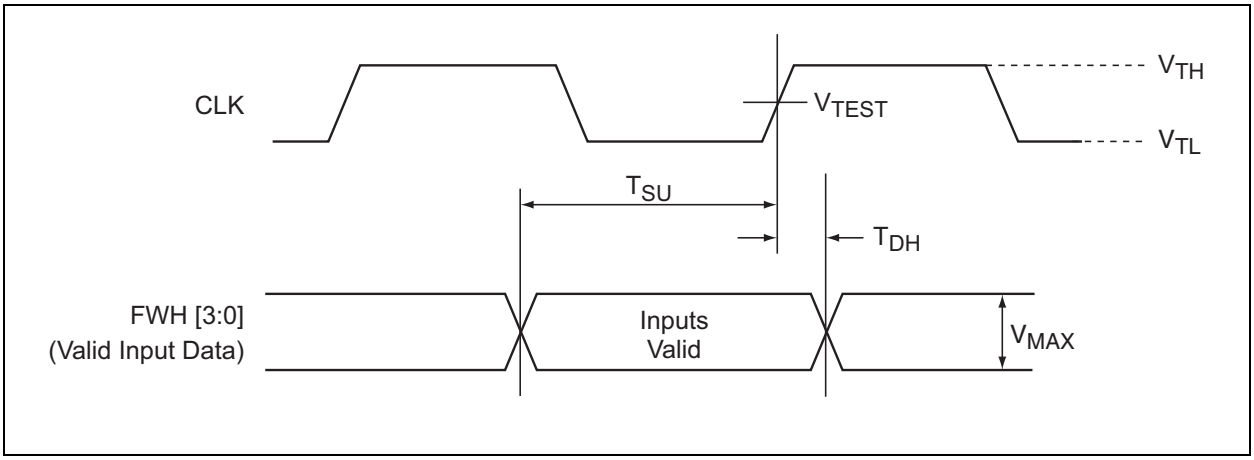


TABLE 10-11: INTERFACE MEASUREMENT CONDITION PARAMETERS

Symbol	Value	Units
V_{TH}(1)	0.6 V_{DD}	V
V_{TL}(1)	0.2 V_{DD}	V
V_{TEST}	0.4 V_{DD}	V
V_{MAX}(1)	0.4 V_{DD}	V
Input Signal Edge Rate	1 V/ns	V

Note 1: The input test environment is done with 0.1 V_{DD} of overdrive over V_{IH} and V_{IL}. Timing parameters must be met with no more overdrive than this.
V_{MAX} specified the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values but must correlate results back to these parameters.

TABLE 10-12: READ CYCLE TIMING PARAMETERS (PP MODE)(1)

Symbol	Parameter	Min.	Max.	Units
TRC	Read Cycle Time	270	—	ns
TRST	RST# High to Row Address Setup	1	—	µs
TAS	R/C# Address Set-Up Time	45	—	ns
TAH	R/C# Address Hold Time	45	—	ns
TAA	Address Access Time	—	120	ns
TOE	Output Enable Access Time	—	60	ns
TOLZ	OE# Low to Active Output	0	—	ns
TOHZ	OE# High to High-Z Output	—	35	ns
TOH	Output Hold from Address Change	0	—	ns

Note 1: VDD = 3.0V-3.6V

TABLE 10-13: PROGRAM/ERASE CYCLE TIMING PARAMETERS (PP MODE)(1)

Symbol	Parameter	Min.	Max.	Units
TRST	RST# High to Row Address Setup	1	—	µs
TAS	R/C# Address Setup Time	50	—	ns
TAH	R/C# Address Hold Time	50	—	ns
TCWH	R/C# to Write Enable High Time	50	—	ns
TOES	OE# High Setup Time	20	—	ns
TOEH	OE# High Hold Time	20	—	ns
TOEP	OE# to Data# Polling Delay	—	40	ns
TOET	OE# to Toggle Bit Delay	—	40	ns
TWP	WE# Pulse Width	100	—	ns
TWPH	WE# Pulse Width High	100	—	ns
TDS	Data Setup Time	50	—	ns
TDH	Data Hold Time	5	—	ns
TIDA	Software ID Access and Exit Time	—	150	ns
TBP	Byte Programming Time	—	20	µs
TSE	Sector Erase Time	—	25	ms
TBE	Block Erase Time	—	25	ms
TSCE	Chip Erase Time	—	100	ms

Note 1: VDD = 3.0V-3.6V

TABLE 10-14: RESET TIMING PARAMETERS (PP MODE)(1)

Symbol	Parameter	Min.	Max.	Units
TPRST	VDD Stable to Reset Low	1	—	ms
TRSTP	RST# Pulse Width	100	—	ns
TRSTF	RST# Low to Output Float	—	48	ns
TRST(2)	RST# High to Row Address Setup	1	—	µs
TRSTE	RST# Low to Reset during Sector/Block Erase or Program	—	10	µs
TRSTC	RST# Low to Reset during Chip Erase	—	50	µs

Note 1: VDD = 3.0V-3.6V

2: There will be a Reset latency of TRSTE or TRSTC if a Reset procedure is performed during a Program or Erase operation.

FIGURE 10-5: RESET TIMING DIAGRAM (PP MODE)

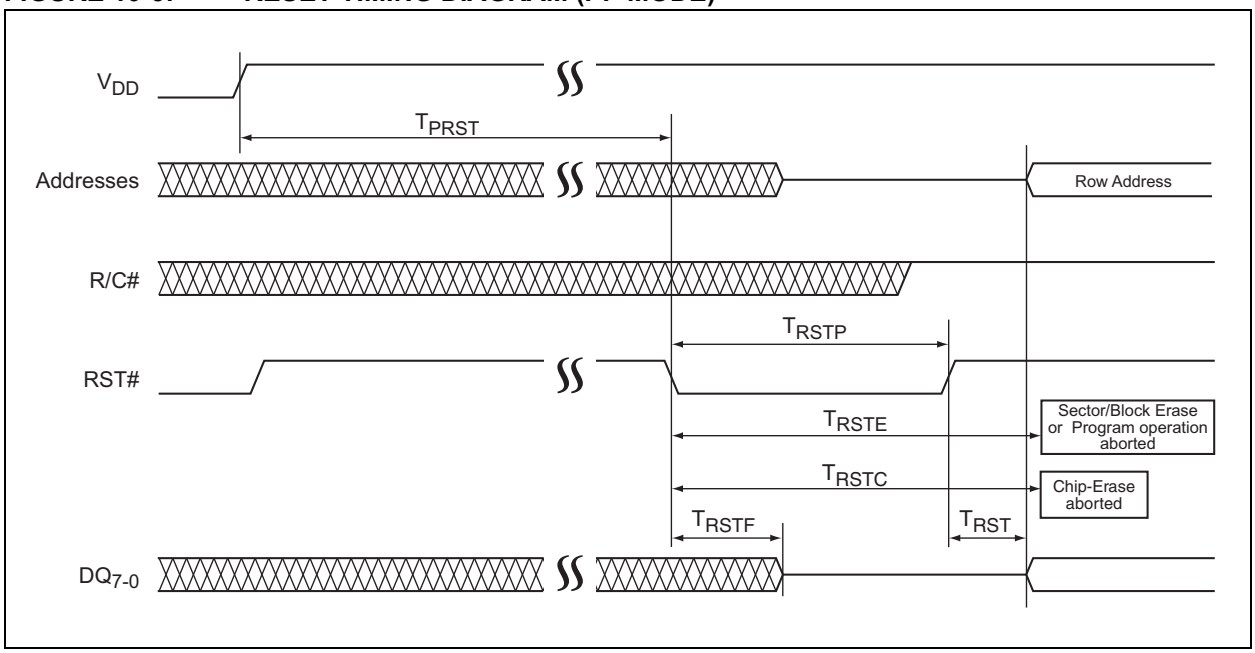


FIGURE 10-6: READ CYCLE TIMING DIAGRAM (PP MODE)

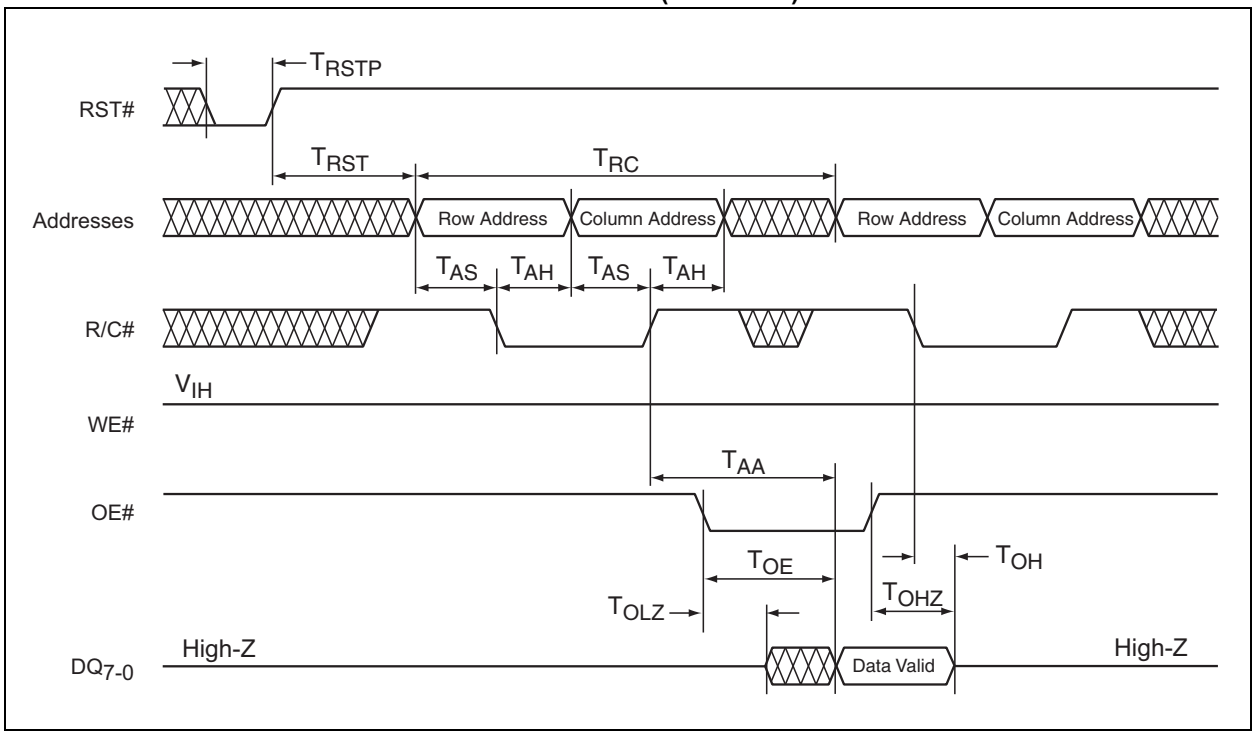


FIGURE 10-7: WRITE CYCLE TIMING DIAGRAM (PP MODE)

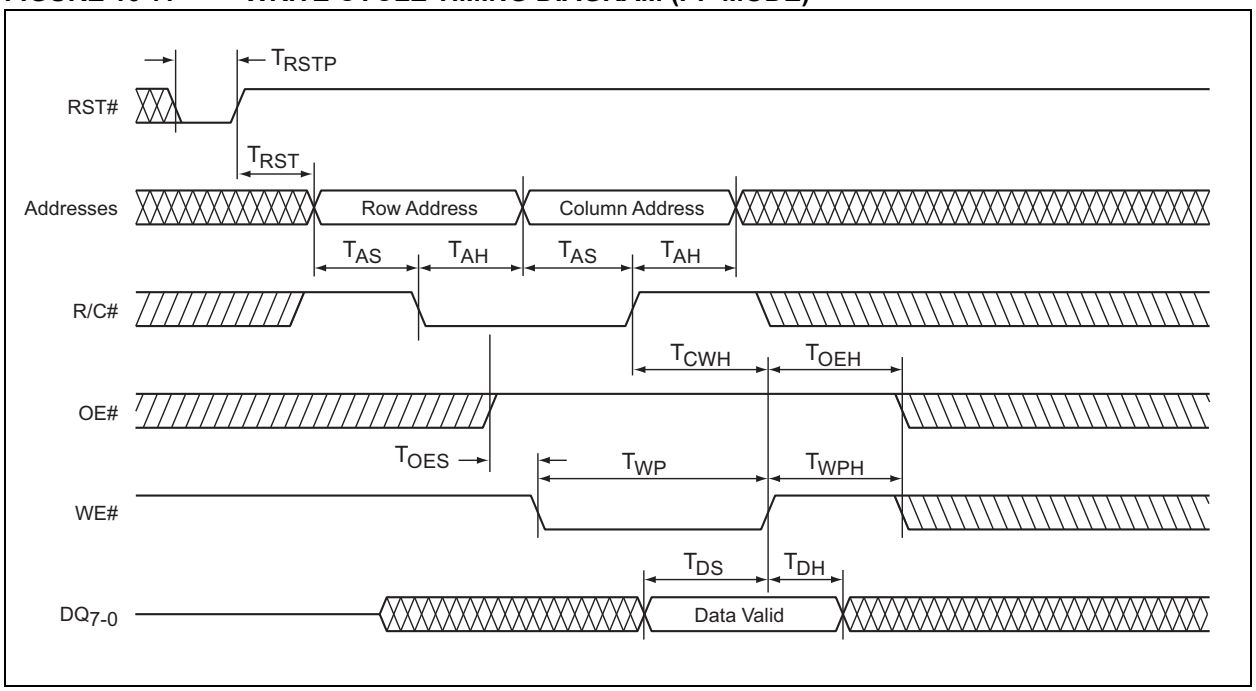


FIGURE 10-8: DATA# POLLING TIMING DIAGRAM (PP MODE)

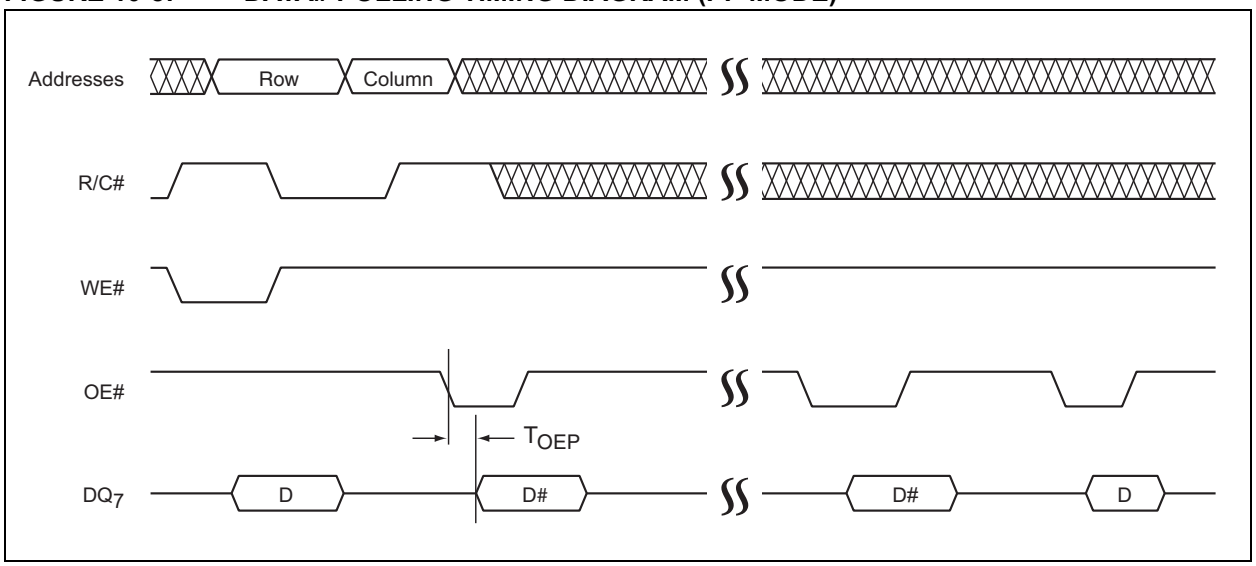


FIGURE 10-9: TOGGLE BIT TIMING DIAGRAM (PP MODE)

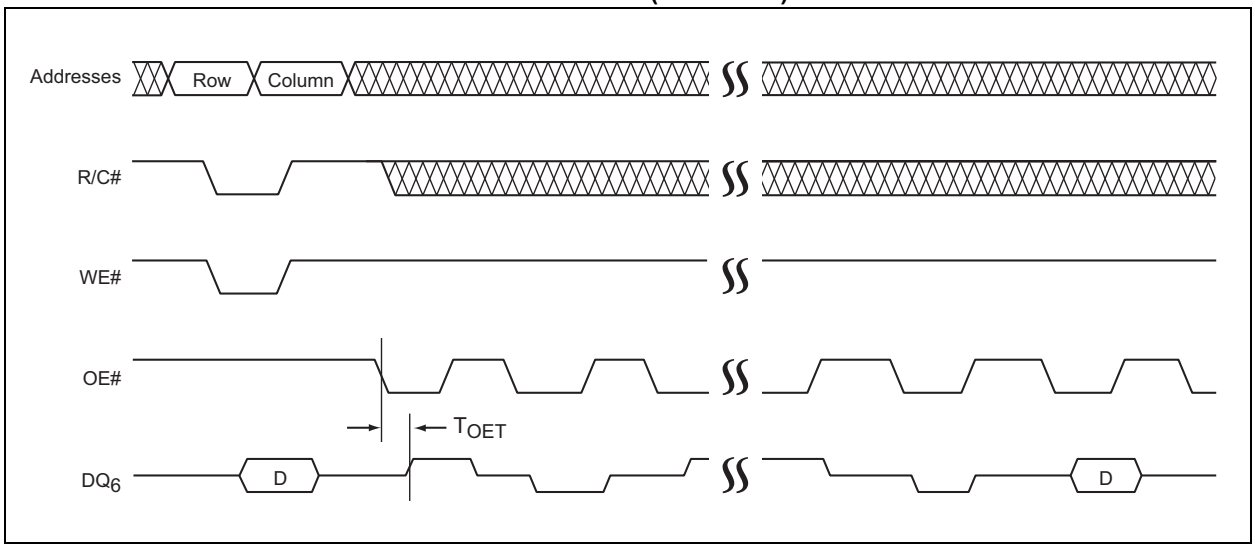


FIGURE 10-10: BYTE PROGRAM TIMING DIAGRAM (PP MODE)

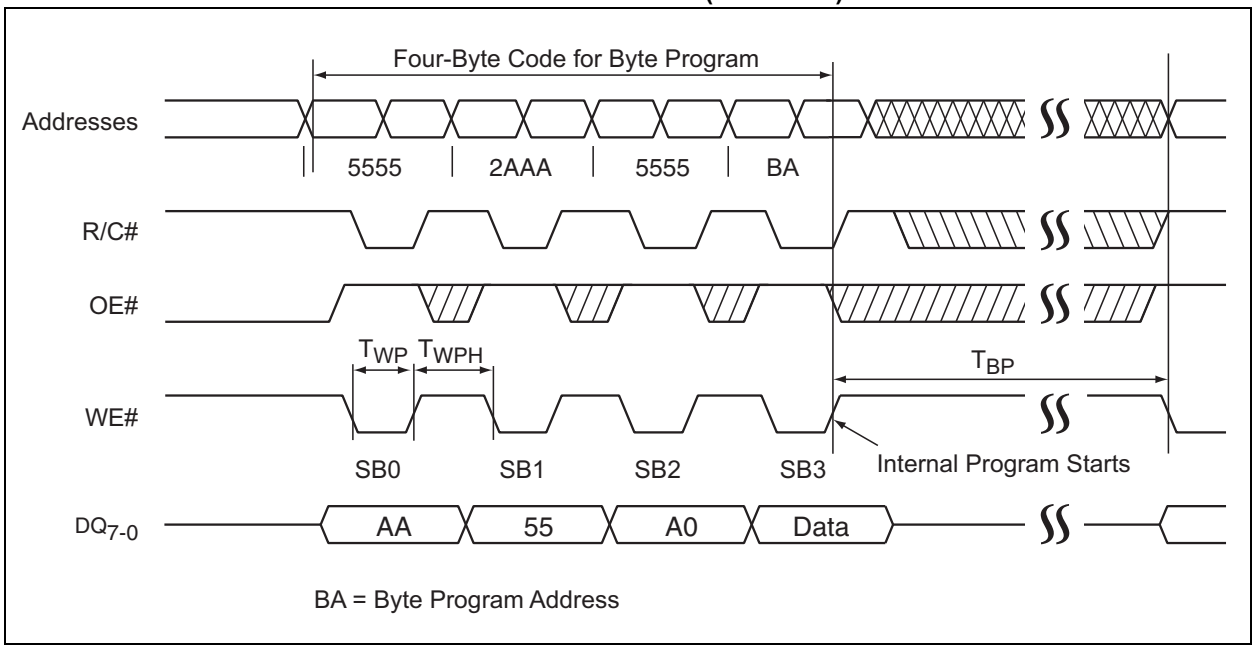


FIGURE 10-11: SECTOR ERASE TIMING DIAGRAM (PP MODE)

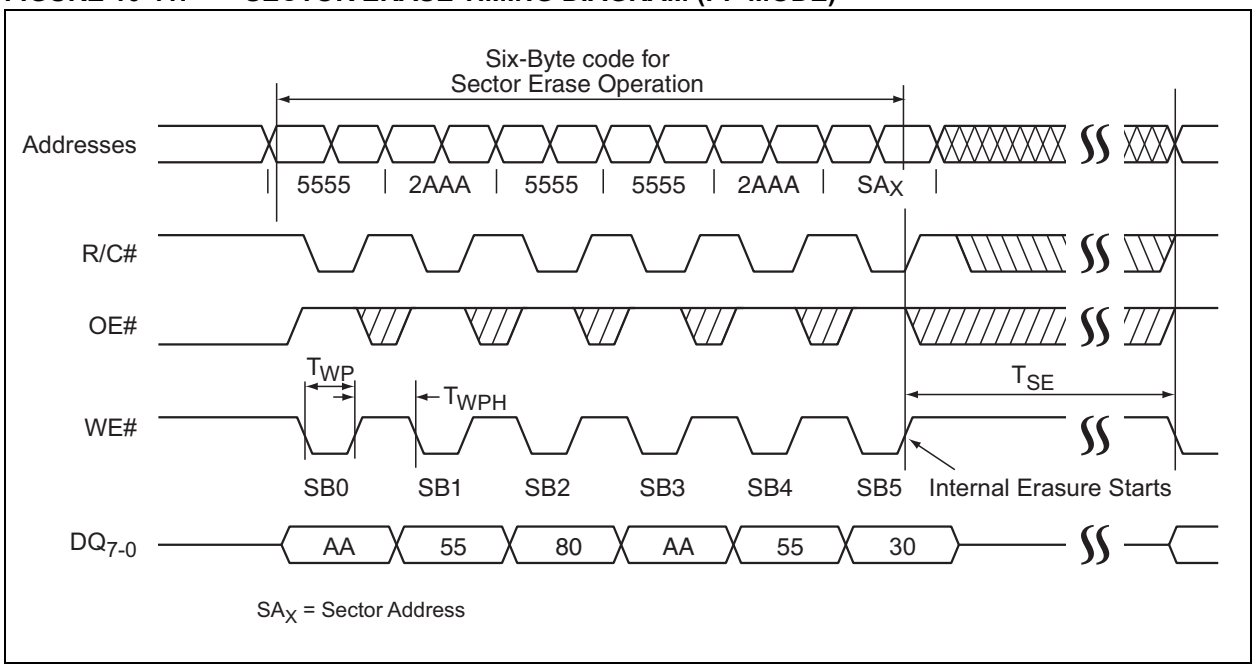


FIGURE 10-12: BLOCK ERASE TIMING DIAGRAM (PP MODE)

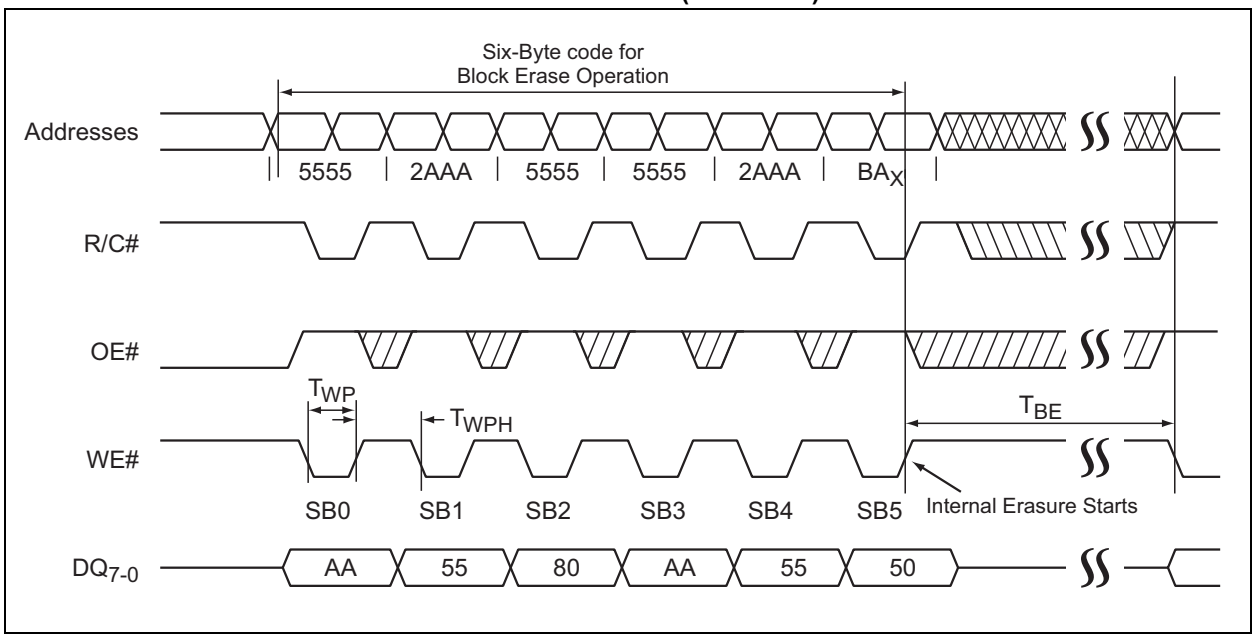


FIGURE 10-13: CHIP ERASE TIMING DIAGRAM (PP MODE)

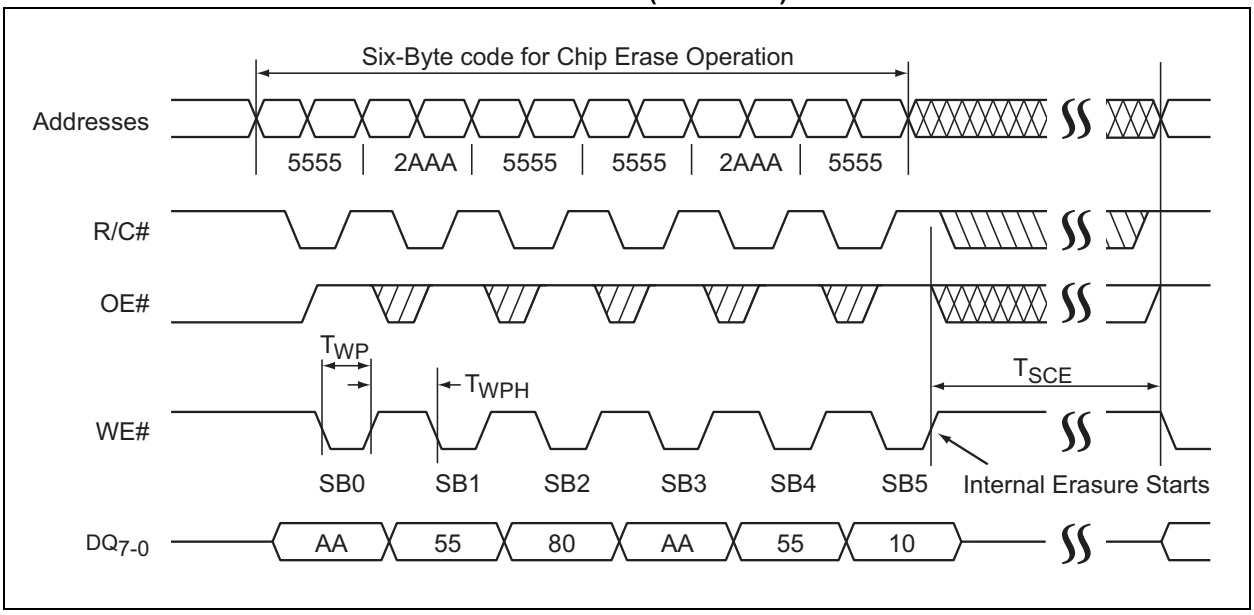


FIGURE 10-14: SOFTWARE ID ENTRY AND READ (PP MODE)

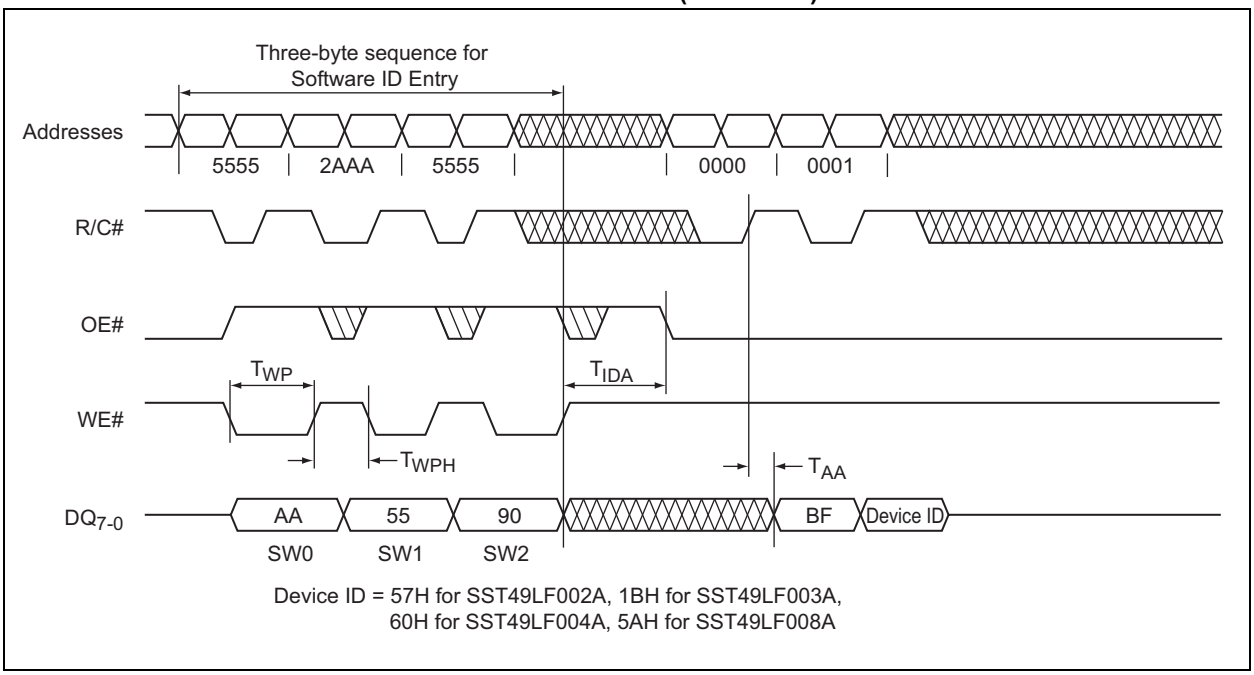


FIGURE 10-15: SOFTWARE ID EXIT AND RESET (PP MODE)

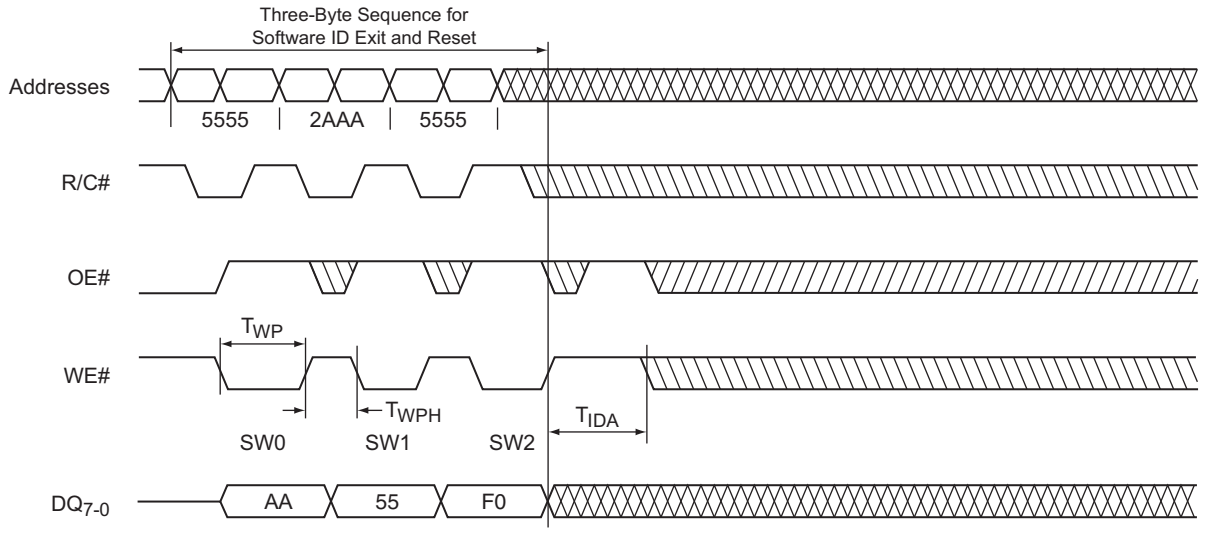
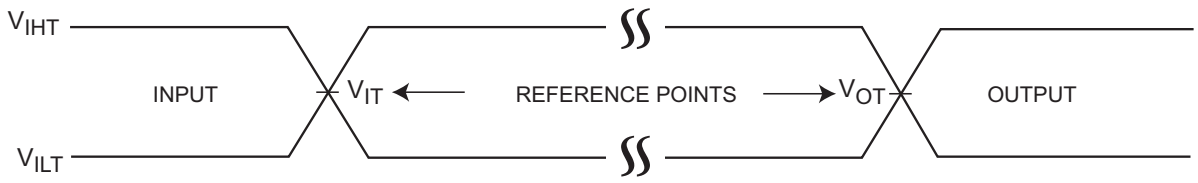


FIGURE 10-16: AC INPUT/OUTPUT REFERENCE WAVEFORMS (PP MODE)



Note 1: AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic '1' and V_{ILT} (0.1 V_{DD}) for a logic '0'. Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

2: V_{IT} = V_{INPUT} Test
V_{OT} = V_{OUTPUT} Test
V_{IHT} = V_{INPUT} HIGH Test
V_{ILT} = V_{INPUT} LOW Test

FIGURE 10-17: TEST LOAD EXAMPLE (PP MODE)

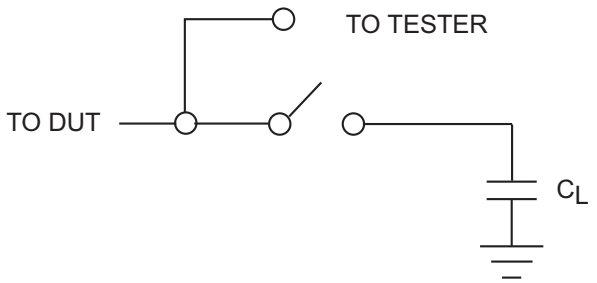


FIGURE 10-18: BYTE PROGRAM ALGORITHM

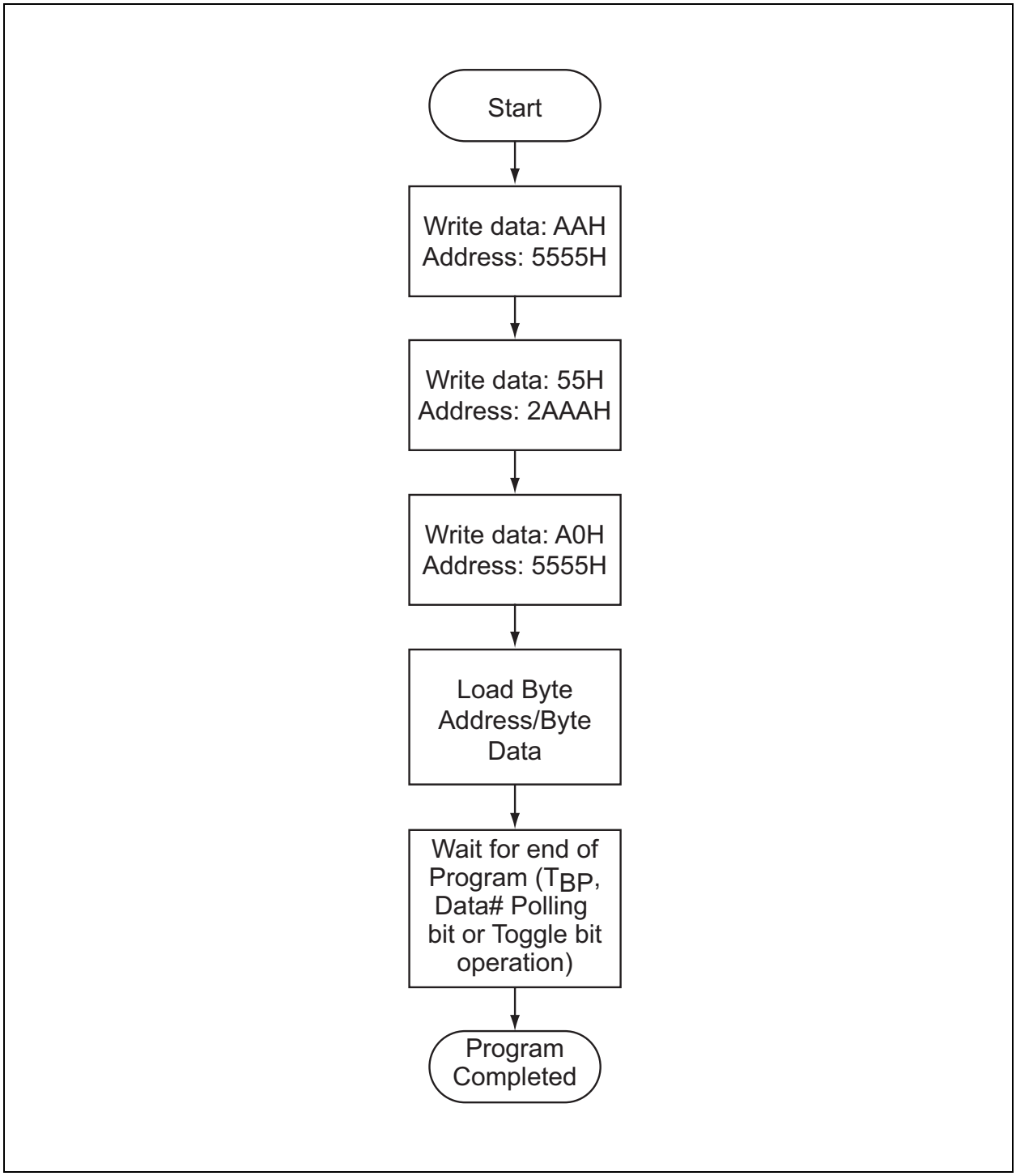


FIGURE 10-19: WAIT OPTIONS

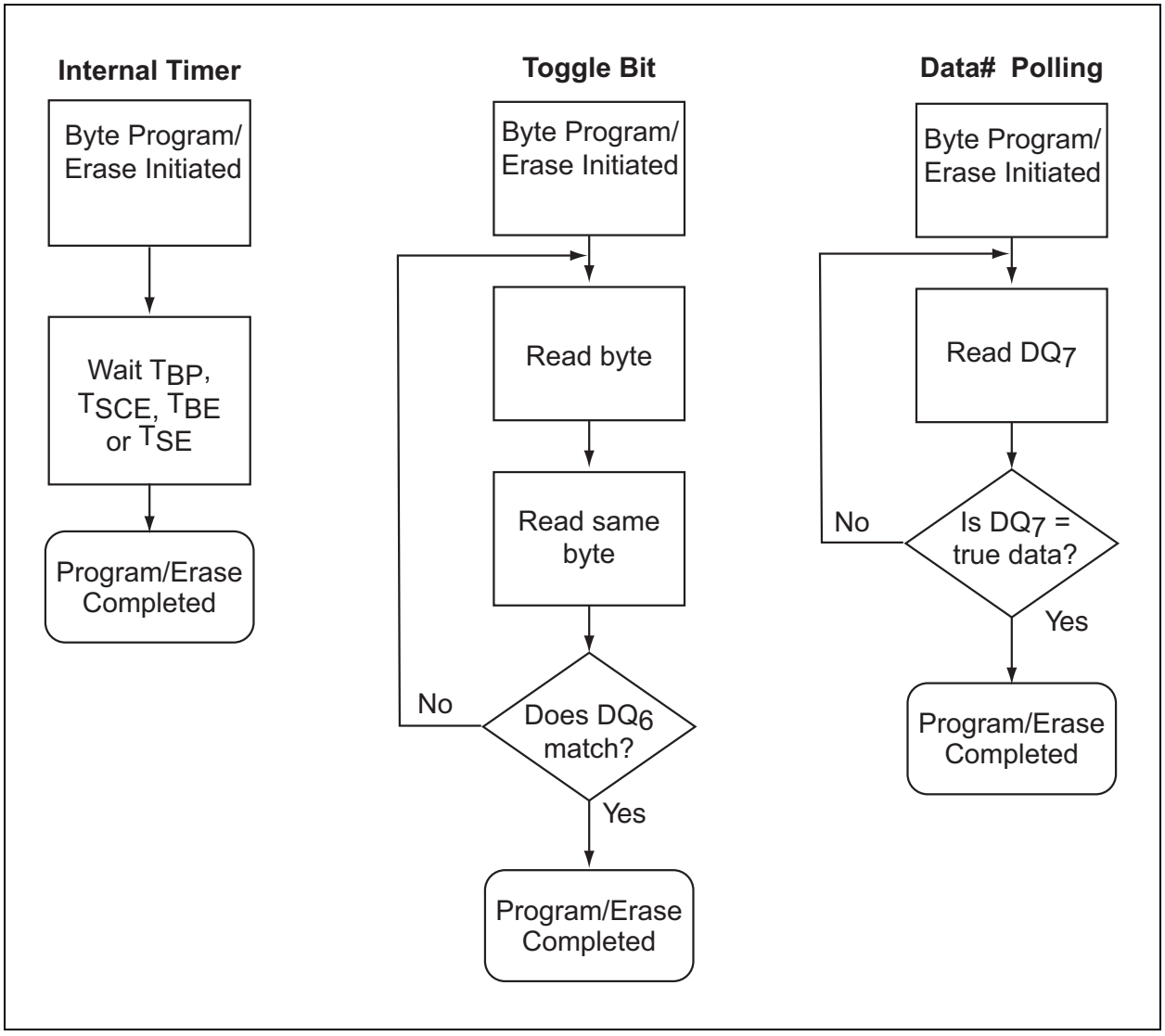


FIGURE 10-20: SOFTWARE PRODUCT COMMAND FLOWCHARTS

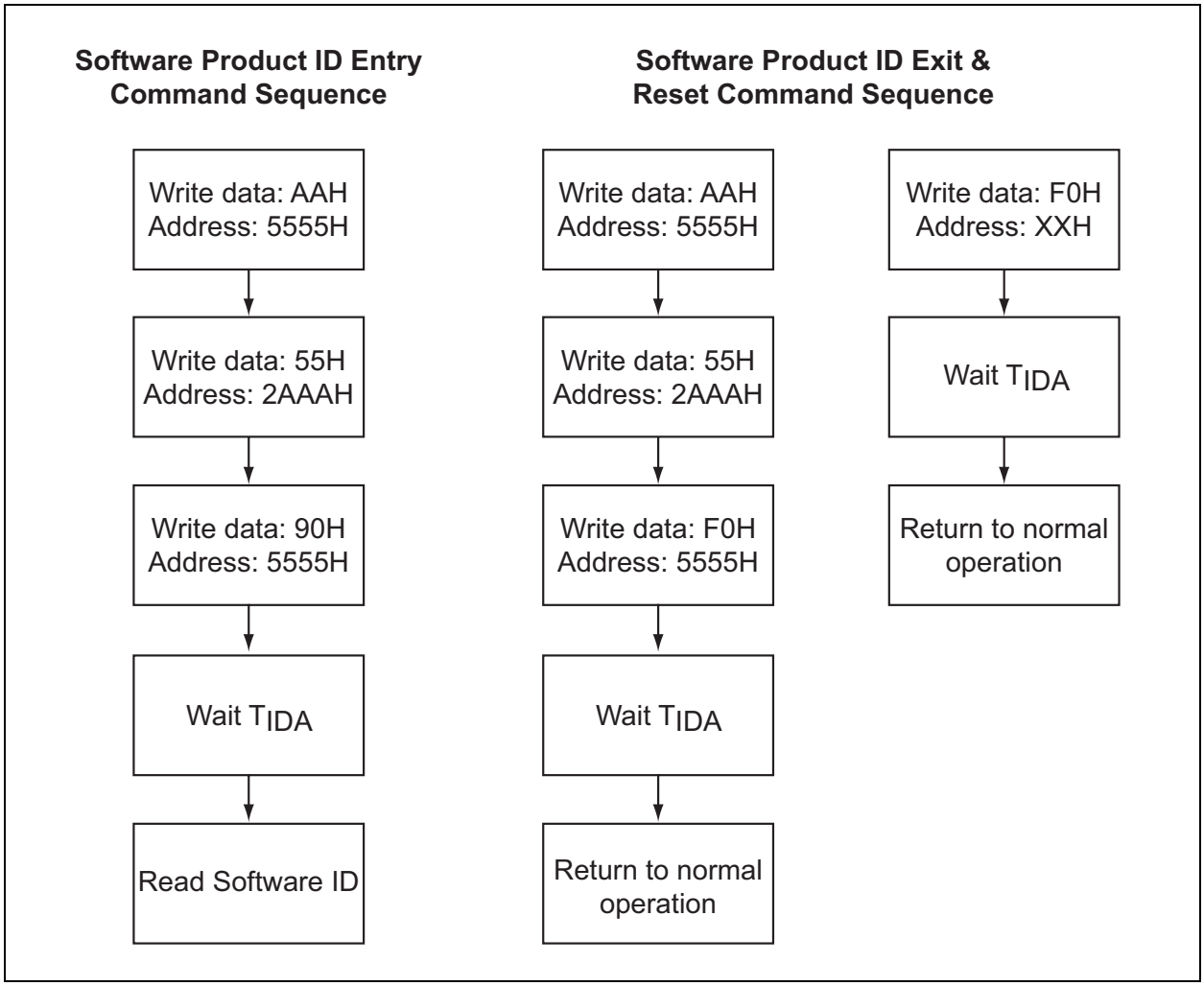
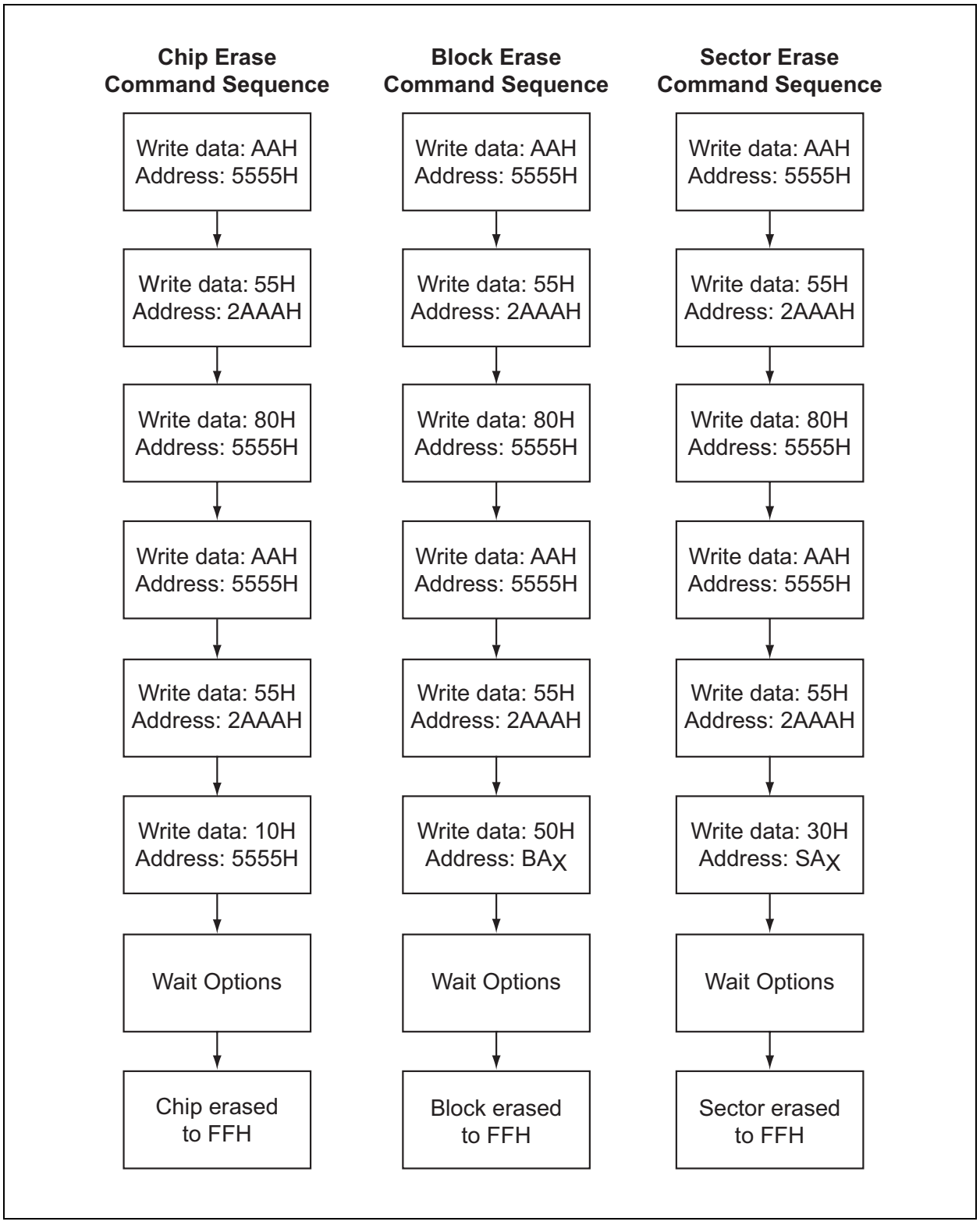


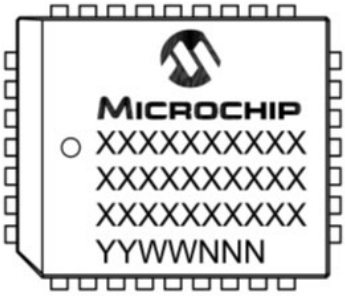
FIGURE 10-21: ERASE COMMAND SEQUENCE



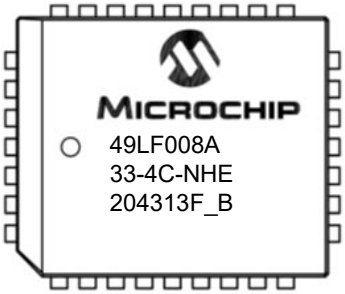
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

32-Lead PLCC

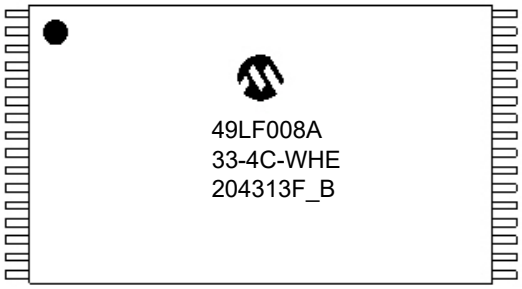


Example



32-Lead TSOP

Example



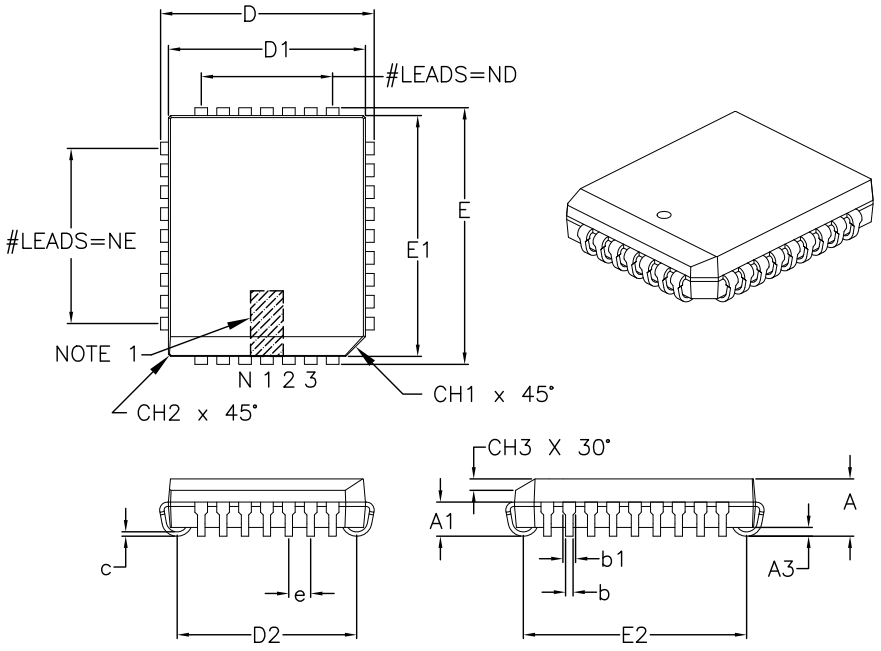
Part Number	1st Line Marking Codes	
	PLCC	TSOP
SST49LF008A	SST49LF008A-33-4C-NHE	SST49LF008A-33-4C-WHE
	SST49LF008A-33-4C-NHE-T	SST49LF008A-33-4C-WHE-T

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC® designator (e3) , the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]



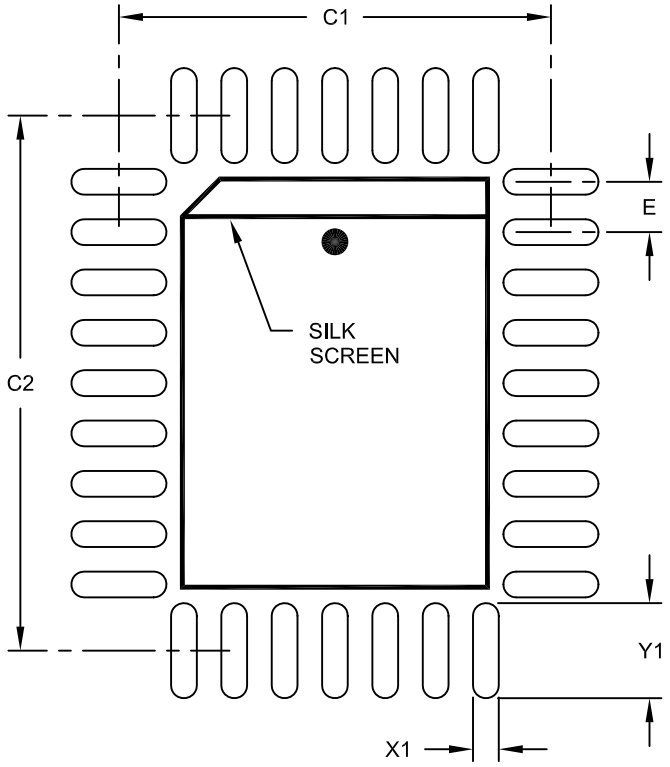
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		32	
Pitch	e		.050	
Pins along Length	ND		7	
Pins along Width	NE		9	
Overall Height	A	.125	–	.140
Contact Height	A1	.060	–	.095
Standoff §	A3	.015	–	–
Corner Chamfer	CH1	.042	–	.048
Chamfers	CH2	–	–	.020
Side Chamfer Height	CH3	.023	–	.029
Overall Length	D	.485	–	.495
Overall Width	E	.585	–	.595
Molded Package Length	D1	.447	–	.453
Molded Package Width	E1	.547	–	.553
Footprint Length	D2	.376	–	.446
Footprint Width	E2	.476	–	.546
Lead Thickness	c	.008	–	.013
Upper Lead Width	b1	.026	–	.032
Lower Lead Width	b	.013	–	.021

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

Microchip Technology Drawing No. C04–023B

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		.050 BSC	
Contact Pad Spacing	C1		.429	
Contact Pad Spacing	C2		.531	
Contact Pad Width (X32)	X1			,026
Contact Pad Length (X32)	Y1			.094

Notes:

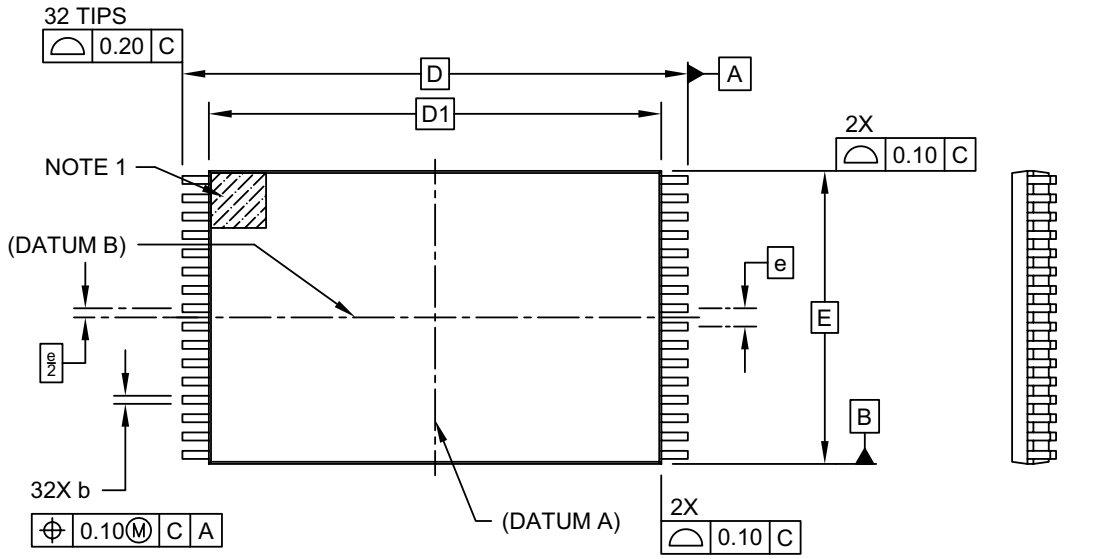
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2023A

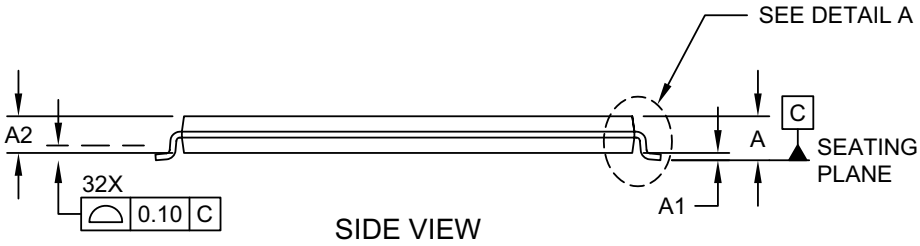
32-Lead Plastic Thin Small Outline Package (TP) - 8x14 mm Body [TSOP]
SST Legacy Package WHE

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

END VIEW

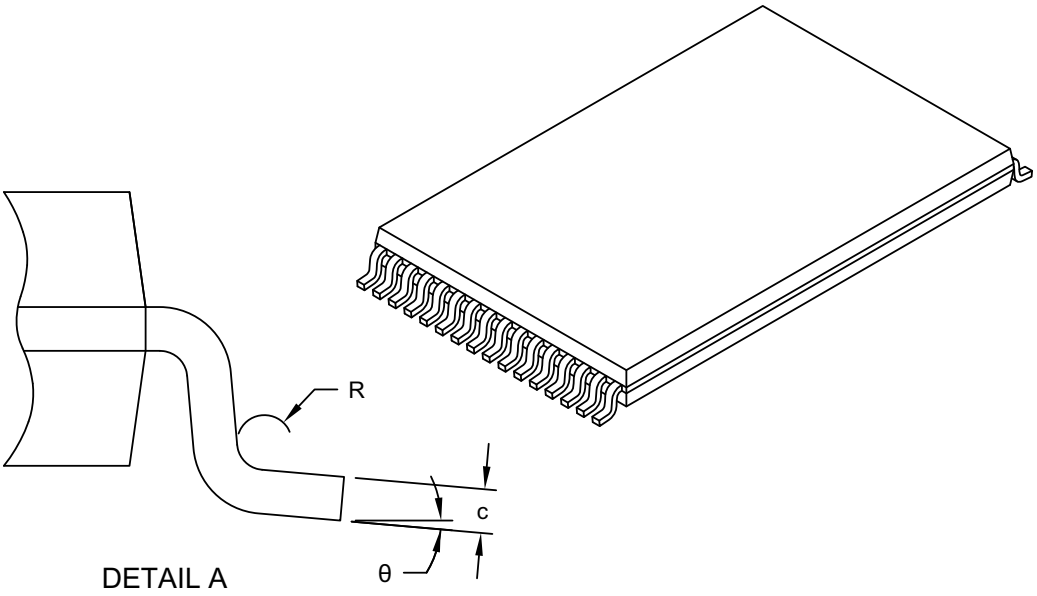


SIDE VIEW

Microchip Technology Drawing C04-174 Rev A Sheet 1 of 2

32-Lead Plastic Thin Small Outline Package (TP) - 8x14 mm Body [TSOP]
SST Legacy Package WHE

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		14.00 BSC	
Molded Package Length	D1		12.40 BSC	
Overall Width	E		8.00 BSC	
Terminal Thickness	c	0.10	-	0.21
Terminal Width	b	0.17	0.22	0.27
Terminal Length	L	0.50	0.60	0.70
Foot Angle	θ	0°	5°	8°
Terminal Bend Radius	R	0.08	-	0.35

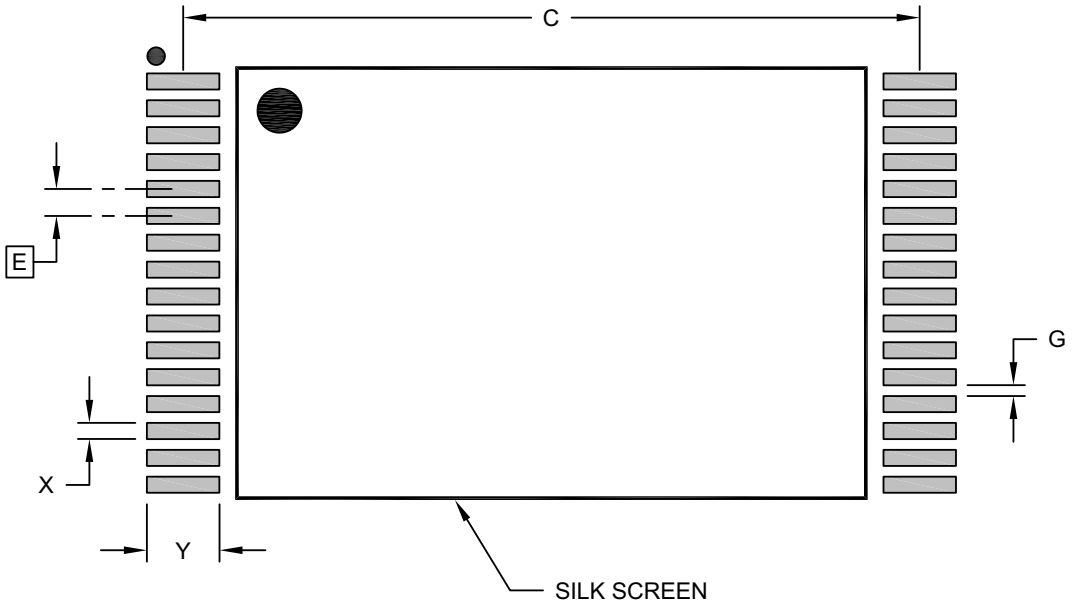
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D1 and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-174 Rev A Sheet 2 of 2

32-Lead Plastic Thin Small Outline Package (TP) - 8x14 mm Body [TSOP]
SST Legacy Package WHE

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C		13.70	
Contact Pad Width (X32)	X			0.30
Contact Pad Length (X32)	Y			1.35
Contact Pad to Contact Pad (X30)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2174 Rev A

12.0 REVISION HISTORY

Revision B (December 2020)

Converted document to Microchip format; Removed 40-lead TSOP package.

Revision A (October 2011)

Applied new document format; Released document under letter revision system; Updated Spec number from S71161 to DS25085.

SST Document S71161 Revision 11 (March 2006)

Removed 4 Mbit WH/WHE device – refer to EOL Product Data Sheet S71161(03); Added statement that non-Pb devices are RoHS compliant to Features section; Updated Surface Mount Solder Reflow Temperature information; Removed leaded part numbers; Applied new formatting.

SST Document S71161 Revision 10 (November 2004)

Removed 32-PLCC (NH/NHE) Package and associated MPNs for the 4-Mbit device – refer to EOL Product Data Sheet S71161(03); Clarified the Solder Temperature Profile under “Absolute Maximum Stress Ratings” on page 22.

SST Document S71161 Revision 9 (October 2004)

Removed 2-Mbit and 3-Mbit devices – refer to EOL Product Data Sheet S71161(01).

SST Document S71161 Revision 8 (December 2003)

2004 Data Book; Updated document status to Data Sheet.

SST Document S71161 Revision 7 (June 2003)

Added 40-lead TSOP for SST49LF008A only;
Corrected the IDD Test Conditions in Table 12 on page 23.

SST Document S71161 Revision 6 (July 2001)

2002 Data Book; Changed Transient Voltage from -1.0V to V_{DD} +1.0V to -2.0V to V_{DD} +2.0V to match Intel FWH spec per IBM requirement; Added footnote for Transient Voltage; Updated footnote for Output Short Circuit Current; Updated Data# Polling description; Corrected the values in Table 5 on page 14: General Purpose Inputs Register; Added note to Table 12 on page 23: DC Operating Characteristics.

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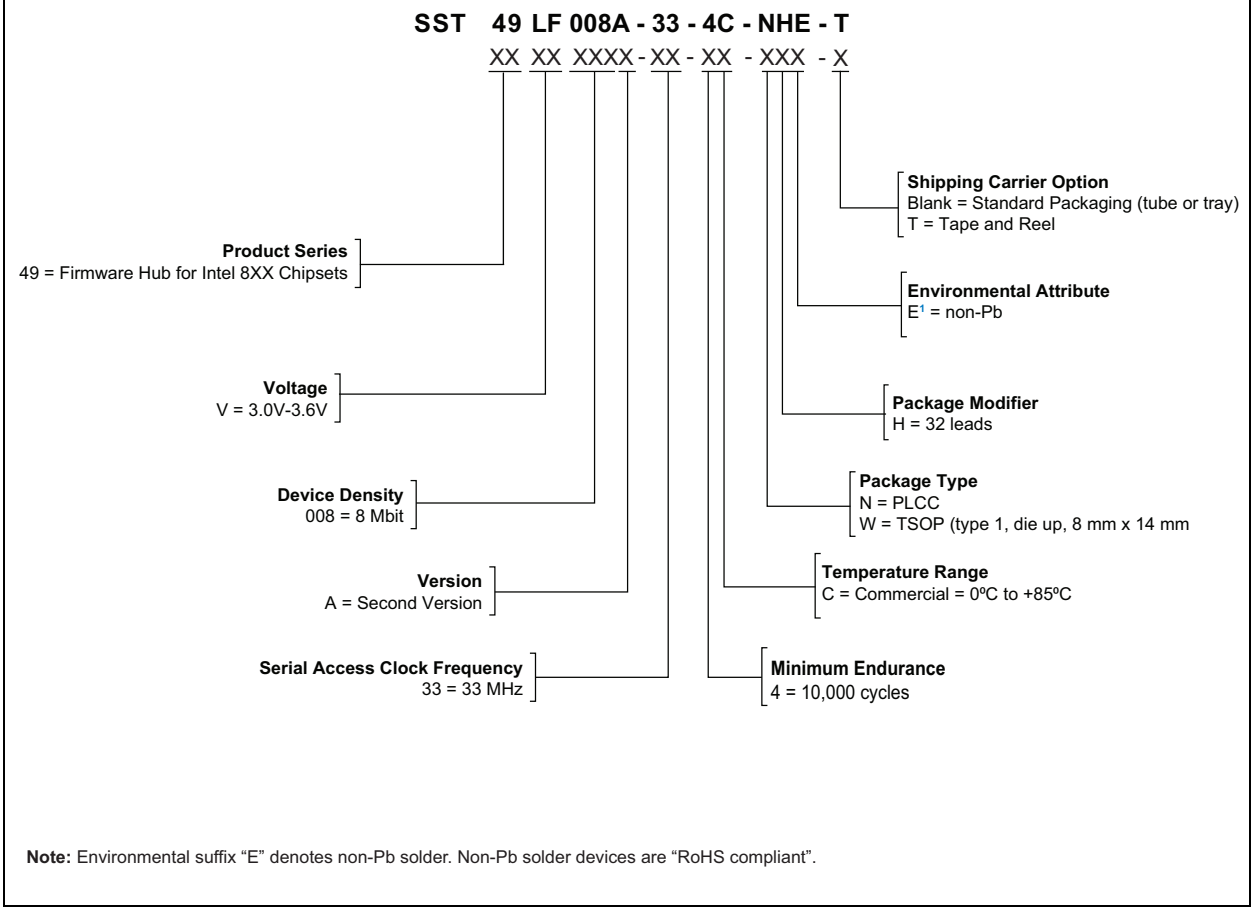

Note: Environmental suffix “E” denotes non-Pb solder. Non-Pb solder devices are “RoHS compliant”.

Valid Combinations
SST49LF008A-33-4C-WHE
SST49LF008A-33-4C-NHE
SST49LF008A-33-4C-WHE-T
SST49LF008A-33-4C-NHE-T

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