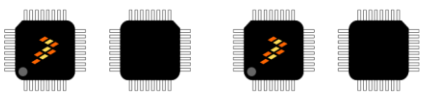
具有最高 256 KB FLASH 的 Kinetis KE15Z/14Z

最高 72 MHz 基于 ARM® Cortex®-M0+的微控制器

MKE1xZ256VLL7
MKE1xZ256VLH7
MKE1xZ128VLL7
MKE1xZ128VLH7

Kinetis KE1xZ256 MCU 是基于 ARM® Cortex®-M0+内核的 KE1xZ 系列的主要器件。KE1xZ 提供最高 256 KB 的 Flash、最高 32 KB 的 RAM 和一整套模拟/数字功能，将 Kinetis E 系列提升到更高的性能和更广泛的可扩展性。稳健的 TSI 为客户的 HMI 系统提供高水平的稳定性和准确度。1 Msps ADC 和 FlexTimer 有助于为 BLDC 电机控制系统构建出色的解决方案。



100 LQFP (LL)
14x14x1.4 mm P 0.5

64 LQFP (LH)
10x10x1.4 mm P 0.5

内核处理器和系统

- ARM® Cortex®-M0+内核，最高支持 72 MHz 频率
- 基于 ARMv6 架构和 Thumb®-2 ISA 的 ARM 内核
- 可配置嵌套向量中断控制器(NVIC)
- 存储器映射除法和平方根模块(MMDVSQ)
- 8 通道 DMA 控制器通过 DMAMUX 扩展至 63 个通道

可靠性、功能安全与信息安全

- Flash 访问控制(FAC)
- 循环冗余校验(CRC)发生器模块
- 128 位唯一标识(ID)号
- 具有独立时钟源的内部看门狗(WDOG)
- 外部看门狗监测器(EWM)模块
- ADC 自校准功能
- 片上时钟丢失监控

人机界面(HMI)

- 支持最多 32 个中断请求(IRQ)源
- 最多 89 个具有中断功能的 GPIO 引脚
- 触摸感应输入(TSI)模块

存储器和存储器接口

- 最高 256 KB 的程序 Flash
- 最高 32 KB SRAM
- 用于数据 Flash 的 32 KB FlexNVM，带 EEPROM 模拟
- 用于 EEPROM 模拟的 2 KB FlexRAM
- 128 字节 Flash 缓存
- 带有内置引导加载程序的启动 ROM

混合信号模拟

- 2 个 12 位模数转换器(ADC)，每个模块最多 16 个通道模拟输入，最高 1 Msps
- 2 个带内部 8 位数模转换器(DAC)的高速模拟比较器(CMP)；CMP0 的 8 位 DAC 支持通过缓冲器输出到引脚的选项

时序与控制

- 3 个用于 PWM 生成的 Flex Timer (FTM)，提供最多 8 个标准通道
- 1 个 16 位低功耗定时器(LPTMR)，具有灵活的唤醒控制
- 1 个可编程延迟模块(PDB)，具有灵活的触发系统
- 1 个 32 位低功耗周期性中断定时器(LPIT)，具有 4 个通道
- 实时定时器时钟(RTC)

时钟接口

- 4 - 40 MHz 快速外部振荡器(OSC)
- 32 kHz 慢速外部振荡器(OSC32)
- 用于正常运行的 48 - 60 MHz 高精度（最高±1%）快速内部参考时钟(FIRC)
- 用于低速运行的 8 MHz / 2 MHz 高精度（最高±3%）慢速内部参考时钟(SIRC)
- 128 kHz 低功耗振荡器(LPO)
- 低功耗 FLL (LPFLL)
- 最高 60 MHz 的 DC 外部方波输入时钟
- 系统时钟发生器(SCG)
- 实时计数器(RTC)

电源管理

- 低功耗 ARM Cortex-M0+内核，具有出色的能效
- 具有多种电源模式的电源管理控制器(PMC)：运行、等待、停止、VLPR、VLPW 和 VLPS
- 支持未使用模块的时钟门控，特定外设仍可在低功耗模式下工作
- POR、LVD/LVR

连接和通信接口

- 3 个具有 DMA 支持和低功耗可用性的低功耗通用异步接收器/发射器(LPUART)模块
- 2 个具有 DMA 支持和低功耗可用性的低功耗串行外设接口(LPSPI)模块
- 2 个具有 DMA 支持和低功耗可用性的低功耗内部集成电路(LPI2C)模块
- 用于灵活和高性能串行接口的 FlexIO 模块

调试功能

- 串行线调试(SWD)调试接口
- 调试观察点和跟踪(DWT)
- 微跟踪缓冲区(MTB)

工作特性

- 电压范围：2.7 至 5.5 V
- 环境温度范围：-40 至 105 ℃

相关资源

类型	说明	资源
产品简介	产品简介包含简要的概述/摘要信息，以便快速评估器件的设计适用性。	KE1xZ256PB[1]
参考手册	本参考手册全面地描述了器件的结构和功能（工作方式）。	KE1xZP100M72SF0RM[1]
数据手册	本数据手册包括电气特性和信号连接。	此文档：KE1xZP100M72SF0
芯片勘误表	芯片掩码集勘误表为特定器件掩码集提供了附加或纠正信息。	Kinetis_E_1N36S[1] Kinetis_E_2N36S[1]
封装图	封装尺寸见封装图纸。	100-LQFP：98ASS23308W 64-LQFP：98ASS23234W

1. 要查找相关资源，请访问 http://www.nxp.com 并使用该术语进行搜索。

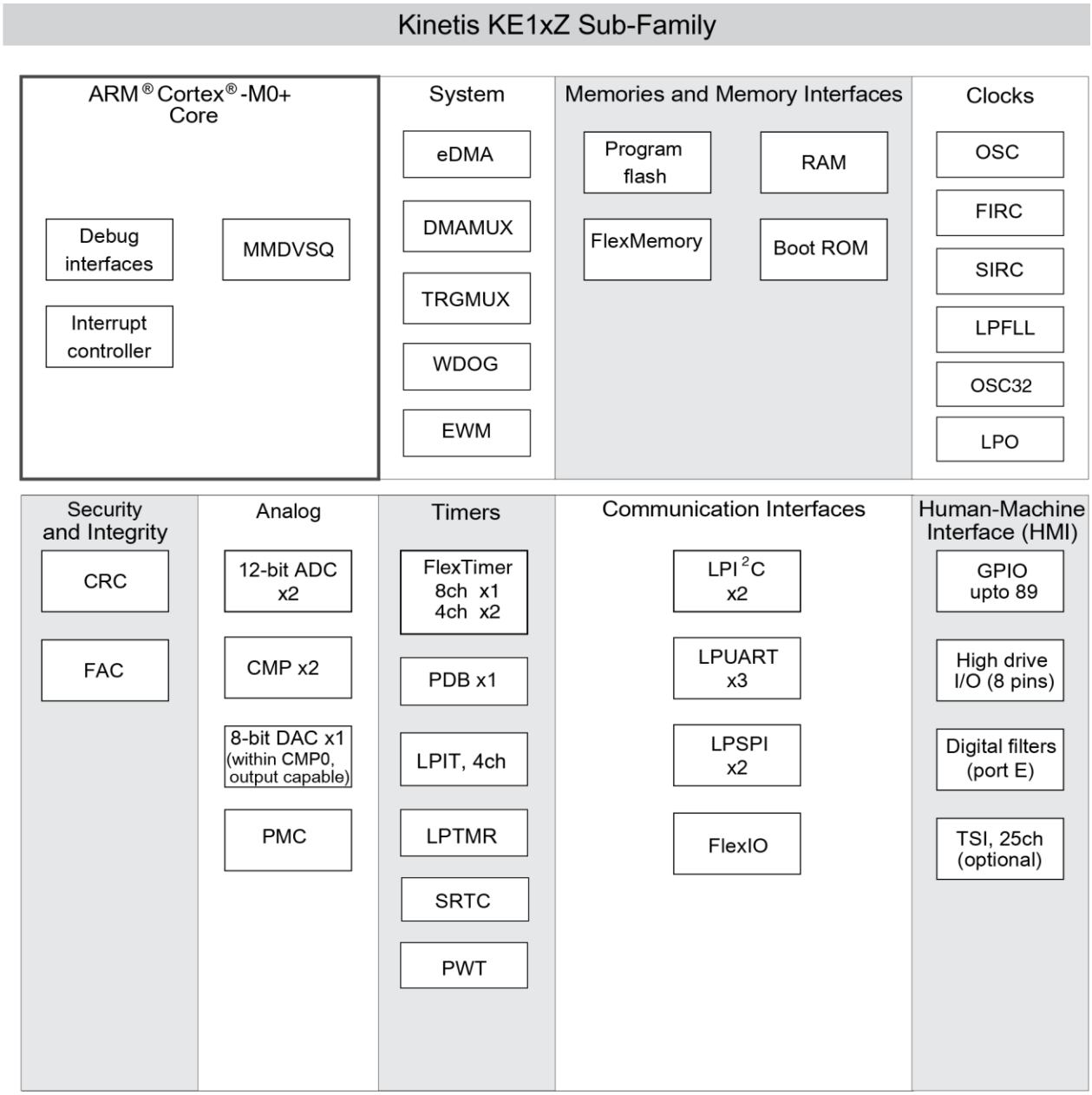

Kinetis KE1xZ Sub-Family
ARM® Cortex®-M0+ Core
Debug interfaces
MMDVSQ
Interrupt controller
System
eDMA
DMAMUX
TRGMUX
WDOG
EWM
Memories and Memory Interfaces
Program flash
RAM
FlexMemory
Boot ROM
Clocks
OSC
FIRC
SIRC
LPFLL
OSC32
LPO
Security and Integrity
CRC
FAC
Analog
12-bit ADC x2
CMP x2
8-bit DAC x1 (within CMP0, output capable)
PMC
Timers
FlexTimer 8ch x1 4ch x2
PDB x1
LPIT, 4ch
LPTMR
SRTC
PWT
Communication Interfaces
LPI2C x2
LPUART x3
LPSPI x2
FlexIO
Human-Machine Interface (HMI)
GPIO upto 89
High drive I/O (8 pins)
Digital filters (port E)
TSI, 25ch (optional)

图 1.功能框图

目录

1 订购信息

以下芯片可供订购。

表 1.订购信息

产品	存储器			封装		IO 和 ADC 通道			HMI
器件编号	Flash (KB)	SRAM (KB)	FlexNVM/ FlexRAM (KB)	引脚数量	封装	GPIO	GPIO (INT/HD)[1]	ADC 通道	TSI
MKE15Z256VLL7	256	32	32/2	100	LQFP	89	89/8	16+12	是
MKE15Z256VLH7	256	32	32/2	64	LQFP	58	58/8	16+11	是
MKE15Z128VLL7	128	16	32/2	100	LQFP	89	89/8	16+12	是
MKE15Z128VLH7	128	16	32/2	64	LQFP	58	58/8	16+11	是
MKE14Z256VLL7	256	32	32/2	100	LQFP	89	89/8	16+12	否
MKE14Z256VLH7	256	32	32/2	64	LQFP	58	58/8	16+11	否
MKE14Z128VLL7	128	16	32/2	100	LQFP	89	89/8	16+12	否
MKE14Z128VLH7	128	16	32/2	64	LQFP	58	58/8	16+11	否

1. INT：中断引脚编号；HD：高驱动引脚数

2 概述

下图为本器件的系统图。

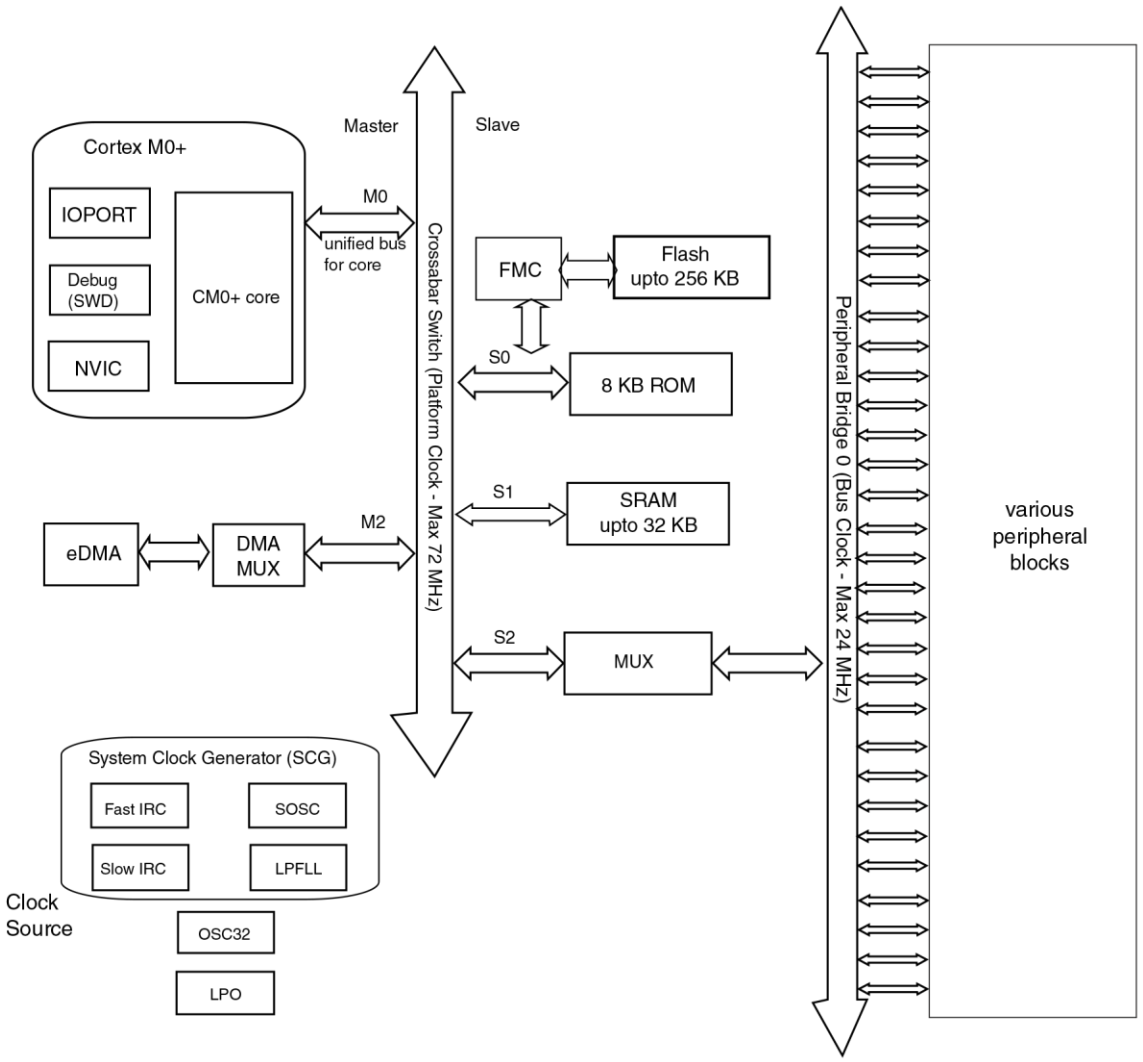


图 2.系统图

交叉开关使用交叉开关结构连接总线 Master 和 Slave。这种结构允许最多四个总线 Master 同时访问不同的总线 Slave，同时在它们访问同一个 Slave 时在总线 Master 之间提供仲裁。

2.1 系统特性

以下部分介绍了高级系统功能。

2.1.1 ARM Cortex-M0+内核

增强型 ARM Cortex M0+是 Cortex-M 系列处理器的成员，其目标是微控制器内核，侧重于对成本非常敏感的低功耗应用。它具有单个 32 位 AMBA AHB-Lite 接口，并包括一个 NVIC 组件。它还具有硬件调试功能，包括支持简单的程序跟踪功能。该处理器支持 ARMv6-M 指令集(Thumb)架构，包括三个 16 位 Thumb 操作码（总共 52 个）和七个 32 位指令。它与其他 Cortex-M 配置文件处理器向上兼容。

2.1.2 NVIC

嵌套向量中断控制器支持嵌套中断和 4 个中断优先级。在 NVIC 中，IPR 寄存器中的每个源都包含 2 个位。它的中断源数量也不同，支持 32 个中断向量。

Cortex-M 系列使用多种方法将 Cortex-M0+的中断延迟提高到最多 15 个时钟周期。它还可用于将 MCU 内核从等待和 VLPW 模式唤醒。

2.1.3 AWIC

异步唤醒中断控制器(AWIC)用于检测停止模式下的异步唤醒事件，并向时钟控制逻辑发送信号以恢复系统计时。时钟重启后，NVIC 观察待定中断并执行正常的中断或事件处理。AWIC 可用于将 MCU 内核从部分停止、停止和 VLPS 模式唤醒。

该 SoC 的唤醒源如下所示：

表 2.AWIC 停止和 VLPS 唤醒源

唤醒信号源	说明
可用的系统复位	RESET 引脚、WDOG、时钟丢失(LOC)复位和锁定丢失(LOL)复位
引脚中断	端口控制模块——任何启用的引脚中断都能够唤醒系统
ADCx	ADCx 是可选功能，具有来自 SIRC 或 OSC 的时钟源
CMPx	在停止/VLPS 模式下工作，具有来自 SIRC 或 OSC 的时钟源
LPI2C	在停止/VLPS 模式下工作，具有来自 SIRC 或 OSC 的时钟源
LPUART	在停止/VLPS 模式下工作，具有来自 SIRC 或 OSC 的时钟源

表格接下页……

表 2.AWIC 停止和 VLPS 唤醒源（续）

唤醒信号源	说明
LPSPI	在停止/VLPS 模式下工作，具有来自 SIRC 或 OSC 的时钟源
LPIT	在停止/VLPS 模式下工作，具有来自 SIRC 或 OSC 的时钟源
FlexIO	在停止/VLPS 模式下工作，具有来自 SIRC 或 OSC 的时钟源
LPTMR	在停止/VLPS 模式下工作
RTC	在停止/VLPS 模式下工作
SCG	在停止模式下的工作（仅限 SIRC）
TSI	触摸感应唤醒
NMI	非屏蔽中断

2.1.4 存储器

本器件具有以下特点：

- 最高 256 KB 的嵌入式程序 Flash。
- 最高 32 KB 的嵌入式 RAM，可在 CPU 时钟速度下以零等待状态访问（读/写）。
- 非易失性存储器分为几个阵列：
  - 32 KB 的嵌入式数据 Flash
  - 2 KB 的模拟 EEPROM
  - 8 KB ROM（内置引导加载程序，支持 UART、I2C 和 SPI 接口）

  程序 Flash 包含一个 16 字节的 Flash 配置字段，用于存储默认保护设置和安全信息。程序 Flash 的页面大小为 1 KB。

  保护设置可以保护程序 Flash 的 32 个区域免遭意外擦除或编程操作。

  安全电路可防止未经授权从调试端口访问 RAM 或 Flash 内容。

2.1.5 复位和启动

下表列出了该器件支持的所有复位源。

注意

下表中，“是”表示特定模块（脚注中提到的寄存器、位或条件除外）被相应的复位源复位。“否”表示特定模块没有被相应的复位源复位。

表 3.复位源

复位源	说明	模块									
		PMC	SIM	SMC	RCM	复位引脚被取消	WDOG	SCG	RTC	LPTMR	其他
POR 复位	上电复位(POR)	是	是	是	是	是	是	是	是	是	是
系统复位	低压检测(LVD)	是 [1]	是	是	是	是	是	是	否	是	是
	外部引脚复位(RESET)	是 [1]	是 [2]	是 [3]	是 [4]	是	是 [5]	是 [6]	否	否	是
	看门狗(WDOG)复位	是 [1]	是 [2]	是 [3]	是 [4]	是	是 [5]	是 [6]	否	否	是
	多用途时钟发生器时钟丢失(LOC)复位	是 [1]	是 [2]	是 [3]	是 [4]	是	是 [5]	是 [6]	否	否	是
	多用途时钟发生器锁定丢失(LOL)复位	是 [1]	是 [2]	是 [3]	是 [4]	是	是 [5]	是 [6]	否	否	是
	停止模式确认错误(SACKERR)	是 [1]	是 [2]	是 [3]	是 [4]	是	是 [5]	是 [6]	否	否	是
	软件复位(SW)	是 [1]	是 [2]	是 [3]	是 [4]	是	是 [5]	是 [6]	否	否	是
	锁定复位(LOCKUP)	是 [1]	是 [2]	是 [3]	是 [4]	是	是 [5]	是 [6]	否	否	是
	MDM DAP 系统复位	是 [1]	是 [2]	是 [3]	是 [4]	是	是 [5]	是 [6]	否	否	是
调试复位	调试复位	是 [1]	是 [2]	是 [3]	是 [4]	是	是 [5]	是 [6]	否	否	是

1. 除了 PMC_LVDSC1[LVDV]和 PMC_LVDSC2[LVWV]
2. 除了 SIM_SOPT1
3. 除了 SMC_PMPROT、SMC_PMCTRL_RUM、SMC_PMCTRL_STOPM、SMC_STOPCTRL、SMC_PMSTAT
4. 除了 RCM_RPC、RCM_MR、RCM_FM、RCM_SRIE、RCM_SRS、RCM_SSRS
5. 除了 WDOG_CS[TST]
6. 除了 SCG_CSR 和 SCG_FIRCSTAT

此器件支持从以下位置启动：

- 内部 Flash
- 启动 ROM

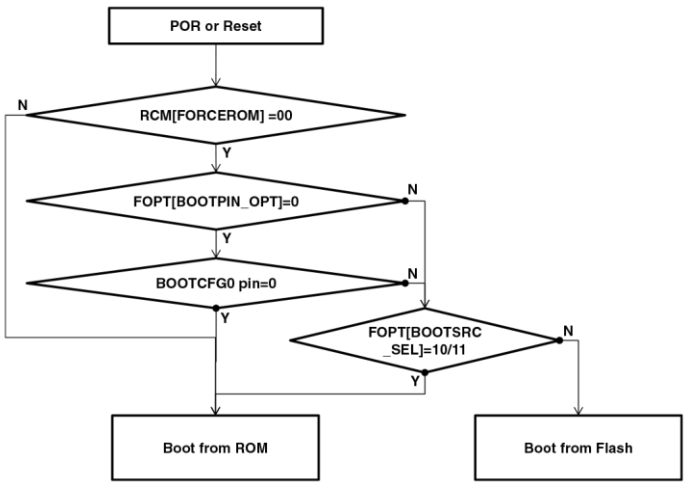


图 3.启动流程图

空白芯片默认从 ROM 启动，并将向量表重新映射到 ROM 基地址，否则，它重新映射到 Flash 地址。

2.1.6 时钟选项

SCG 模块控制使用哪个时钟源来获取系统时钟。时钟生成逻辑将选定的时钟源划分为各种时钟域，包括系统总线 Master、系统总线 Slave 和 Flash 的时钟。时钟生成逻辑还实现了特定于模块的时钟门控，以允许对模块进行精细关闭。

下图是时钟生成的简要功能框图。有关时钟操作和配置的更多详细信息，请参见参考手册中的“时钟”章节。

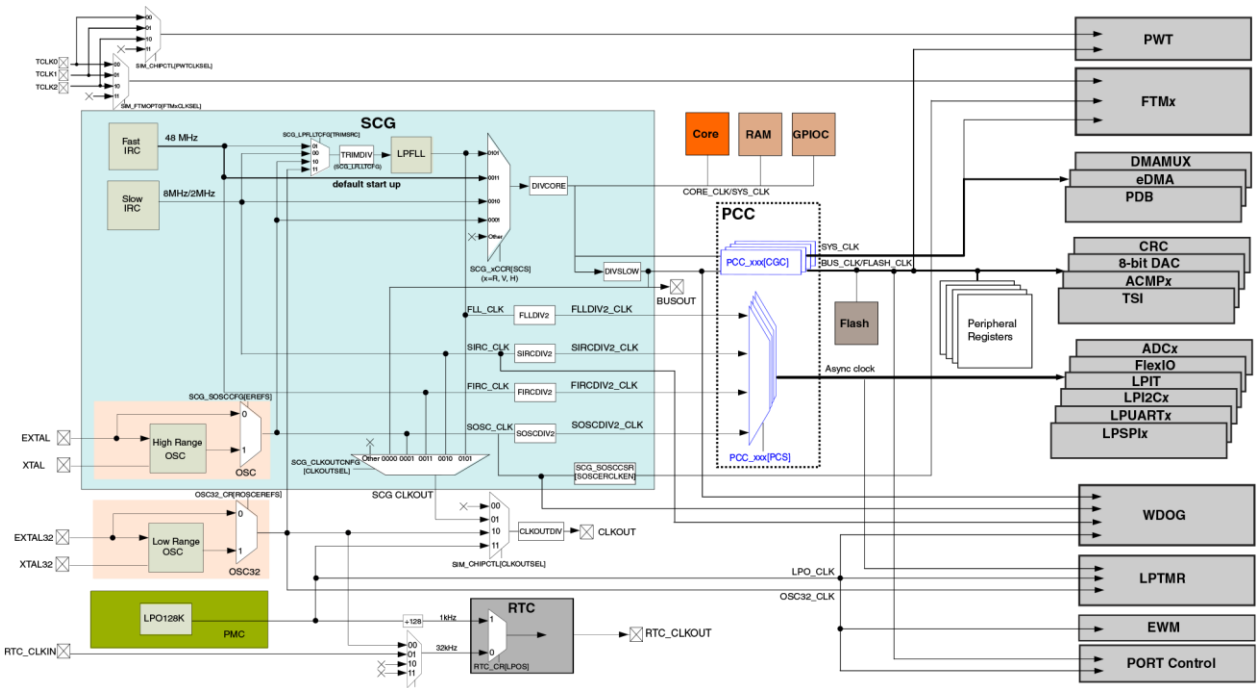


图 4。时钟功能框图

2.1.7 安全性

可以通过编程 Flash 配置字段(0x40e)使能安全状态。使能器件安全后，SWD 端口无法访问 MCU 的存储器资源。

外部接口	安全性	不安全
SWD 端口	无法通过 SWD 接口访问存储器源	调试器可以写入 MDM-AP 控制寄存器的“正在进行 Flash 批量擦除”字段，以触发批量擦除（擦除所有块）命令

2.1.7.1 Flash 访问控制(FAC)

FAC 是一种原生或第三方可配置的存储器保护方案，经过优化，允许最终用户利用软件库，同时为这些库提供可编程限制。Flash 分成大小相等的段，为专有软件库提供保护。这些段的保护受到控制，因为 FAC 为路由到片上 Flash 的每个事务提供了访问权限的逐周期评估。可配置性允许越来越多的受保护段，同时支持两个级别的供应商将其专有软件添加到器件。

2.1.8 电源管理

电源管理控制器(PMC)在 ARM 的运行、睡眠和深度睡眠工作模式上进行扩展，以提供多种可配置模式。这些模式可用于优化各种应用的电流消耗。WFI 或 WFE 指令调用等待或停止模式，具体取决于当前配置。有关 ARM 工作模式的更多信息，请参见 ARM® Cortex®用户指南。

PMC 在 ARM 的运行工作模式下提供正常运行(RUN)和超低功耗运行(VLPR)配置。在这些模式下，MCU 内核处于活动状态并且可以访问所有外设。模式之间的区别在于系统的最大时钟频率，也就是功耗。可以选择与应用程序的功率与性能要求相匹配的配置。

PMC 在 ARM 的睡眠工作模式下提供等待(Wait)和极低功耗等待(VLPW)配置。在这些模式下，即使 MCU 内核处于非活动状态，也可以使能所有外设并按照编程工作。模式之间的区别在于系统的最大时钟频率，也就是功耗。

PMC 在 ARM 的深度睡眠工作模式下提供停止(Stop)、极低功耗停止(VLPS)配置。在这些模式下，MCU 内核和大部分外设都被禁用。根据应用的要求，可以保留或禁用模拟、逻辑和存储器的不同部分以节省功率。

嵌套向量中断控制器(NVIC)、异步唤醒中断控制器(AWIC)用于将 MCU 从低功耗状态唤醒。NVIC 用于将 MCU 内核从 WAIT 和 VLPW 模式唤醒。AWIC 用于将 MCU 内核从停止和 VLPS 模式唤醒。

有关工作模式、电源管理、NVIC、AWIC 的更多信息，请参见参考手册。

下表提供了有关各种工作模式下的外设状态以及可将 MCU 从低功耗模式唤醒的模块的信息。

表 5.不同工作模式下的外设状态

核心模式	器件模式	说明
运行模式	运行	在运行模式下，所有器件模块都可以工作。
	极低功耗运行	在 VLPR 模式下，所有器件模块都以较低的频率运行，但禁用的低电压检测(LVD)监测器除外。
睡眠模式	等待	在等待模式下，所有外设模块都可以工作。MCU 内核进入睡眠模式。
	极低功耗等待	在 VLPW 模式下，所有外设模块都以较低的频率运行，但禁用的低电压检测(LVD)监测器除外。MCU 内核进入睡眠模式。
深度睡眠	停止	在停止模式下，大多数外设时钟被禁用并处于静态状态。停止模式保留所有寄存器和 SRAM，同时保持低电压检测保护。在停止模式下，ADC、CMP、LPTMR、RTC 和引脚中断都可以工作。NVIC 被禁用，但 AWIC 可用于从中断中唤醒。
	极低功耗停止	在 VLPS 模式下，SRAM 的内容保留。CMP（低速）、ADC、OSC、RTC、LPTMR、LPIT、FlexIO、LPUART、LPI2C、LPSPI 和 DMA 都可以工作，LVD 和 NVIC 被禁用，AWIC 用于从中断中唤醒。

注意

当 MCU 处于 HSRUN 或 VLP 模式时，用户无法写入 FlexRAM(EEPROM)，也无法启动包括 Flash 编程/擦除在内的 FTFE 命令。

2.1.9 调试控制器

该器件具有广泛的调试功能，包括运行控制和跟踪功能。标准 ARM 调试端口支持 SWD 接口。

2.2 外设功能

以下各节介绍了芯片各外设的特点。

2.2.1 eDMA 和 DMAMUX

eDMA 是一种高度可编程的数据传输引擎，经过优化，可以尽可能减少主机处理器所需的任何中断。它旨在用于特定应用，其中要传输的数据大小是静态已知且未在传输的数据本身中进行定义。该器件中的 DMA 控制器实现了 8 个通道，这些通道可以通过 DMA MUX 模块从最多 63 个 DMA 请求源路由。

eDMA 的主要特点如下：

- 通过双地址传输的所有数据移动：从源读取，写入目标
- 采用 8 通道，可执行复杂的数据传输，主机处理器干预极少
- 传输控制描述符(TCD)进行组织以支持两个深层嵌套传输操作
- 通过三种方法之一激活通道
- 固定优先级和轮询通道仲裁
- 通过可编程中断请求报告通道完成
- 对分散/聚集 DMA 处理提供可编程支持
- 支持复杂的数据结构

2.2.2 FTM

该器件包含三个 FlexTimer 模块。

FlexTimer 模块(FTM)是一个 2 到 8 通道定时器，支持输入捕获、输出比较和产生 PWM 信号，以控制电机和电源管理应用。FTM 时间参考是一个 16 位计数器，可用作无符号或有符号计数器。

对该模块进行了几项关键增强：

- 有符号计数器
- 死区时间插入硬件
- 故障控制输入
- 增强的触发功能
- 初始化和极性控制

2.2.3 ADC

该器件包含两个 12 位 SAR ADC 模块。ADC 模块支持来自 FTM、LPTMR、PIT、RTC、外部触发引脚和 CMP 输出的硬件触发。当使用内部时钟源或外部晶振时钟时，它支持在低功耗模式下唤醒 MCU。

ADC 模块具有以下特点：

- 具有最高 12 位分辨率的线性逐次逼近算法
- 最多 16 个单端外部模拟输入
- 支持 12 位、10 位和 8 位单端输出模式
- 单次或连续转换

- 可配置的采样时间和转换速度/功率
- 输入时钟可从最多四个源中选择
- 在低功耗模式下工作以降低噪声
- 可选硬件转换触发
- 自动比较小于、大于或等于、在范围内或超出范围、可编程值的中断
- 温度传感器
- 硬件一般功能
- 可选基准电压源：来自外部或备用
- 自校准模式

2.2.3.1 温度传感器

该器件包含一个内部连接到 AD26 输入通道的温度传感器，请参见 ADC 电气特性，了解线性因数的详细信息。

必须校准传感器以获得良好的精度，从而提供良好的线性度，另请参见 AN3031，了解有关温度传感器的更详细应用信息。

2.2.4 CMP

该器件上有两个模拟比较器。

- 每个 CMP 都有自己独立的 8 位 DAC。
- 每个 CMP 最多支持来自外部引脚的 6 个模拟输入。
- 每个 CMP 都能够从带隙转换内部基准电压源。
- 每个 CMP 都支持轮询采样方案。总之，这允许 CMP 在 VLPS 和停止模式下独立运行，同时定期触发以对最多 8 个输入进行采样。只有当输入改变状态时，才会产生完全唤醒。

CMP 具有以下特点：

- 输入范围可能从轨到轨
- 可编程迟滞控制
- 可选择在比较器输出的上升沿、下降沿或上升沿和下降沿进行中断
- 比较器输出的可选反相
- 能够产生广泛的输出，例如采样、加窗或数字滤波
- 可在输出滤波器用于内部功能的同时使用外部迟滞

- 两个软件可选的性能级别：以更高的功率为代价实现更短的传播延迟，而更长的传播延迟实现低功耗
- DMA 传输支持
- 在此 MCU 上可用的所有电源模式下均正常工作
- 窗口和滤波器功能在停止模式下不可用
- 集成 8 位 DAC，具有可选基准电压源，并且可以掉电以节省功率

2.2.5 RTC

RTC 是一个始终通电的模块，在所有低功耗模式下都保持活动状态。RTC 内的时间计数器由 32.768 kHz 时钟提供时钟，该时钟来自使用振荡器的外部晶振，或直接从 RTC_CLKIN 引脚提供时钟。

RTC 在上电复位时复位，RTC 中的软件复位位也可以初始化所有 RTC 寄存器。

RTC 模块具有以下特点

- 具有翻转保护和 32 位报警的 32 位秒计数器
- 带补偿功能的 16 位预分频器，可纠正 0.12 ppm 至 3906 ppm 之间的误差
- 具有寄存器锁定机制的寄存器写保护
- 1 Hz 方波或秒脉冲输出，带可选中断

2.2.6 LPIT

低功耗周期性中断定时器(LPIT)是一个多通道定时器模块，可生成独立的预触发和触发输出。这些定时器通道可以单独操作，也可以链接在一起。如果 LPIT 配置为低功耗模式，则可在该模式下运行。预触发和触发输出可用于触发器件上的其他模块。

该器件包含一个具有四个通道的 LPIT 模块。LPIT 为 DMAMUX 生成周期性触发事件。

2.2.7 PDB

可编程延迟模块(PDB)提供可控延迟，范围从内部或外部触发或可编程间隔节拍到 ADC 的硬件触发输入，和/或对 DAC 生成间隔触发，以便 ADC 转换之间的精确时序和/或可以实现 DAC 更新。PDB 可以选择性地提供脉冲输出(Pulse-Out's)，用作 CMP 模块中的采样窗口。

PDB 模块具有以下功能：

- 触发输入源和一个软件触发源
- 1 个 DAC 刷新触发输出，用于此器件
- 用于 ADC 硬件触发的可配置 PDB 通道
- 1 个脉冲输出，用于此器件

2.2.8 LPTMR

在所有电源模式（包括低泄漏模式）下，低功耗定时器(LPTMR)可配置为用作带有可选预分频器的时间计数器或带有可选毛刺滤波器的脉冲计数器。它还可以在大多数系统复位事件中继续运行，使其可以用作日常时间计数器。

LPTMR 模块具有以下特点：

- 带比较功能的 16 位时间计数器或脉冲计数器
  - 可选中断可以从任何低功耗模式生成异步唤醒
  - 硬件触发输出
  - 计数器支持自由运行模式或比较复位
- 用于预分频器/毛刺滤波器的可配置时钟源
- 脉冲计数器的可配置输入源

2.2.9 CRC

该器件包含一个循环冗余校验(CRC)模块，可生成 16/32 位 CRC 码用于错误检测。

CRC 模块提供了实现 16 位或 32 位 CRC 标准所需的可编程多项式、WAS 和其他参数。

CRC 模块具有以下特点：

- 使用 16 位或 32 位可编程移位寄存器的硬件 CRC 生成器电路
- 可编程初始种子值和多项式
- 逐位或逐字节转置输入数据或输出数据（CRC 结果）的选项
- 最终 CRC 结果的反相选项
- 32 位 CPU 寄存器编程接口

2.2.10 LPUART

本产品包含三个低功耗 UART 模块，可以在停止和 VLPS 模式下工作。该模块还支持 4 倍至 32 倍的数据过采样率，以满足不同的应用。

LPUART 模块具有以下特点：

- 可编程波特率（13 位模分频器），具有从 4 倍到 32 倍的可配置过采样率
- 发送和接收波特率可以与总线时钟异步工作，并且可以独立于总线时钟频率进行配置，支持在停止模式下工作
- 中断、DMA 或轮询操作
- 硬件奇偶校验生成和检查
- 可编程 8 位、9 位或 10 位字符长度
- 可编程 1 位或 2 位停止位
- 三种接收器唤醒方式
    - 空闲线路唤醒
    - 地址标记唤醒
    - 接收数据匹配
- 自动地址匹配，以减少 ISR 开销：
    - 地址标记匹配
    - 空闲线路地址匹配
    - 地址匹配开始，地址匹配结束
- 可选的 13 位中断字符生成/11 位中断字符检测
- 可配置的空闲长度检测，支持 1、2、4、8、16、32、64 或 128 个空闲字符
- 可选择的发射器输出和接收器输入极性

2.2.11 LPSPI

该器件包含两个 LPSPI 模块。LPSPI 是一种低功耗串行外设接口(SPI)模块，支持 SPI 总线的高效接口作为 Master 和/或 Slave。如果有适当的时钟可用，LPSPI 可以继续在停止模式下工作，并且设计通过 FIFO 寄存器访问的 DMA 分流实现低 CPU 开销。

LPSPI 模块具有以下特点：

- 4 个字的命令/发送 FIFO
- 4 个字的接收 FIFO
- 主机请求输入可用于控制 SPI 总线传输的开始时间

2.2.12 LPI2C

该器件包含两个 LPI2C 模块。LPI2C 是一种低功耗的内部集成电路(I2C)模块，它支持 I2C 总线的高效接口作为 Master 和/或 Slave。如果有适当的时钟可用，LPI2C 可以继续在停止模式下工作，并且设计通过 FIFO 寄存器访问的 DMA 分流实现低 CPU 开销。LPI2C 实现了对标准模式、快速模式、快速模式+和超快速工作模式的逻辑支持。LPI2C 模块还符合*系统管理总线(SMBus)规范第 2 版*。

LPI2C 模块具有以下特点：

- 支持标准、快速、快速+和超快速模式
- Slave 模式下支持 HS 模式
- 多 Master 支持，包括同步和仲裁
- 时钟延伸
- 一般调用、7 位和 10 位寻址
- 软件复位、起始字节和器件 ID 需要软件支持
- 对于 Master 模式：
  - 4 个字的命令/发送 FIFO
  - 4 个字的接收 FIFO
- 对于 Slave 模式：
  - 独立的 I2C Slave 寄存器，以最大限度地减少由于 Master/Slave 切换导致的软件开销
  - 支持 7 位或 10 位寻址、地址范围、SMBus 报警和一般调用地址
  - 支持中断或 DMA 请求的发送/接收数据寄存器

2.2.13 FlexIO

FlexIO 是一个高度可配置的模块，提供广泛的协议，包括但不限于 UART、I2C、SPI、Camera IF、LCD RGB、PWM/波形生成。该模块支持独立于总线时钟频率的可编程波特率，具有自动启动/停止位生成功能。

FlexIO 模块具有以下特点：

- 在 VLPR/VLPW/停止/VLPS 模式下正常工作，前提是它使用的时钟保持使能状态
- 四个 32 位双缓冲移位寄存器，具有发送、接收和数据匹配模式以及连续数据传输
- 移位器的移位、加载和存储事件的时序由分配给移位器的高度灵活的 16 位定时器控制
- 可以连接使用两个或多个移位器，以支持大的数据传输大小
- 每个 16 位定时器独立运行，支持在各种内部或外部触发条件下进行复位、使能和禁用，具有可编程的触发极性
- 灵活的引脚配置，支持输出禁用、开漏、双向输出数据和输出模式
- 支持中断、DMA 或轮询的发送/接收操作

2.2.14 端口控制和 GPIO

端口控制和中断(PORT)模块支持端口控制、数字滤波和外部中断功能。当引脚配置为 GPIO 功能时，GPIO 数据方向和输出数据寄存器控制每个引脚的方向和输出数据。当引脚配置为任何数字功能时，GPIO 输入数据寄存器显示每个引脚上的逻辑值，前提是该引脚对应的端口控制和中断模块已使能。

下图显示了基本的 I/O 引脚结构。当配置为开漏工作时，伪开漏引脚会禁用 P 沟道输出驱动器。任何 I/O 引脚，包括开漏和伪开漏引脚，都不允许超过 VDD。

注意

RESET_b 引脚也是具有伪开漏的普通 I/O 引脚。

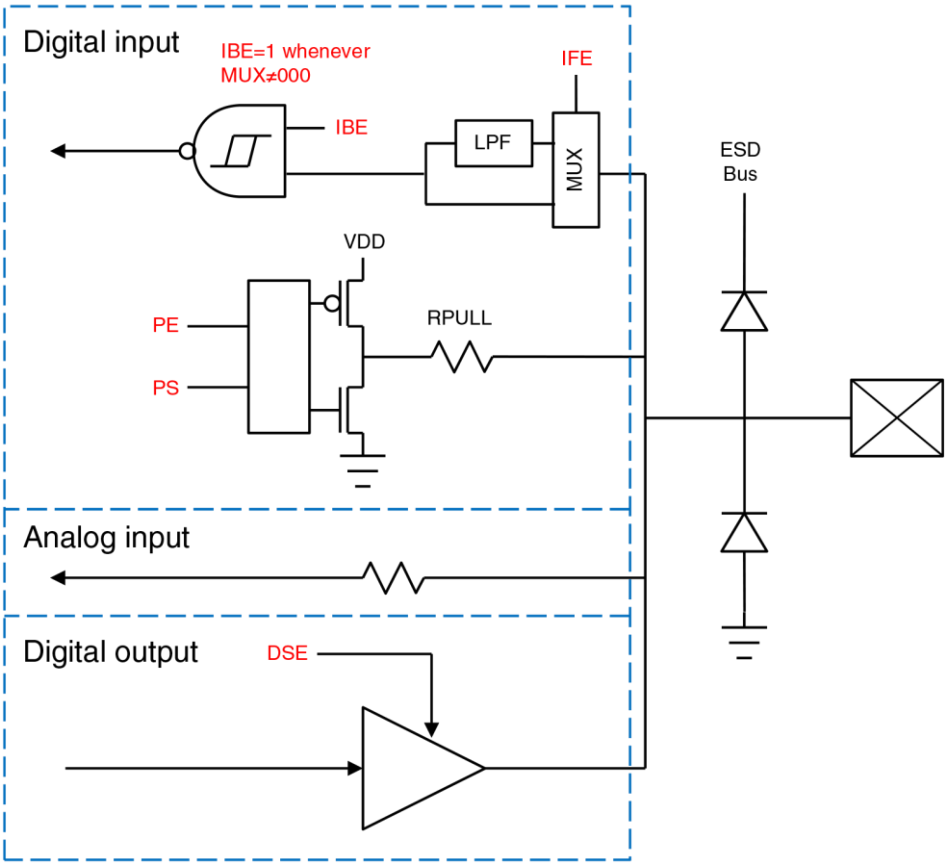


图 5.I/O 简化功能框图

PORT 模块具有以下特点：

- 所有 PIN 支持中断使能
- 可配置边沿（上升、下降或两者）或电平敏感中断类型
- 支持 DMA 请求
- 低功耗模式下异步唤醒
- 选定引脚上可配置的上拉、下拉和上拉禁用
- 选定引脚上可配置的高和低驱动强度
- 选定引脚上可配置的无源滤波器
- 支持模拟或引脚禁用、GPIO 以及芯片特定数字功能的单个多路复用器控制字段
- 引脚配置字段在所有数字引脚复用模式下都有效

GPIO 模块具有以下特点：

- 端口数据输入寄存器在所有数字引脚复用模式下可见
- 具有相应置 1/清 0/翻转寄存器的端口数据输出寄存器
- 端口数据方向寄存器
- GPIO 支持通过快速 GPIO 进行单周期访问

3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. For more details of the system memory and peripheral locations, see the Memory Map chapter in the Reference Manual.

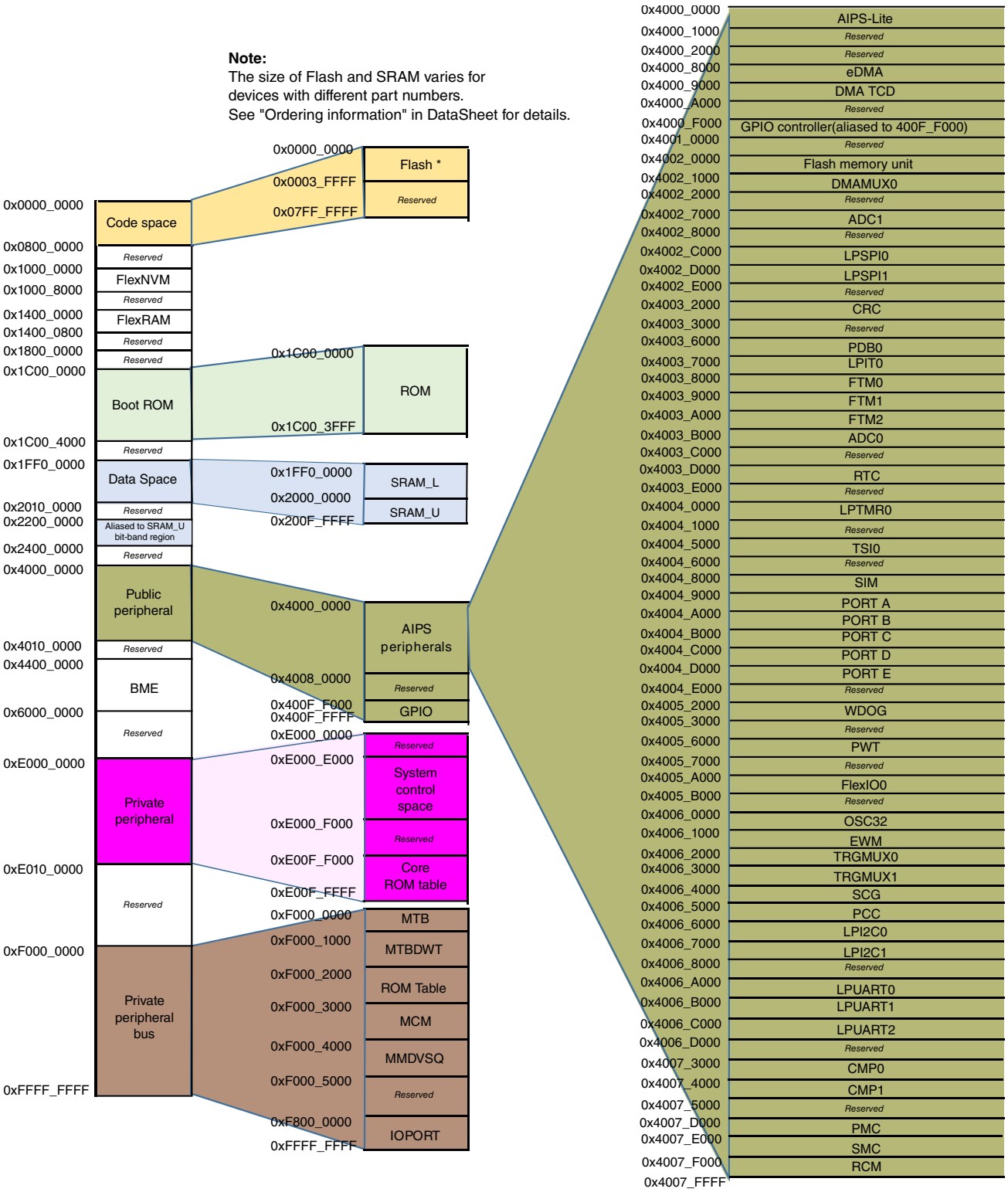


Figure 6. Memory map

4 Pinouts

4.1 KE1xZ Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

On this device, there are several special ADC channels which support hardware interleave between multiple ADCs. Taking ADC0_SE4 and ADC1_SE14 channels as an example, these two channels can work independently, but they can also be hardware interleaved. In the hardware interleaved mode, a signal on the pin PTB0 can be sampled by both ADC0 and ADC1. The interleaved mode is enabled by SIM_CHIPCTL[ADC_INTERLEAVE_EN] bits. For more information, see "ADC Hardware Interleaved Channels" in the ADC chapter of Reference Manual.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	10	VREFL/ VSS	VREFL/ VSS	VREFL/ VSS							
1	—	PTE16	DISABLED		PTE16					FXIO_D3	TRGMUX_ OUT7
2	—	PTE15	DISABLED		PTE15					FXIO_D2	TRGMUX_ OUT6
3	1	PTD1	TSI0_CH5	TSI0_CH5	PTD1	FTM0_CH3	LPSPI1_SIN	FTM2_CH1		FXIO_D1	TRGMUX_ OUT2
4	2	PTD0	TSI0_CH4	TSI0_CH4	PTD0	FTM0_CH2	LPSPI1_SCK	FTM2_CH0		FXIO_D0	TRGMUX_ OUT1
5	3	PTE11	TSI0_CH3	TSI0_CH3	PTE11	PWT_IN1	LPTMR0_ ALT1			FXIO_D5	TRGMUX_ OUT5
6	4	PTE10	TSI0_CH2	TSI0_CH2	PTE10	CLKOUT				FXIO_D4	TRGMUX_ OUT4
7	—	PTE13	DISABLED		PTE13						
8	5	PTE5	TSI0_CH0	TSI0_CH0	PTE5	TCLK2	FTM2_QD_ PHA	FTM2_CH3		FXIO_D7	EWM_IN
9	6	PTE4	TSI0_CH1	TSI0_CH1	PTE4	BUSOUT	FTM2_QD_ PHB	FTM2_CH2		FXIO_D6	EWM_OUT_b

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
10	7	VDD	VDD	VDD							
11	8	VDDA	VDDA	VDDA							
12	9	VREFH	VREFH	VREFH							
13	—	VREFL	VREFL	VREFL							
14	—	VSS	VSS	VSS							
15	11	PTB7	EXTAL	EXTAL	PTB7	LPI2C0_SCL					
16	12	PTB6	XTAL	XTAL	PTB6	LPI2C0_SDA					
17	—	PTE14	DISABLED		PTE14	FTM0_FLT1					
18	13	PTE3	TSI0_CH24	TSI0_CH24	PTE3	FTM0_FLT0	LPUART2_ RTS			TRGMUX_IN6	
19	—	PTE12	DISABLED		PTE12	FTM0_FLT3	LPUART2_TX				
20	—	PTD17	DISABLED		PTD17	FTM0_FLT2	LPUART2_RX				
21	14	PTD16	DISABLED		PTD16	FTM0_CH1					
22	15	PTD15	DISABLED		PTD15	FTM0_CH0					
23	16	PTE9	DAC0_OUT	DAC0_OUT	PTE9	FTM0_CH7	LPUART2_ CTS				
24	—	PTD14	DISABLED		PTD14						CLKOUT
25	—	PTD13	DISABLED		PTD13						RTC_CLKOUT
26	17	PTE8	ACMP0_IN3/ TSI0_CH11	ACMP0_IN3/ TSI0_CH11	PTE8	FTM0_CH6					
27	18	PTB5	TSI0_CH9	TSI0_CH9	PTB5	FTM0_CH5	LPSPI0_PCS1			TRGMUX_IN0	ACMP1_OUT
28	19	PTB4	ACMP1_IN2/ TSI0_CH8	ACMP1_IN2/ TSI0_CH8	PTB4	FTM0_CH4	LPSPI0_SOUT			TRGMUX_IN1	
29	20	PTC3	ADC0_SE11/ ACMP0_IN4/ EXTAL32	ADC0_SE11/ ACMP0_IN4/ EXTAL32	PTC3	FTM0_CH3					
30	21	PTC2	ADC0_SE10/ ACMP0_IN5/ XTAL32	ADC0_SE10/ ACMP0_IN5/ XTAL32	PTC2	FTM0_CH2					
31	22	PTD7	TSI0_CH10	TSI0_CH10	PTD7	LPUART2_TX		FTM2_FLT3			
32	23	PTD6	TSI0_CH7	TSI0_CH7	PTD6	LPUART2_RX		FTM2_FLT2			
33	24	PTD5	TSI0_CH6	TSI0_CH6	PTD5	FTM2_CH3	LPTMR0_ ALT2		PWT_IN2	TRGMUX_IN7	
34	—	PTD12	DISABLED		PTD12	FTM2_CH2	LPI2C1_HREQ			LPUART2_ RTS	
35	—	PTD11	DISABLED		PTD11	FTM2_CH1	FTM2_QD_ PHA			LPUART2_ CTS	
36	—	PTD10	DISABLED		PTD10	FTM2_CH0	FTM2_QD_ PHB				
37	—	VSS	VSS	VSS							
38	—	VDD	VDD	VDD							
39	25	PTC1	ADC0_SE9/ ACMP1_IN3/ TSI0_CH23	ADC0_SE9/ ACMP1_IN3/ TSI0_CH23	PTC1	FTM0_CH1					

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
40	26	PTC0	ADC0_SE8/ ACMP1_IN4/ TSI0_CH22	ADC0_SE8/ ACMP1_IN4/ TSI0_CH22	PTC0	FTM0_CH0					
41	—	PTD9	ACMP1_IN5	ACMP1_IN5	PTD9	LPI2C1_SCL		FTM2_FLT3			
42	—	PTD8	DISABLED		PTD8	LPI2C1_SDA		FTM2_FLT2			
43	27	PTC17	ADC0_SE15	ADC0_SE15	PTC17	FTM1_FLT3		LPI2C1_SCLS			
44	28	PTC16	ADC0_SE14	ADC0_SE14	PTC16	FTM1_FLT2		LPI2C1_SDAS			
45	29	PTC15	ADC0_SE13	ADC0_SE13	PTC15	FTM1_CH3					
46	30	PTC14	ADC0_SE12	ADC0_SE12	PTC14	FTM1_CH2					
47	31	PTB3	ADC0_SE7/ TSI0_CH21	ADC0_SE7/ TSI0_CH21	PTB3	FTM1_CH1	LPSPI0_SIN	FTM1_QD_ PHA		TRGMUX_IN2	
48	32	PTB2	ADC0_SE6/ TSI0_CH20	ADC0_SE6/ TSI0_CH20	PTB2	FTM1_CH0	LPSPI0_SCK	FTM1_QD_ PHB		TRGMUX_IN3	
49	—	PTC13	DISABLED		PTC13						
50	—	PTC12	DISABLED		PTC12						
51	—	PTC11	DISABLED		PTC11						
52	—	PTC10	DISABLED		PTC10						
53	33	PTB1	ADC0_SE5	ADC0_SE5	PTB1	LPUART0_TX	LPSPI0_SOUT	TCLK0			
54	34	PTB0	ADC0_SE4	ADC0_SE4	PTB0	LPUART0_RX	LPSPI0_PCS0	LPTMR0_ ALT3	PWT_IN3		
55	35	PTC9	DISABLED		PTC9	LPUART1_TX				LPUART0_ RTS	
56	36	PTC8	DISABLED		PTC8	LPUART1_RX				LPUART0_ CTS	
57	37	PTA7	ADC0_SE3/ ACMP1_IN1	ADC0_SE3/ ACMP1_IN1	PTA7	FTM0_FLT2		RTC_CLKIN		LPUART1_ RTS	
58	38	PTA6	ADC0_SE2/ ACMP1_IN0	ADC0_SE2/ ACMP1_IN0	PTA6	FTM0_FLT1	LPSPI1_PCS1			LPUART1_ CTS	
59	39	PTE7	DISABLED		PTE7	FTM0_CH7					
60	40	VSS	VSS	VSS							
61	41	VDD	VDD	VDD							
62	—	PTA17	DISABLED		PTA17	FTM0_CH6		EWM_OUT_b			
63	—	PTB17	DISABLED		PTB17	FTM0_CH5	LPSPI1_PCS3				
64	—	PTB16	DISABLED		PTB16	FTM0_CH4	LPSPI1_SOUT				
65	—	PTB15	DISABLED		PTB15	FTM0_CH3	LPSPI1_SIN				
66	—	PTB14	ADC1_SE9	ADC1_SE9	PTB14	FTM0_CH2	LPSPI1_SCK				
67	42	PTB13	ADC1_SE8	ADC1_SE8	PTB13	FTM0_CH1					
68	43	PTB12	ADC1_SE7	ADC1_SE7	PTB12	FTM0_CH0					
69	44	PTD4	ADC1_SE6	ADC1_SE6	PTD4	FTM0_FLT3					
70	45	PTD3	NMI_b	ADC1_SE3	PTD3		LPSPI1_PCS0	FXIO_D5		TRGMUX_IN4	NMI_b
71	46	PTD2	ADC1_SE2	ADC1_SE2	PTD2		LPSPI1_SOUT	FXIO_D4		TRGMUX_IN5	
72	47	PTA3	ADC1_SE1	ADC1_SE1	PTA3		LPI2C0_SCL	EWM_IN		LPUART0_TX	

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
73	48	PTA2	ADC1_SE0	ADC1_SE0	PTA2		LPI2C0_SDA	EWM_OUT_b		LPUART0_RX	
74	—	PTB11	DISABLED		PTB11		LPI2C0_HREQ				
75	—	PTB10	DISABLED		PTB10		LPI2C0_SDAS				
76	—	PTB9	DISABLED		PTB9		LPI2C0_SCLS				
77	—	PTB8	DISABLED		PTB8						
78	49	PTA1	ADC0_SE1/ ACMP0_IN1/ TSI0_CH18	ADC0_SE1/ ACMP0_IN1/ TSI0_CH18	PTA1	FTM1_CH1	LPI2C0_SDAS	FXIO_D3	FTM1_QD_ PHA	LPUART0_ RTS	TRGMUX_ OUT0
79	50	PTA0	ADC0_SE0/ ACMP0_IN0/ TSI0_CH17	ADC0_SE0/ ACMP0_IN0/ TSI0_CH17	PTA0	FTM2_CH1	LPI2C0_SCLS	FXIO_D2	FTM2_QD_ PHA	LPUART0_ CTS	TRGMUX_ OUT3
80	51	PTC7	ADC1_SE5/ TSI0_CH16	ADC1_SE5/ TSI0_CH16	PTC7	LPUART1_TX					
81	52	PTC6	ADC1_SE4/ TSI0_CH15	ADC1_SE4/ TSI0_CH15	PTC6	LPUART1_RX					
82	—	PTA16	DISABLED		PTA16	FTM1_CH3	LPSPI1_PCS2				
83	—	PTA15	DISABLED		PTA15	FTM1_CH2	LPSPI0_PCS3				
84	53	PTE6	ADC1_SE11	ADC1_SE11	PTE6	LPSPI0_PCS2				LPUART1_ RTS	
85	54	PTE2	ADC1_SE10/ TSI0_CH19	ADC1_SE10/ TSI0_CH19	PTE2	LPSPI0_SOUT	LPTMR0_ ALT3		PWT_IN3	LPUART1_ CTS	
86	—	VSS	VSS	VSS							
87	—	VDD	VDD	VDD							
88	—	PTA14	DISABLED		PTA14	FTM0_FLT0		EWM_IN			BUSOUT
89	55	PTA13	DISABLED		PTA13			LPI2C1_SCLS			
90	56	PTA12	DISABLED		PTA12			LPI2C1_SDAS			
91	57	PTA11	DISABLED		PTA11		LPUART0_RX	FXIO_D1			
92	58	PTA10	DISABLED		PTA10		LPUART0_TX	FXIO_D0			
93	59	PTE1	TSI0_CH14	TSI0_CH14	PTE1	LPSPI0_SIN	LPI2C0_HREQ	LPI2C1_SCL			
94	60	PTE0	TSI0_CH13	TSI0_CH13	PTE0	LPSPI0_SCK	TCLK1	LPI2C1_SDA		FTM1_FLT2	
95	61	PTC5	TSI0_CH12	TSI0_CH12	PTC5	FTM2_CH0	RTC_CLKOUT	LPI2C1_HREQ		FTM2_QD_ PHB	
96	62	PTC4	SWD_CLK	ACMP0_IN2	PTC4	FTM1_CH0	RTC_CLKOUT		EWM_IN	FTM1_QD_ PHB	SWD_CLK
97	63	PTA5	RESET_b		PTA5		TCLK1				RESET_b
98	64	PTA4	SWD_DIO		PTA4			ACMP0_OUT	EWM_OUT_b		SWD_DIO
99	—	PTA9	DISABLED		PTA9			FXIO_D7		FTM1_FLT3	
100	—	PTA8	DISABLED		PTA8			FXIO_D6			

4.2 Port control and interrupt summary

The following table provides more information regarding the Port Control and Interrupt configurations.

Table 6. Ports summary

Feature	Port A	Port B	Port C	Port D	Port E
Pull select control	Yes	Yes	Yes	Yes	Yes
Pull select at reset	PTA4/PTA5=Pull up, Others=No	No	PTC4=Pull down, Others=No	PTD3=Pull up, Others=No	No
Pull enable control	Yes	Yes	Yes	Yes	Yes
Pull enable at reset	PTA4/ PTA5=Enabled; Others=Disabled	Disabled	PTC4=Enabled; Others=Disabled	PTD3=Enabled; Others=Disabled	Disabled
Passive filter enable control	PTA5=Yes; Others=No	No	No	PTD3=Yes; Others=No	No
Passive filter enable at reset	PTA5=Enabled; Others=Disabled	Disabled	Disabled	Disabled	Disabled
Open drain enable control	I2C and UART Tx=Enabled; Others=Disabled	I2C and UART Tx=Enabled; Others=Disabled	I2C and UART Tx=Enabled; Others=Disabled	I2C and UART Tx=Enabled; Others=Disabled	I2C and UART Tx=Enabled; Others=Disabled
Open drain enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Drive strength enable control	No	PTB4/PTB5 only	No	PTD0/PTD1/ PTD15/PTD16 only	PTE0/PTE1 only
Drive strength enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Pin mux control	Yes	Yes	Yes	Yes	Yes
Pin mux at reset	PTA4/PTA5=ALT7; Others=ALT0	ALT0	PTC4=ALT7; Others=ALT0	PTD3=ALT7; Others=ALT0	ALT0
Lock bit	Yes	Yes	Yes	Yes	Yes
Interrupt and DMA request	Yes	Yes	Yes	Yes	Yes
Digital glitch filter	No	No	No	No	Yes

4.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

4.3.1 Core Modules

Table 7. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_CLK	SWD_CLK	Serial Wire Clock	I
SWD_DIO	SWD_DIO	Serial Wire Data	I/O

4.3.2 System Modules

Table 8. System Signal Descriptions

Chip signal name	Module signal name	Description	I/O
NMI_b	—	Non-maskable interrupt NOTE: Driving the NMI signal low forces a non-maskable interrupt, if the NMI function is selected on the corresponding pin.	I
RESET_b	—	Reset bidirectional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

Table 9. EWM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_IN is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT_b	$\overline{\text{EWM\_out}}$	EWM reset out signal	O

4.3.3 Clock Modules

Table 10. OSC (in SCG) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL	EXTAL	External clock/Oscillator input	I
XTAL	XTAL	Oscillator output	O

Table 11. RTC Oscillator (OSC32) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O

4.3.4 Analog

Table 12. ADC*0* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ADC*0*_SE[15:0]	AD[15:0]	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I

Table 13. ADC*1* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ADC*1*_SE[11:0]	AD[11:0]	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I

Table 14. ACMP*0* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ACMP*0*_IN[5:0]	IN[5:0]	Analog voltage inputs	I
ACMP*0*_OUT	CMPO	Comparator output	O
DAC0_OUT	—	DAC output	O

Table 15. ACMP*1* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ACMP*1*_IN[5:0]	IN[5:0]	Analog voltage inputs	I
ACMP*1*_OUT	CMPO	Comparator output	O

4.3.5 Timer Modules

Table 16. LPTMR0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR_ALT*n*	Pulse Counter Input pin	I

Table 17. RTC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
RTC_CLKOUT	RTC_CLKOUT	1 Hz square-wave output or 32 kHz clock	O

Table 18. FTM*0* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM*0*_CH[7:0]	CHn	FTM channel (n), where n can be 7-0	I/O
FTM*0*_FLT[3:0]	FAULTj	Fault input (j), where j can be 3-0	I
TCLK[2:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I

Table 19. FTM*1* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM*1*_CH[3:0]	CHn	FTM channel (n), where n can be 3-0	I/O
FTM*1*_FLT[3:2]	FAULTj	Fault input (j), where j can be 3-2	I
TCLK[2:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I

Table 20. FTM*2* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM*2*_CH[3:0]	CHn	FTM channel (n), where n can be 3-0	I/O
FTM*2*_FLT[3:2]	FAULTj	Fault input (j), where j can be 3-2	I
TCLK[2:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I

4.3.6 Communication Interfaces

Table 21. LPSPI*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPSPI*n*_SOUT	SOUT	Serial Data Out	O
LPSPI*n*_SIN	SIN	Serial Data In	I
LPSPI*n*_SCK	SCK	Serial Clock	I/O
LPSPI*n*_PCS[3:0]	PCS[3:0]	Peripheral Chip Select 0-3	I/O

Table 22. LPI2C*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPI2C*n*_SCL	SCL	Bidirectional serial clock line of the I2C system.	I/O
LPI2C*n*_SDA	SDA	Bidirectional serial data line of the I2C system.	I/O
LPI2C*n*_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C*n*_SCLS	SCLS	Secondary I2C clock line.	I/O
LPI2C*n*_SDAS	SDAS	Secondary I2C data line.	I/O

Table 23. LPUART*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART*n*_TX	LPUART_TXD	Transmit data	I/O
LPUART*n*_RX	LPUART_RXD	Receive data	I
LPUART*n*_CTS	LPUART_CTS	Clear to send	I
LPUART*n*_RTS	LPUART_RTS	Request to send	O

Table 24. FlexIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FXIO_D[7:0]	FXIO_D[7:0]	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

4.3.7 Human-Machine Interfaces (HMI)

Table 25. GPIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PTA[17:0]	PORTA17–PORTA0	General-purpose input/output	I/O
PTB[17:0]	PORTB17–PORTB0	General-purpose input/output	I/O
PTC[17:0]	PORTC17–PORTC0	General-purpose input/output	I/O
PTD[17:0]	PORTD17–PORTD0	General-purpose input/output	I/O
PTE[16:0]	PORTE16–PORTE0	General-purpose input/output	I/O

Table 26. TSI0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TSI0_CH[24:0]	TSI[24:0]	TSI sensing pins or GPIO pins	I/O

4.4 Pinout diagram

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous table of Pin Assignments.

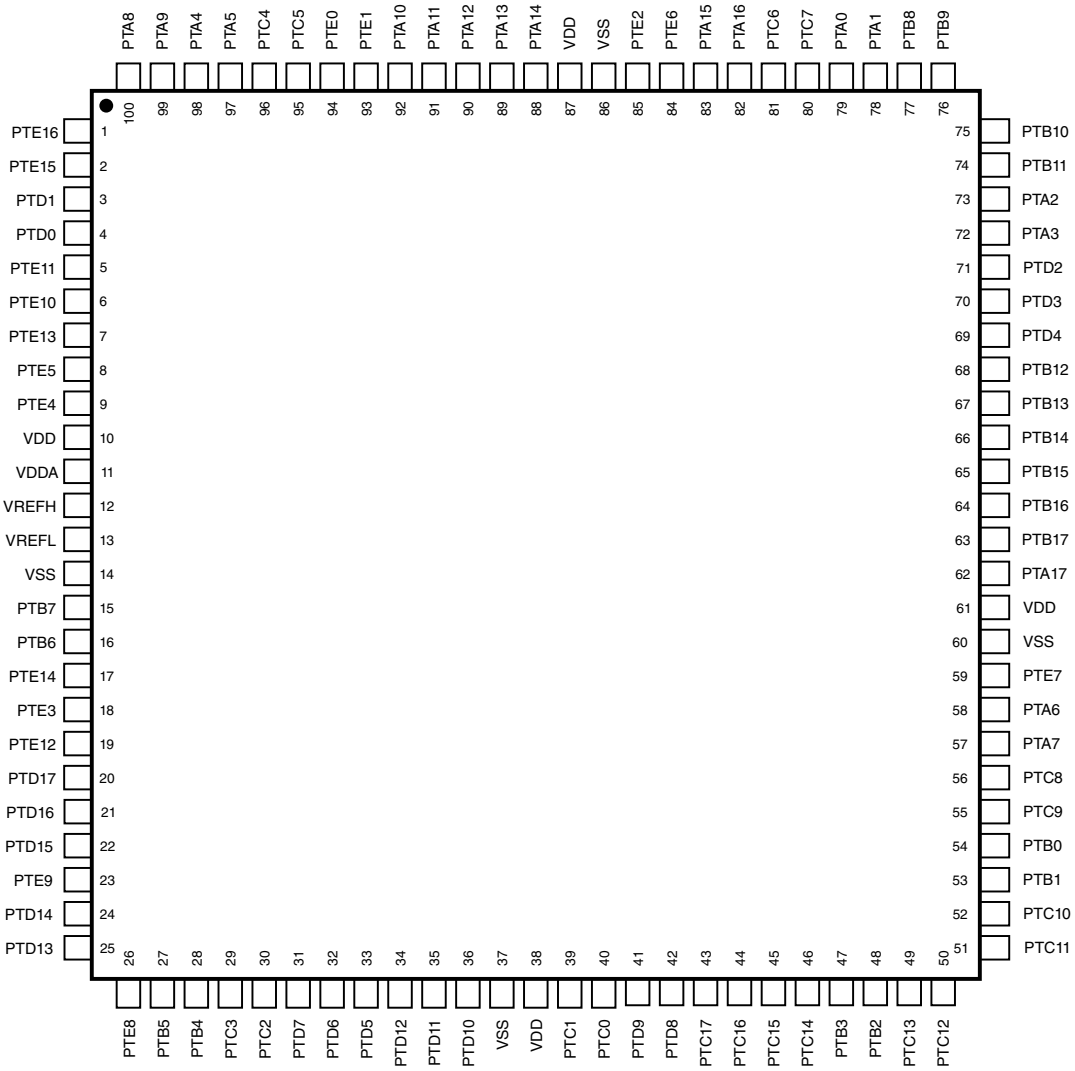


Figure 7. 100 LQFP Pinout Diagram

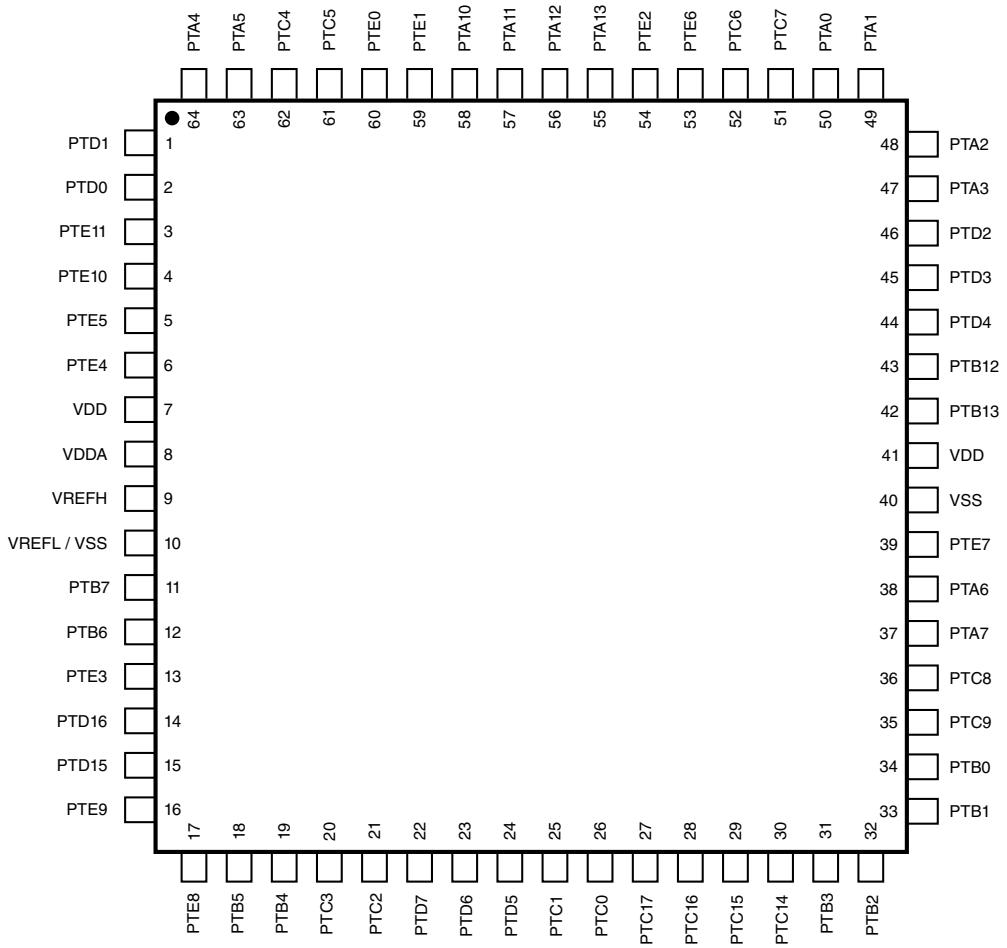


Figure 8. 64 LQFP Pinout Diagram

4.5 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.

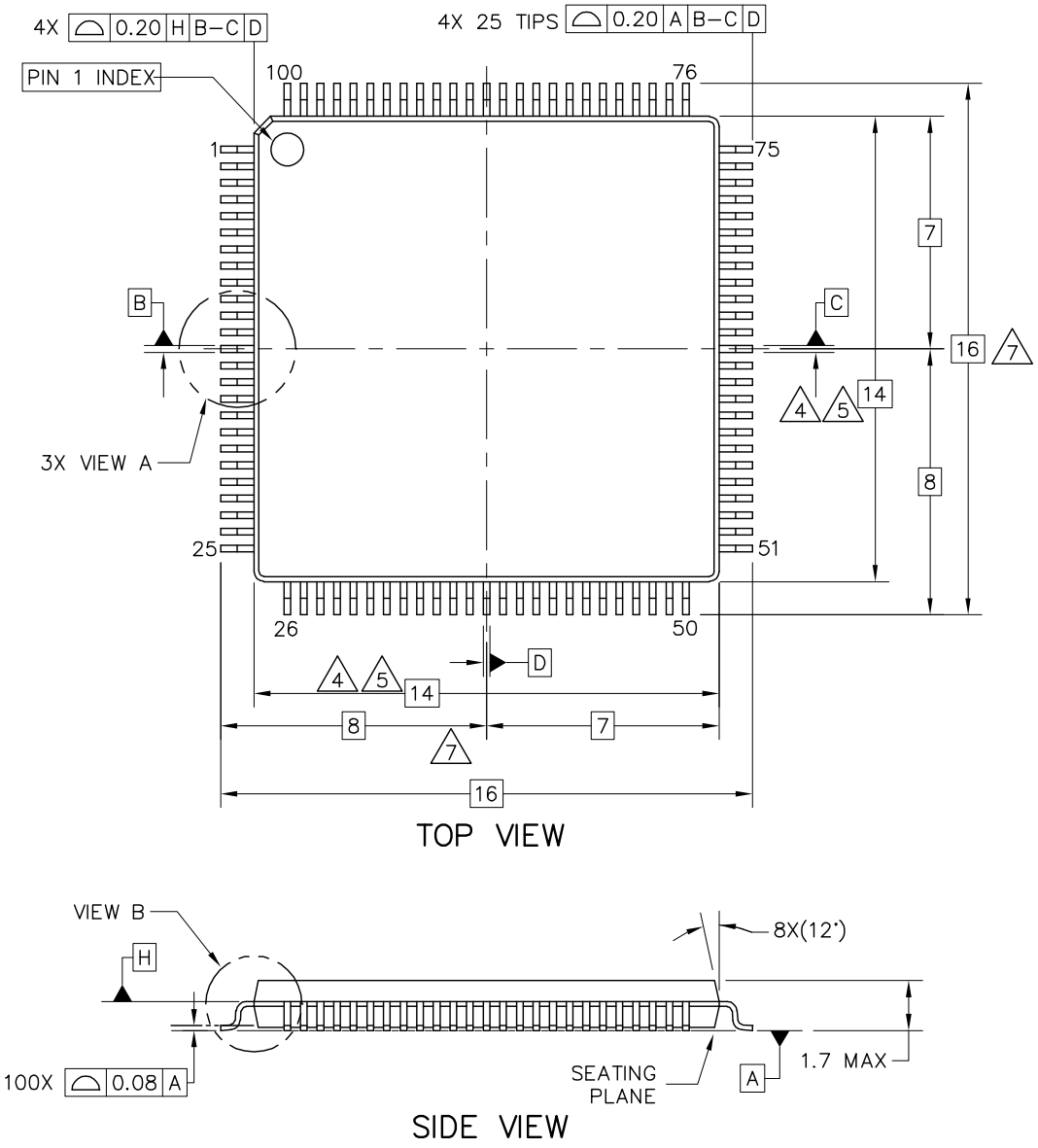
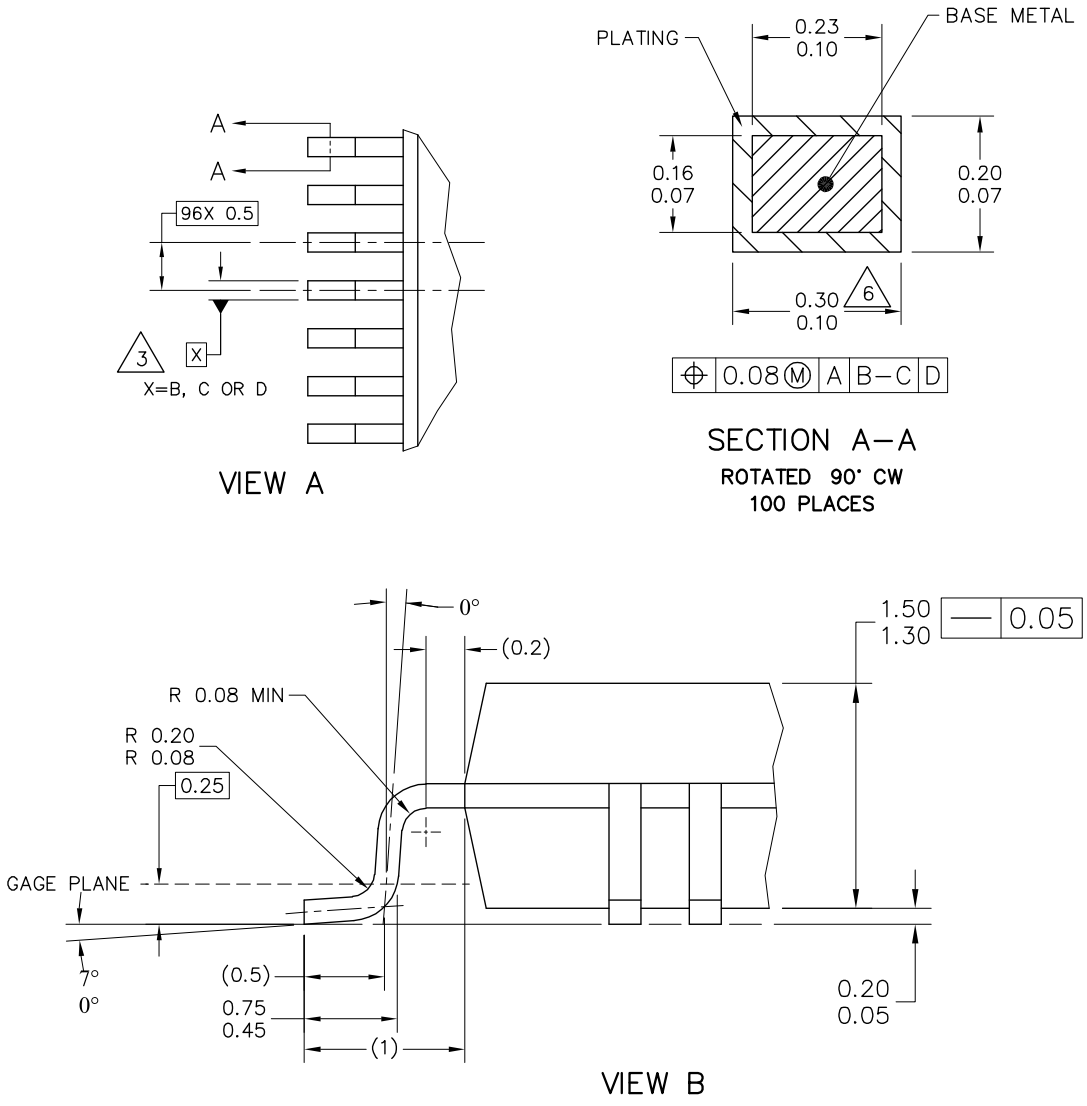


Figure 9. 100-pin LQFP package dimensions 1



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.
5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 10. 100-pin LQFP package dimensions 2

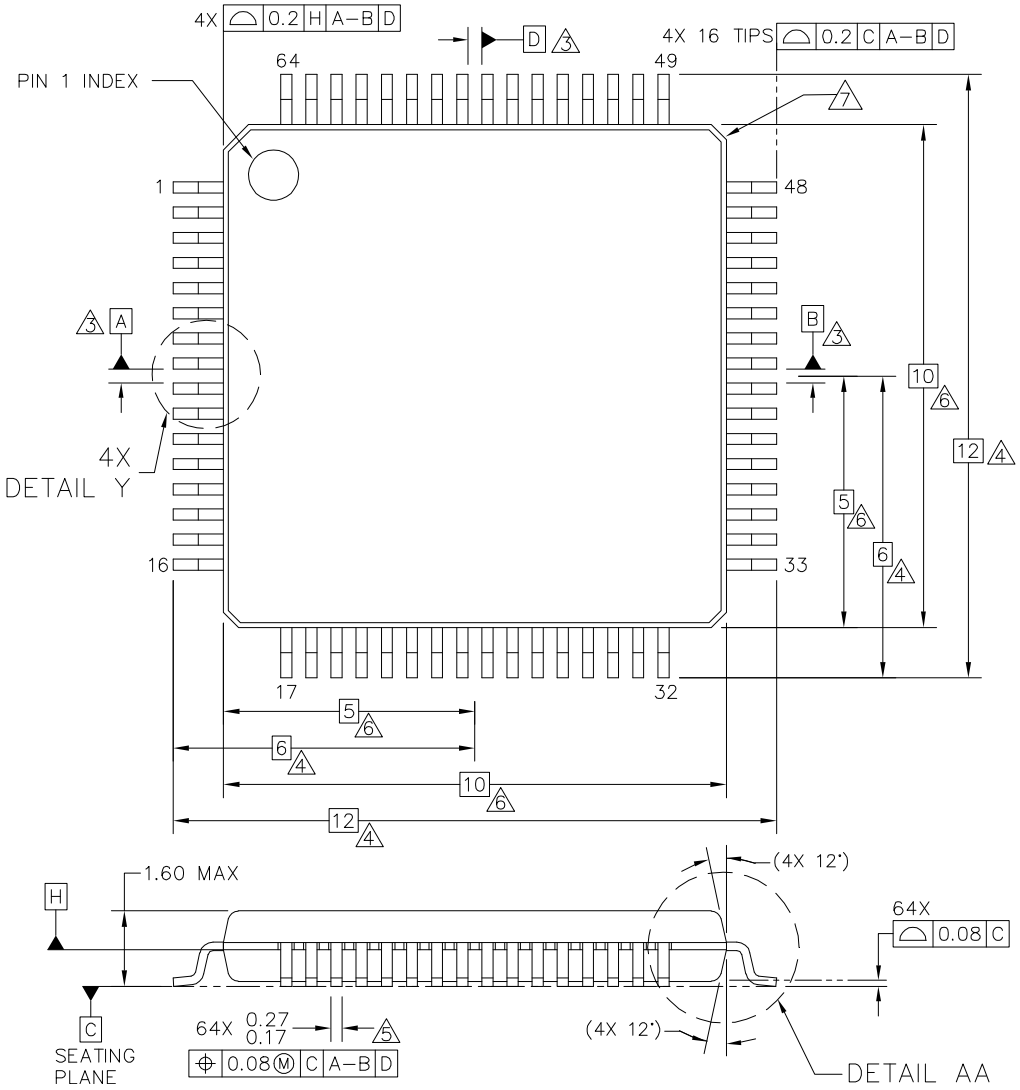
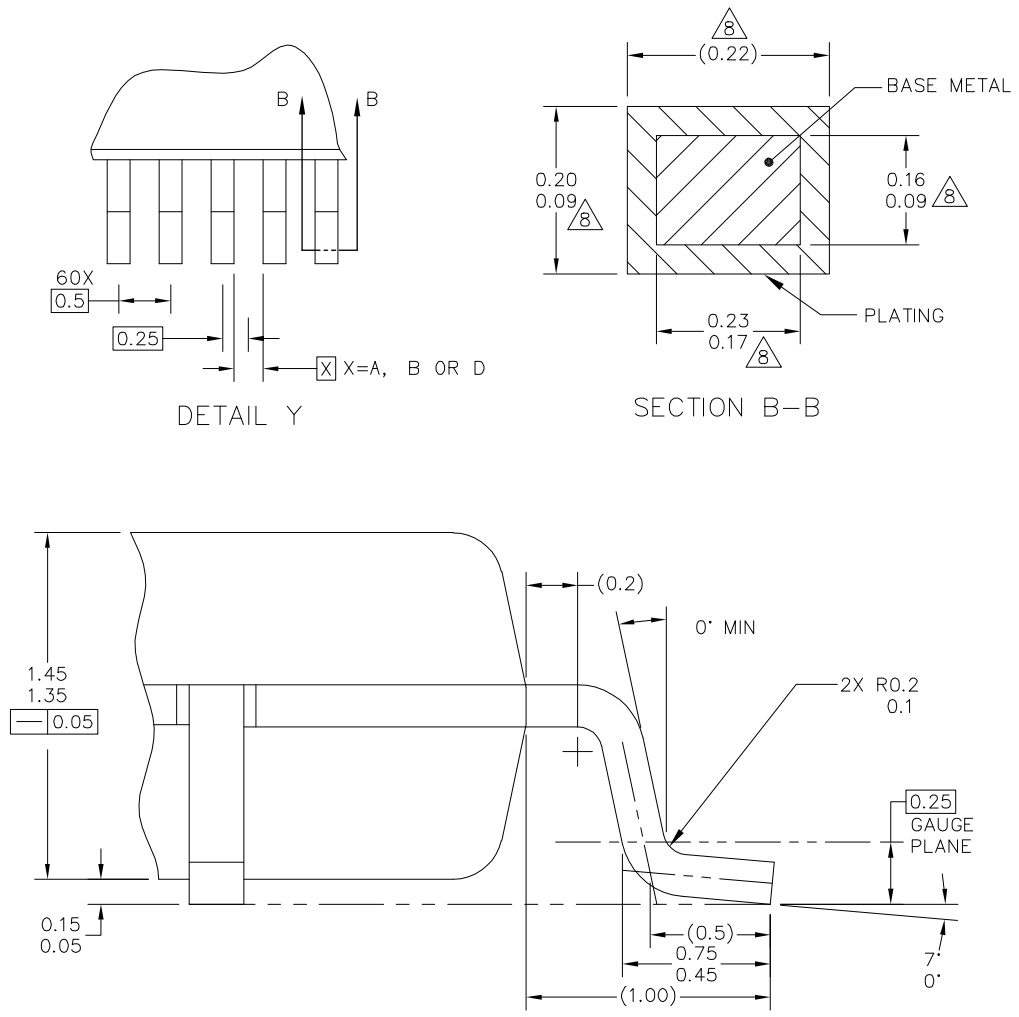


Figure 11. 64-pin LQFP package dimensions 1



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 12. 64-pin LQFP package dimensions 2

5 Electrical characteristics

5.1 Terminology and guidelines

5.1.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

5.1.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

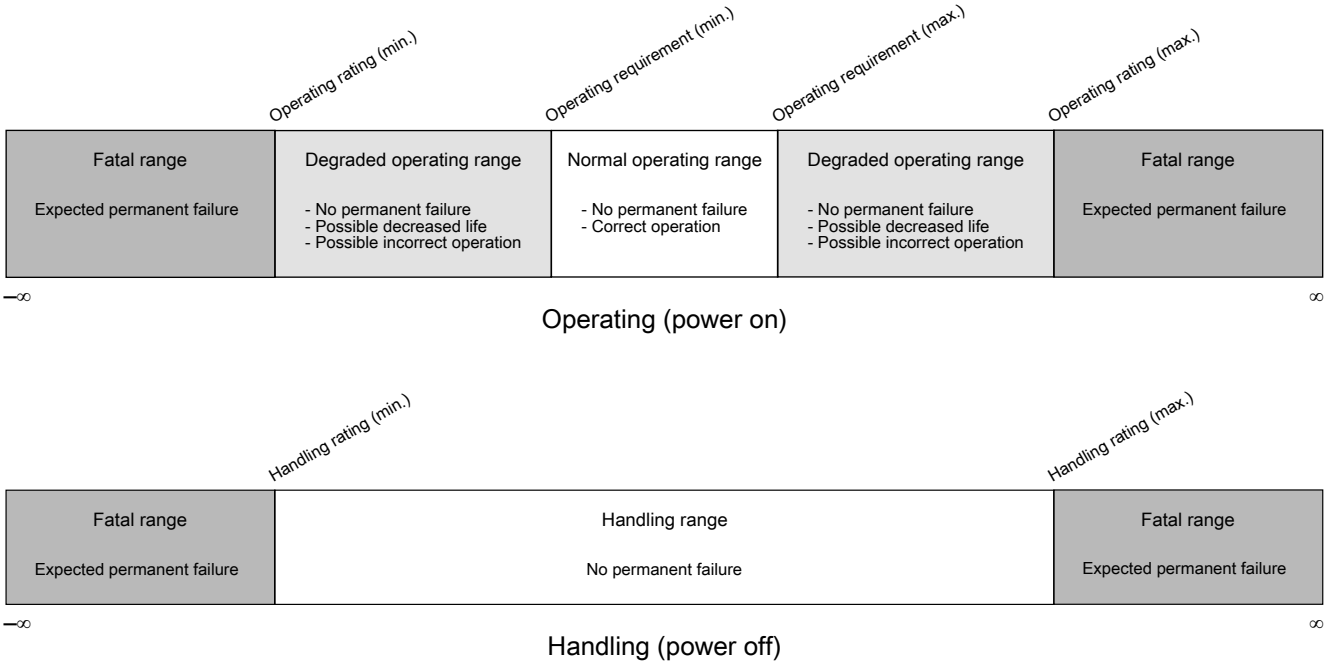
Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

5.1.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	5.0	V

5.1.4 Relationship between ratings and operating requirements



5.1.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.2 Ratings

5.2.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	– 6000	6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I_{LAT}	Latch-up current at ambient temperature upper limit	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.2.4 Voltage and current operating ratings

NOTE

Functional operating conditions appear in the "DC electrical specifications". Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 27. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	–0.3	5.8 [1]	V
I_{DD}	Digital supply current	—	60	mA

Table continues on the next page...

Table 27. Voltage and current operating ratings (continued)

Symbol	Description	Min.	Max.	Unit
V_{IO}	IO pin input voltage	V_{SS} – 0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.1	V_{DD} + 0.1	V

1. 60s lifetime - No restrictions, i.e. the part can switch.

   10 hours lifetime - Device in reset, i.e. the part cannot switch.

5.3 General

5.3.1 Nonswitching electrical specifications

5.3.1.1 Voltage and current operating requirements

Table 28. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	5.5	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	
V_{DD} – V_{DDA}	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	
V_{SS} – V_{SSA}	V_{SS}-to-V_{SSA} differential voltage	– 0.1	0.1	V	
I_{ICIO}	DC injection current — single pin				
	$V_{IN} < V_{SS}$ - 0.3 V (Negative current injection)	– 3	—	mA	1
	$V_{IN} > V_{DD}$ + 0.3 V (Positive current injection)	—	+ 3	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins	– 25	+ 25	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2

1. All pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{SS} – 0.3V or greater than V_{DD} + 0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{SS} – 0.3V–V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R=[V_{IN}–(V_{DD} + 0.3V)]/|I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.
2. Open drain outputs must be pulled to V_{DD}.

5.3.1.2 DC electrical specifications at 3.3 V Range and 5.0 V Range

Table 29. DC electrical specifications

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{DD}	I/O Supply Voltage [1] @ V_{DD} = 3.3 V	2.7	3.3	4	V	
	@ V_{DD} = 5.0 V	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage @ V_{DD} = 3.3 V	0.7 × V_{DD}	—	V_{DD} + 0.3	V	
	@ V_{DD} = 5.0 V	0.65 × V_{DD}	—	V_{DD} + 0.3	V	
V_{il}	Input Buffer Low Voltage @ V_{DD} = 3.3 V	V_{SS} – 0.3	—	0.3 × V_{DD}	V	
	@ V_{DD} = 5.0 V	V_{SS} – 0.3	—	0.35 × V_{DD}	V	
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_5	Normal drive I/O current source capability measured when pad = (V_{DD} – 0.8 V) @ V_{DD} = 3.3 V	2.8	—	—	mA	
	@ V_{DD} = 5.0 V	4.8	—	—	mA	
Iol_5	Normal drive I/O current sink capability measured when pad = 0.8 V @ V_{DD} = 3.3 V	2.4	—	—	mA	
	@ V_{DD} = 5.0 V	4.4	—	—	mA	
Ioh_20	High drive I/O current source capability measured when pad = (V_{DD} – 0.8 V), [2] @ V_{DD} = 3.3 V	10.8	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
Iol_20	High drive I/O current sink capability measured when pad = 0.8 V[4] @ V_{DD} = 3.3 V	10.1	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
I_leak	Hi-Z (Off state) leakage current (per pin)	—	—	300	nA	5, 6
V_{OH}	Output high voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	V_{DD} – 0.8	—	—	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	V_{DD} – 0.8	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	

Table continues on the next page...

Table 29. DC electrical specifications (continued)

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{OL}	Output low voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	—	—	0.8	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	—	—	0.8	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	—	—	0.8	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	—	—	0.8	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range @ V_{DD} = 3.3 V					8, 7
	All pins other than high drive port pins	—	0.002	0.5	µA	
	High drive port pins	—	0.004	0.5	µA	
	Input leakage current (per pin) for full temperature range @ V_{DD} = 5.5 V					
	All pins other than high drive port pins	—	0.005	0.5	µA	
	High drive port pins	—	0.010	0.5	µA	
R_{PU}	Internal pull-up resistors @ V_{DD} = 3.3 V	20	—	65	kΩ	9
	@ V_{DD} = 5.0 V	20	—	50	kΩ	
R_{PD}	Internal pull-down resistors @ V_{DD} = 3.3 V	20	—	65	kΩ	10
	@ V_{DD} = 5.0 V	20	—	50	kΩ	

1. Max power supply ramp rate is 500 V/ms.
2. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_5 value given above.
3. The 20 mA I/O pin is capable of switching a 50 pF load at up to 40 MHz.
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_5 value given above.
5. Refers to the current that leaks into the core when the pad is in Hi-Z (Off state).
6. Maximum pin leakage current at the ambient temperature upper limit.
7. PTD0, PTD1, PTD15, PTD16, PTB4, PTB5, PTE0 and PTE1 I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
8. Refers to the pin leakage on the GPIOs when they are OFF.
9. Measured at V_{DD} supply voltage = V_{DD} min and input V = V_{SS}
10. Measured at V_{DD} supply voltage = V_{DD} min and input V = V_{DD}

5.3.1.3 Voltage regulator electrical characteristics

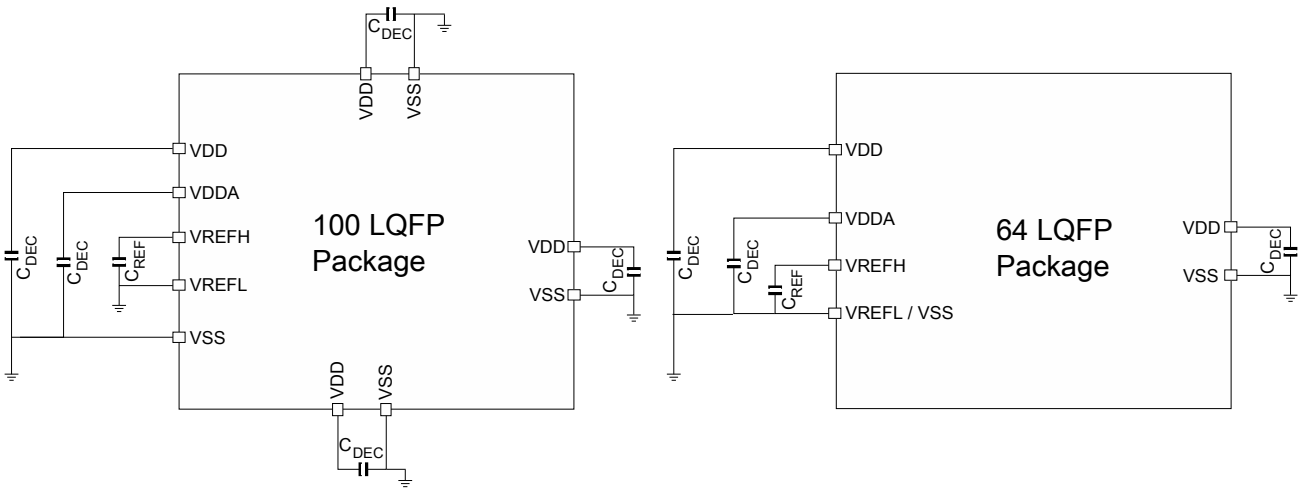


Figure 13. Pinout decoupling

Table 30. Voltage regulator electrical characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF}[1, 2]	ADC reference high decoupling capacitance	—	100	—	nF
C_{DEC}[2, 3]	Recommended decoupling capacitance	—	100	—	nF

1. For improved ADC performance it is recommended to use 1 nF X7R/C0G and 10 nF X7R ceramics in parallel.
2. The capacitors should be placed as close as possible to the VREFH/VREFL pins or corresponding V_{DD}/V_{SS} pins.
3. The requirement and value of of C_{DEC} will be decided by the device application requirement.

5.3.1.4 LVR, LVD and POR operating requirements

Table 31. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and Falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVRX}	LVRX falling threshold (RUN and STOP modes)	2.53	2.58	2.64	V	
V_{LVRX_HYST}	LVRX hysteresis	—	45	—	mV	1
V_{LVRX_LP}	LVRX falling threshold (VLPS/VLPR modes)	1.97	2.12	2.44	V	
$V_{LVRX\_LP\_HYST}$	LVRX hysteresis (VLPS/VLPR modes)	—	40	—	mV	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.88	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	1
V_{LVW}	Falling low-voltage warning threshold	4.19	4.31	4.5	V	
V_{LVW_HYST}	LVW hysteresis		68		mV	1
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

5.3.1.5 Power mode transition operating behaviors

Table 32. Power mode transition operating behaviors

Description	System Clock	Core, Bus, Flash frequency (MHz)	Min.	Typ. (µs)[1]	Max. (µs)[2]
STOP→RUN	FIRC	48, 24, 24	—	7.15	11.8
STOP→RUN	FLL	72, 24, 24	—	7.51	13.4
VLPS→RUN	FIRC	48, 24, 24	—	7.15	11.8
VLPS→RUN	FLL	72, 24, 24	—	9.8	15.9
RUN→VLPR	FLL→SIRC	72, 24, 24→4, 1, 1	—	13.6	14.4
VLPR→RUN	SIRC→FIRC	4, 1, 1→48, 24, 24	—	24	30.7
VLPR→RUN	SIRC→FLL	4, 1, 1→72, 24, 24	—	27	35.7
WAIT→RUN	FIRC	48, 24, 24	—	0.660	0.760
WAIT→RUN	FLL	72, 24, 24	—	0.516	0.653
VLPW→VLPR	SIRC	4, 1, 1	—	20.7	24.9
VLPS→VLPR	SIRC	4, 1, 1	—	17.9	22.8
VLPW→RUN	FIRC (reset value)	48, 24, 24 (reset value)	—	127	146
t_{POR}[3]	FIRC (reset value)	48, 24, 24 (reset value)	—	111	127

1. Typical value is the average of values tested at Temperature=25 °C and V_{DD}=3.3 V.
2. Max value is mean+6×sigma of tested values at the worst case of ambient temperature range and V_{DD} 2.7 V to 5.5 V.
3. After a POR event, the amount of time from the point V_{DD} reaches the reference voltage 2.7 V to execution of the first instruction, across the operating temperature range of the chip.

5.3.1.6 Power consumption

The following table shows the power consumption targets for the device in various modes of operations.

NOTE

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 33. Power consumption operating behaviors

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Unit
RUN	I_{DD_RUN}	LPFLL	Running CoreMark in Flash in **Compute Operation** mode. Core@72MHz, bus @24MHz, flash @24MHz, VDD=5V	25 °C	—	11.19	11.43	mA
				105 °C	—	11.70	12.00	

Table continues on the next page...

Table 33. Power consumption operating behaviors (continued)

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Unit
		LPFLL	Running CoreMark in Flash, all peripheral clock disabled. Core@72MHz, bus @24MHz, flash @24MHz, VDD=5V	25 °C	—	12.15	12.41	
				105 °C	—	12.67	12.99	
		LPFLL	Running CoreMark in Flash, all peripheral clock enabled. Core@72MHz, bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	15.07	15.39	
				105 °C	—	15.53	15.92	
		LPFLL	Running While(1) loop in Flash, all peripheral clock disabled. Core@72MHz, bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	8.81	9.00	
				105 °C	—	9.26	9.49	
		LPFLL	Running While(1) loop in Flash, all peripheral clock enabled. Core@72MHz , bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	11.61	11.83	
				105 °C	—	12.01	12.28	
		IRC48M	Running CoreMark in Flash in **Compute Operation** mode. Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V	25 °C	—	8.50	8.69	
				105 °C	—	8.88	9.08	
		IRC48M	Running CoreMark in Flash, all peripheral clock disabled. Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V	25 °C	—	9.37	9.58	
				105 °C	—	9.76	9.98	
		IRC48M	Running CoreMark in Flash, all peripheral clock enabled. Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	11.52	11.76	
				105 °C	—	11.83	12.08	
		IRC48M	Running While(1) loop in Flash, all peripheral clock disabled. Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	7.00	7.16	
				105 °C	—	7.41	7.58	
VLPR	I_{DD_VLPR}	IRC8M	Very Low Power Run Core Mark in Flash in **Compute Operation** mode. Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V	25 °C	—	1070	1136	µA
		IRC8M	Very Low Power Run Core Mark in Flash, all peripheral clock disabled. Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V	25 °C	—	1110	1178	
		IRC8M	Very Low Power Run Core Mark in Flash, all peripheral clock enabled.	25 °C	—	1260	1338	

Table continues on the next page...

Table 33. Power consumption operating behaviors (continued)

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Unit
			Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V					
		IRC8M	Very Low Power Run While(1) loop in Flash, all peripheral clock disabled. Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V	25 °C	—	747	793	
		IRC8M	Very Low Power Run While(1) loop in Flash, all peripheral clock enabled. Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V	25 °C	—	888	943	
		IRC2M	Very Low Power Run While(1) loop in Flash, all peripheral clock disabled. Core@2MHz, bus @1MHz, flash @1MHz, VDD=5V	25 °C	—	585	621	
		IRC2M	Very Low Power Run While(1) loop in Flash, all peripheral clock enabled. Core@2MHz, bus @1MHz, flash @1MHz, VDD=5V	25 °C	—	682	724	
WAIT	I_{DD_WAIT}	LPFLL	core disabled, system@72MHz, bus @24MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled	25 °C	—	5.95	6.09	mA
		IRC48M	core disabled, system@48 MHz, bus @24MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled	25 °C	—	4.86	4.97	
VLPW	I_{DD_VLPW}	IRC8M	Very Low Power Wait current, core disabled system@4MHz, bus and flash@1MHz, all peripheral clocks disabled, VDD=5V	25 °C	—	657	698	µA
		IRC2M	Very Low Power Wait current, core disabled system@2MHz, bus and flash@1MHz, all peripheral clocks disabled, VDD=5V	25 °C	—	550	584	
STOP	I_{DD_STOP}	-	Stop mode current, VDD=5V, clock bias enabled [2]	25 °C and below	—	27	37	µA
				50 °C	—	45	63	
				85 °C	—	135	189	
				105 °C	—	269	377	
STOP	I_{DD_STOP}	-	Stop mode current, VDD=5V, clock bias disabled [2]	25 °C and below	—	26	36	µA
				50 °C	—	47	66	
				85 °C	—	146	204	

Table continues on the next page...

Table 33. Power consumption operating behaviors (continued)

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Unit
				105 °C	—	277	388	
VLPS	I_{DD_VLPS}	-	Very Low Power Stop current, VDD=5V, clock bias enabled [2]	25 °C and below	—	27	37	µA
				50 °C	—	45	64	
				85 °C	—	134	187	
				105 °C	—	267	375	
VLPS	I_{DD_VLPS}	-	Very Low Power Stop current, VDD=5V, clock bias disabled [2]	25 °C and below	—	21	29	µA
				50 °C	—	29	41	
				85 °C	—	66	92	
				105 °C	—	109	153	

1. These values are based on characterization but not covered by test limits in production.
2. PMC_REGSC[CLKBIASDIS] is the control bit to enable or disable bias under STOP/VLPS mode.

NOTE

CoreMark benchmark compiled using IAR 7.40 with optimization level high, optimized for balanced.

5.3.1.6.1 Low power mode peripheral current adder — typical value

Symbol	Description	Typical
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLPS mode with LPTMR enabled using LPO. Includes LPO power consumption.	366 nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLPS mode with CMP enabled using the 8-bit DAC and a single external input for compare. 8-bit DAC enabled with half VDDA voltage, low speed mode. Includes 8-bit DAC power consumption.	16 µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLPS mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC counter enabled. Includes EXTAL32 (32 kHz external crystal) power consumption.	312 nA
I_{LPUART}	LPUART peripheral adder measured by placing the device in VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. (SIRC 8 MHz)	79 µA
I_{FTM}	FTM peripheral adder measured by placing the device in VLPW mode with selected clock source, outputting the edge aligned PWM of 100 Hz frequency.	45 µA

Table continues on the next page...

Symbol	Description	Typical
I_{ADC}	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in VLPS mode. ADC is configured for low power mode using SIRC clock source, 8-bit resolution and continuous conversions.	484 µA
I_{LPI2C}	LPI2C peripheral adder measured by placing the device in VLPS mode with selected clock source sending START and Slave address, waiting for RX data. Includes the DMA power consumption.	179 µA
I_{LPIT}	LPIT peripheral adder measured by placing the device in VLPS mode with internal SIRC 8 MHz enabled in Stop mode. Includes selected clock source power consumption.	18 µA
I_{LPSPI}	LPSPI peripheral adder measured by placing the device in VLPS mode with selected clock source, output data on SOUT pin with SCK 500 kbit/s. Includes the DMA power consumption.	565 µA

5.3.1.6.2 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- SCG in SOSC for both Run and VLPR modes
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

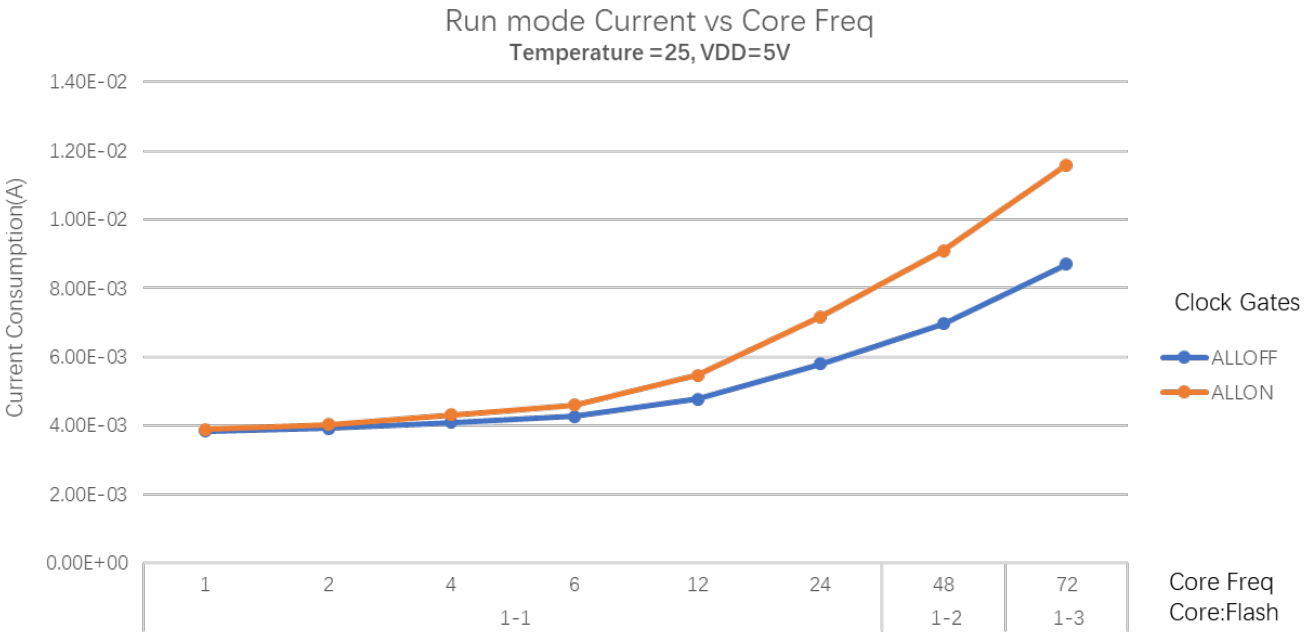


Figure 14. Run mode supply current vs. core frequency

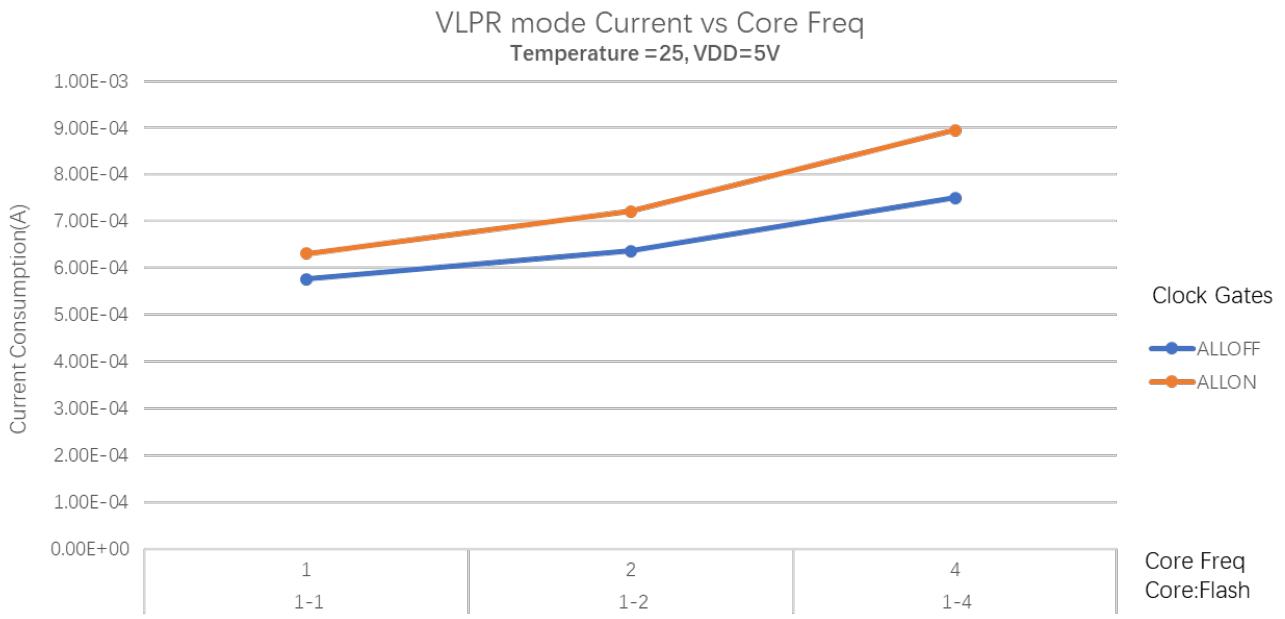


Figure 15. VLPR mode supply current vs. core frequency

5.3.1.7 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following applications notes, available on http://www.nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.3.1.7.1 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5.3.1.7.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to http://www.nxp.com.
2. Perform a keyword search for “EMC design”.
3. Select the "Documents" category and find the application notes.

5.3.1.8 Capacitance attributes

Table 34. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External Oscillator electrical specifications for EXTAL/XTAL pins.

5.3.2 Switching specifications

5.3.2.1 Device clock specifications

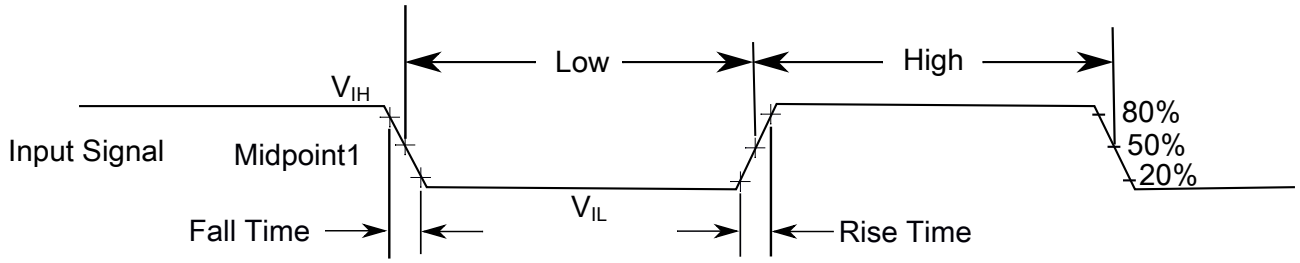
Table 35. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	72	MHz	
f_{BUS}	Bus clock	—	24	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	48	MHz	
VLPR / VLPW mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR}	LPTMR clock	—	13	MHz	

1. The frequency limitations in VLPR / VLPW mode here override any frequency specification listed in the timing specification for any other module.

5.3.2.2 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 16. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Normal drive strength

5.3.2.3 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 36. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.

5.3.2.4 AC specifications at 3.3 V range

Table 37. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	2.7		4	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	17.5	5	17	25
	28	9	32	50
High drive I/O pad	19	5	17	25
	26	9	33	50
CMOS Input [3]	4	1.2	3	0.5

1. Propagation delay measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

NOTE

All measurements were taken accounting for 150 mV drop across VDD and VSS.

5.3.2.5 AC specifications at 5 V range

Table 38. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	4		5.5	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	12	3.6	10	25
	18	8	17	50
High drive I/O pad	13	3.6	10	25
	19	8	19	50
CMOS Input [3]	3	1.2	2.8	0.5

1. As measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

NOTE

All measurements were taken accounting for 150 mV drop across VDD and VSS.

5.3.3 Thermal specifications

5.3.3.1 Thermal operating requirements

Table 39. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

5.3.3.2 Thermal attributes

5.3.3.2.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

5.3.3.2.2 Thermal characteristics for the 64-pin LQFP package

Table 40. Thermal characteristics for the 64-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	62	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	44	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	50	°C/W

Table continues on the next page...

Table 40. Thermal characteristics for the 64-pin LQFP package (continued)

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	37	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	26	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	14	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.3 Thermal characteristics for the 100-pin LQFP package

Table 41. Thermal characteristics for the 100-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	59	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	46	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	49	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	40	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	31	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	16	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.4 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

5.4 Peripheral operating requirements and behaviors

5.4.1 System modules

There are no specifications necessary for the device's system modules.

5.4.2 Clock interface modules

5.4.2.1 Oscillator electrical specifications

5.4.2.1.1 External Oscillator electrical specifications

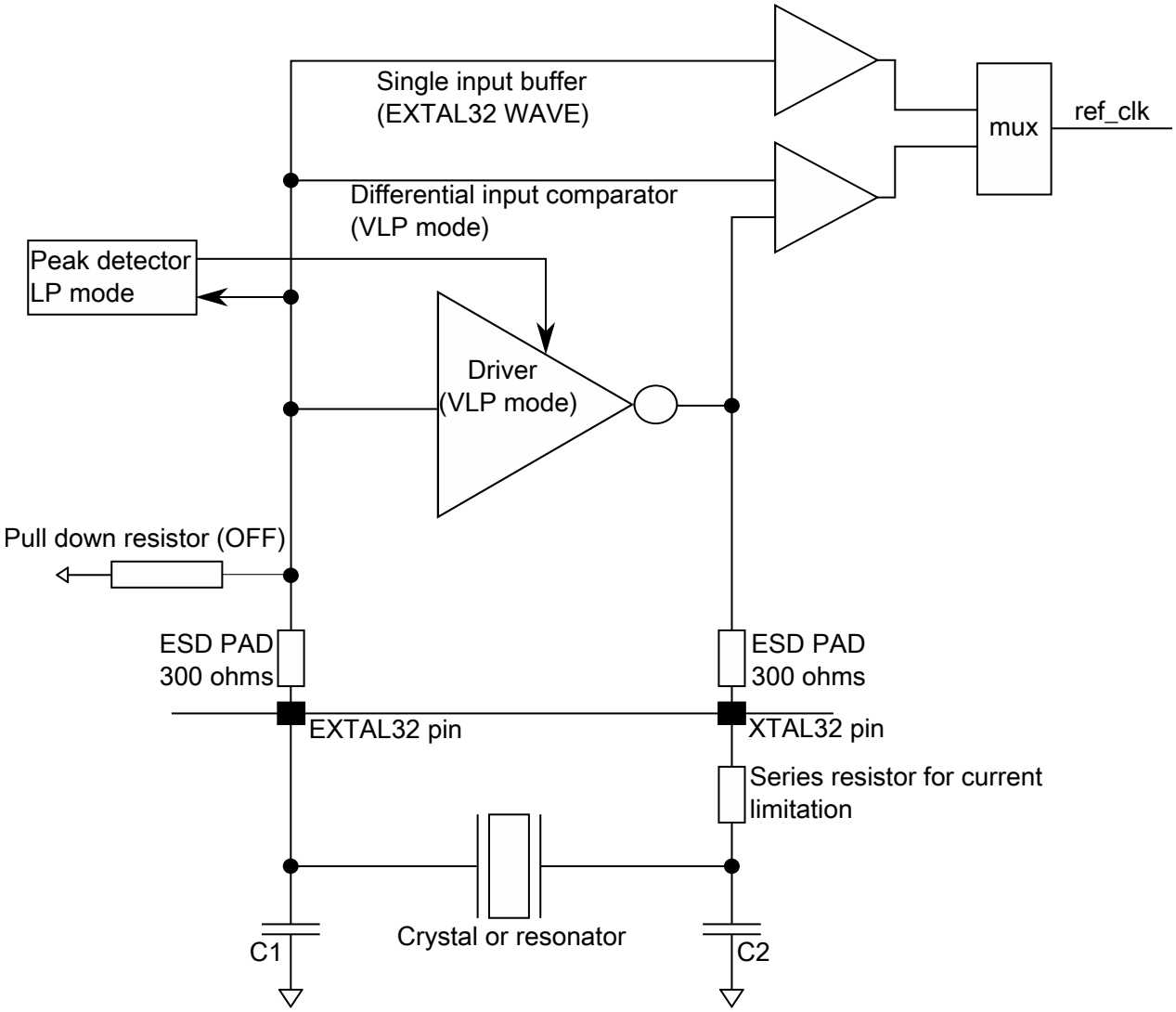
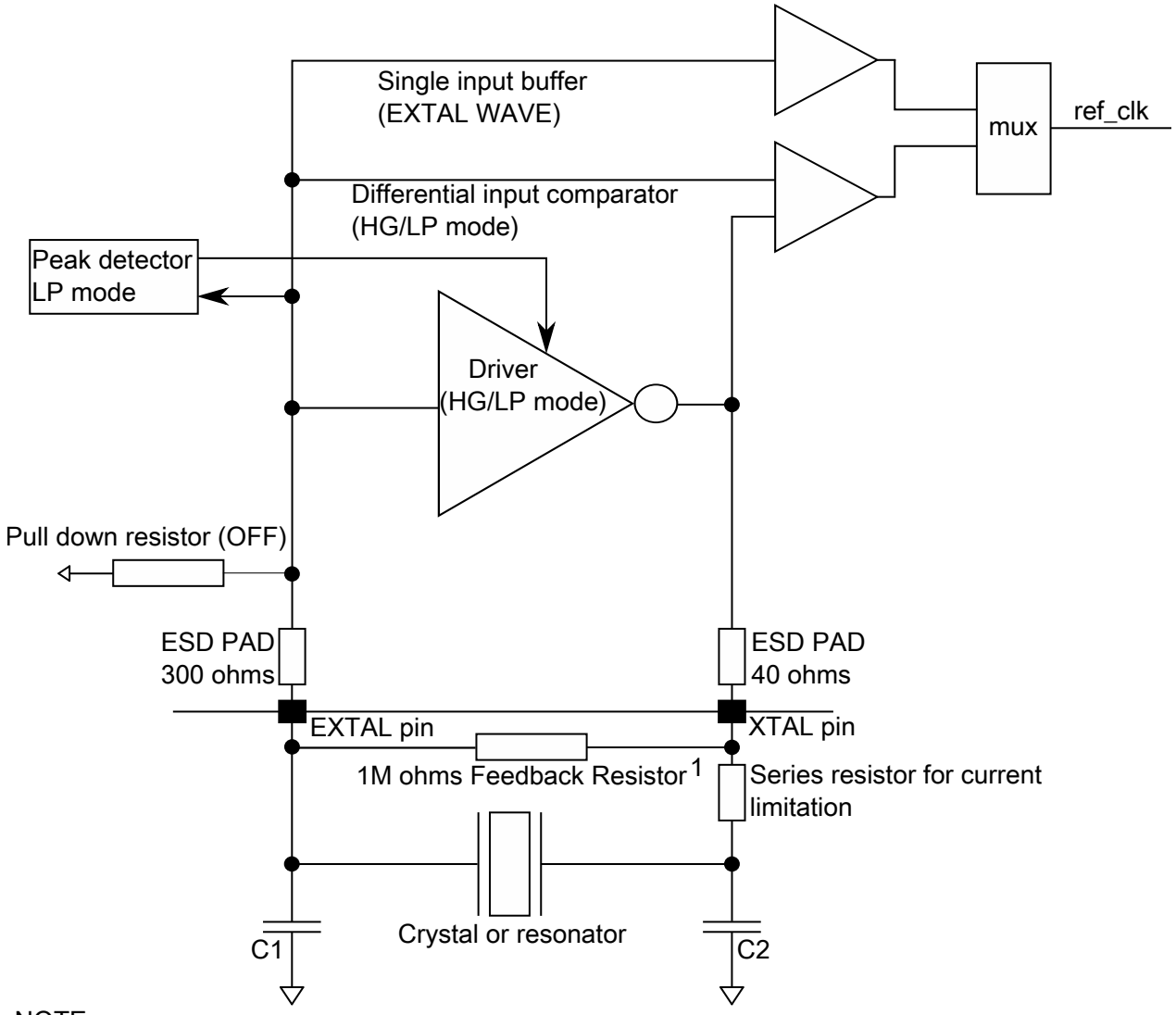


Figure 17. Oscillator connections scheme (OSC32)



NOTE:

1. 1M Feedback resistor is needed only for HG mode.

Figure 18. Oscillator connections scheme (OSC)

NOTE

Data values in the following "External Oscillator electrical specifications" tables are from simulation.

Table 42. External Oscillator electrical specifications (OSC32)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
$I_{DDOSC32}$	Supply current	—	500	—	nA	1
$g_{mXOSC32}$	Oscillator transconductance	6	—	9	µA/V	
V_{IH}	Input high voltage — EXTAL32 pin in external clock mode	0.7 × V_{DD}	—	V_{DD}+0.3	V	

Table continues on the next page...

Table 42. External Oscillator electrical specifications (OSC32) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@V_{DD}=3.3 V					
	@V_{DD}=5.0 V	0.65 × V_{DD}	—	V_{DD}+0.3	V	
V_{IL}	Input low voltage — EXTAL32 pin in external clock mode @V_{DD}=3.3 V	V_{SS} –0.3	—	0.3 × V_{DD}	V	
	@V_{DD}=5.0 V	V_{SS} –0.3	—	0.35 × V_{DD}	V	
C_1	EXTAL32 load capacitance	—	—	—		2
C_2	XTAL32 load capacitance	—	—	—		2
R_F	Feedback resistor	—	—	—	MΩ	
R_S	Series resistor	—	—	—	kΩ	
V_{pp_OSC32}	Peak-to-peak amplitude of oscillation (oscillator mode)	—	0.6	—	V	3

1. Measured at V_{DD} = 5 V, Temperature = 25 °C. The current consumption is according to the crystal or resonator, loading capacitance.
2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values. And also consider the parasitic capacitance of package and board.
3. The EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

Table 43. External Oscillator electrical specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
I_{DDOSC}	Supply current — low-gain mode (low-power mode) (HGO=0)					1
	4 MHz	—	200	—	µA	
	8 MHz	—	300	—	µA	
	16 MHz	—	1.2	—	mA	
	24 MHz	—	1.6	—	mA	
	32 MHz	—	2	—	mA	
	40 MHz	—	2.6	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	32 kHz	—	25	—	µA	
	4 MHz	—	1	—	mA	
	8 MHz	—	1.2	—	mA	
	16 MHz	—	3.5	—	mA	
	24 MHz	—	5	—	mA	
	32 MHz	—	5.5	—	mA	
	40 MHz	—	6	—	mA	
g_{mXOSC}	Fast external crystal oscillator transconductance					

Table continues on the next page...

Table 43. External Oscillator electrical specifications (OSC) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	32 kHz, Low Frequency Range, High Gain (32 kHz)	15	—	45	µA / V	
	Medium Frequency Range (4-8 MHz)	2.2	—	9.7	mA / V	
	High Frequency Range (8-40 MHz)	16		37	mA / V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	1.75	—	V_{DD}	V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	1.20	V	
C_1	EXTAL load capacitance	—	—	—		2
C_2	XTAL load capacitance	—	—	—		2
R_F	Feedback resistor					3
	Low-frequency, high-gain mode (32 kHz)	—	10	—	MΩ	
	Medium/high-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz)	—	—	—	MΩ	
	Medium/high-frequency, high-gain mode (4-8 MHz, 8-40 MHz)	—	1	—	MΩ	
R_S	Series resistor					
	Low-frequency, high-gain mode (32 kHz)	—	200	—	kΩ	
	Medium/high-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz)	—	0	—	kΩ	
	Medium/high-frequency, high-gain mode (4-8 MHz, 8-40 MHz)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					4
	Low-frequency, high-gain mode	—	3.3	—	V	
	Medium/high-frequency, low-gain mode	—	1.0	—	V	
	Medium/high-frequency, high-gain mode	—	3.3	—	V	

1. Measured at V_{DD} = 5 V, Temperature = 25 °C. The current consumption is according to the crystal or resonator, loading capacitance.
2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values. And also consider the parasitic capacitance of package and board.
3. When low power mode is selected, R_F is integrated and must not be attached externally.
4. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

5.4.2.1.2 External Oscillator frequency specifications

Table 44. External Oscillator frequency specifications (OSC32)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc32_lo}	Oscillator crystal or resonator frequency — low-frequency mode	30	—	40	kHz	
$t_{dc\_extal32}$	Input clock duty cycle (external clock mode)	40	50	60	%	

Table continues on the next page...

Table 44. External Oscillator frequency specifications (OSC32) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{ec\_extal32}$	Input clock frequency (external clock mode)	—	—	40	kHz	
t_{cst32}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	2000	—	ms	1

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

Table 45. External Oscillator frequency specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — Low Frequency, High Gain Mode	32	—	40	kHz	
f_{osc_me}	Oscillator crystal or resonator frequency — Medium Frequency	4	—	8	MHz	
f_{osc_hi}	Oscillator crystal or resonator frequency — High Frequency	8	—	40		
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	
t_{cst}	Crystal startup time — 32 kHz Low Frequency, High-Gain Mode	—	500	—	ms	1
	Crystal startup time — 8 MHz Medium Frequency, Low-Power Mode	—	1.5	—		
	Crystal startup time — 8 MHz Medium Frequency, High-Gain Mode	—	2.5	—		
	Crystal startup time — 40 MHz High Frequency, Low-Power Mode	—	2	—		
	Crystal startup time — 40 MHz High Frequency, High-Gain Mode	—	2.5	—		

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

5.4.2.2 System Clock Generation (SCG) specifications

5.4.2.2.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 46. Fast internal RC Oscillator electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	Fast internal reference frequency	—	48	—	MHz
I_{VDD}	Supply current	—	400	500	µA

Table continues on the next page...

Table 46. Fast internal RC Oscillator electrical specifications (continued)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$F_{Untrimmed}$	IRC frequency (untrimmed)	F_{IRC}× (1-0.3)	—	F_{IRC}× (1+0.3)	MHz
ΔF_{OL}	Open loop total deviation of IRC frequency over voltage and temperature[1]				
	Regulator enable	—	±0.5	±1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		—	3	µs[2]
T_{JIT}	Period jitter (RMS)	—	35	150	ps

1. The limit is respected across process, voltage and full temperature range.
2. Startup time is defined as the time between clock enablement and clock availability for system use.

5.4.2.2.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 47. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	Slow internal reference frequency	—	2 8	—	MHz
I_{VDD}	Supply current	—	23	—	µA
$F_{Untrimmed}$	IRC frequency (untrimmed)	—	—	—	MHz
ΔF_{OL}	Open loop total deviation of IRC frequency over voltage and temperature[1]				
	Regulator enable	—	—	±3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	6	—	µs[2]

1. The limit is respected across process, voltage and full temperature range.
2. Startup time is defined as the time between clock enablement and clock availability for system use.

5.4.2.2.3 Low Power Oscillator (LPO) electrical specifications

Table 48. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPO}	Internal low power oscillator frequency	113	128	139	kHz
I_{LPO}	Current consumption	1	3	7	µA
$T_{startup}$	Startup Time	—	—	20	µs

5.4.2.2.4 LPFLL electrical specifications

Table 49. LPFLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{avg}	Power consumption		240		µA
T_{start}	Start-up time		3.6		µs
ΔF_{ol}	Frequency accuracy over temperature and voltage in open loop after process trimmed	–10	—	10	%
ΔF_{cl}	Frequency accuracy in closed loop	–1 [1]	—	1 [1]	%

1. ΔF_{cl} is dependent on reference clock accuracy. For example, if locked to crystal oscillator, ΔF_{cl} is typically limited by trimming ability of the module itself; if locked to other clock source which has 3% accuracy, then ΔF_{cl} can only be ±3%.

5.4.3 Memories and memory interfaces

5.4.3.1 Flash memory module (FTFE) electrical specifications

This section describes the electrical characteristics of the flash memory module (FTFE).

5.4.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 50. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Flash Block high-voltage time for 32 KB	—	26	226	ms	1
$t_{hversblk256k}$	Erase Flash Block high-voltage time for 256 KB	—	208	1808	ms	1

1. Maximum time based on expectations at cycling end-of-life.

5.4.3.1.2 Flash timing specifications — commands

Table 51. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.3	ms	
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.8	ms	

Table continues on the next page...

Table 51. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash)	—	—	75	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	28	240	ms	
$t_{ersblk256k}$	• 256 KB program flash	—	220	1850	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec512}$	Program Section execution time (512B flash)	—	2.5	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	2.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	250	2100	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	250	2100	ms	2
	Program Partition for EEPROM execution time					
$t_{pgmpart24k}$	• 24 KB EEPROM backup	—	69	—	ms	
$t_{pgmpart32k}$	• 32 KB EEPROM backup	—	70	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram24k}$	• 24 KB EEPROM backup	—	0.6	1.1	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
	Byte-write to FlexRAM execution time:					
$t_{eewr8b24k}$	• 24 KB EEPROM backup	—	370	1625	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
	16-bit write to FlexRAM execution time:					
$t_{eewr16b24k}$	• 24 KB EEPROM backup	—	370	1625	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	1500	µs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b24k}$	• 24 KB EEPROM backup	—	600	1950	µs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2000	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.4.3.1.3 Flash high voltage current behaviors

Table 52. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.4.3.1.4 Reliability specifications

Table 53. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
	Data Flash					
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
	FlexRAM as EEPROM					
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
$n_{nvmcycee}$	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	140 K	400 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	1.26 M	3.2 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	5 M	12.8 M	—	writes	
$n_{nvmwree1k}$	• EEPROM backup to FlexRAM ratio = 1,024	10 M	25 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.
3. Write endurance represents the number of writes to each FlexRAM location at -40 °C ≤Tj ≤ 125 °C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

5.4.4 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.4.5 Analog

5.4.5.1 ADC electrical specifications

5.4.5.1.1 12-bit ADC operating conditions

Table 54. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	5.5	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		2.5	V_{DDA}	V_{DDA} + 100m	V	3
V_{REFL}	ADC reference voltage low		– 100	0	100	mV	3
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
R_S	Source impedendance	f_{ADCK} < 4 MHz	—	—	5	kΩ	
R_{SW1}	Channel Selection Switch Impedance		—	0.5	1.2	kΩ	
R_{AD}	Sampling Switch Impedance		—	2	5	kΩ	
C_{P1}	Pin Capacitance		—	3	—	pF	
C_{P2}	Analog Bus Capacitance		—	—	5	pF	
C_S	Sampling capacitance		—	4	5	pF	
f_{ADCK}	ADC conversion clock frequency		2	40	50	MHz	4, 5
C_{rate}	ADC conversion rate	No ADC hardware averaging[6] Continuous conversions enabled, subsequent conversion time	20	—	1200	Ksps	7

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
4. Clock and compare cycle need to be set according the guidelines in the block guide.

5. ADC conversion will become less reliable above maximum frequency.
6. When using ADC hardware averaging, refer to the device *Reference Manual* to determine the most appropriate setting for AVGS.
7. Max ADC conversion rate of 1200 Ksps is with 10-bit mode

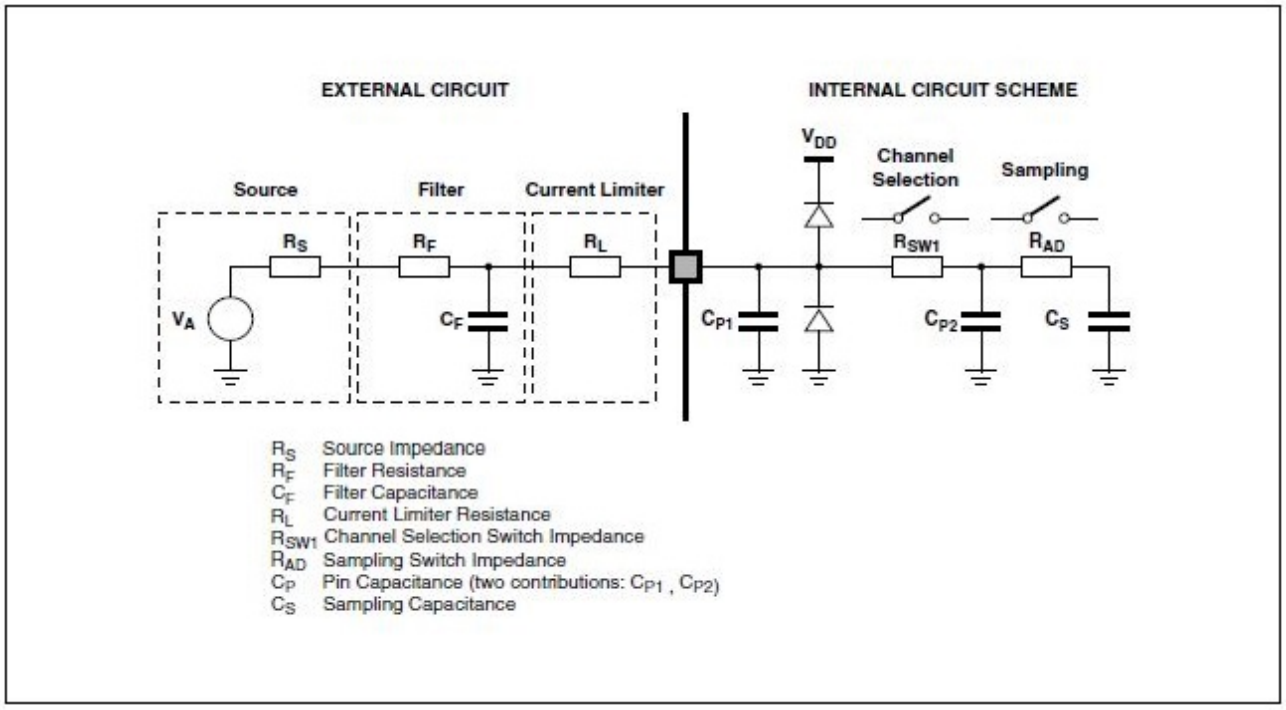


Figure 19. ADC input impedance equivalency diagram

5.4.5.1.2 12-bit ADC electrical characteristics

NOTE

All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

For ADC signals adjacent to VDD/VSS or the XTAL pins some degradation in the ADC performance may be observed.

NOTE

All values guarantee the performance of the ADC for the multiple ADC input channel pins. When using the ADC to monitor the internal analogue parameters, please assume minor degradation.

Table 55. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.[3]	Unit	Notes
I_{DDA_ADC}	Supply current at 2.7 to 5.5 V		927	975 µA @ 5 V	1023	µA	4
	Sample Time		275	—	Refer to the device's *Reference Manual*	ns	
TUE	Total unadjusted error at 2.7 to 5.5 V		—	±4.5	±6.11	LSB[5]	6
DNL	Differential non-linearity at 2.7 to 5.5 V		—	±0.8	±1.07	LSB[5]	6
INL	Integral non-linearity at 2.7 to 5.5 V		—	±1.4	±3.54	LSB[5]	6
E_{FS}	Full-scale error at 2.7 to 5.5 V		—	–2	-3.60	LSB[5]	$V_{ADIN} = V_{DDA}$[6]
E_{ZS}	Zero-scale error at 2.7 to 5.5 V		—	–2.7	-4.24	LSB[5]	
E_Q	Quantization error at 2.7 to 5.5 V		—	—	±0.5	LSB[5]	
ENOB	Effective number of bits at 2.7 to 5.5 V		—	11.3	—	bits	7
SINAD	Signal-to-noise plus distortion at 2.7 to 5.5 V	See ENOB	—	70	—	dB	SINAD = 6.02 × ENOB + 1.76
E_{IL}	Input leakage error at 2.7 to 5.5 V		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
V_{TEMP_S}	Temp sensor slope at 2.7 to 5.5 V	Across the full temperature range of the device	1.492	1.564	1.636	mV/°C	8, 9
V_{TEMP25}	Temp sensor voltage at 2.7 to 5.5 V	25 °C	730	740.5	751	mV	8, 9

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 48 MHz unless otherwise stated.
3. These values are based on characterization but not covered by test limits in production.
4. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
5. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
6. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
7. Input data is 100 Hz sine wave. ADC conversion clock < 40 MHz.
8. ADC conversion clock < 3 MHz
9. The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

5.4.5.2 CMP with 8-bit DAC electrical specifications

Table 56. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ. [1]	Max.	Unit
V_{DD}	Supply voltage	2.7	—	5.5	V
I_{DDHS}	Supply current, High-speed mode[2]				μA
	within ambient temperature range	—	145	200	
I_{DDLS}	Supply current, Low-speed mode[2]				μA
	within ambient temperature range	—	5	10	
V_{AIN}	Analog input voltage	0	0 - V_{DDX}	V_{DDX}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	within ambient temperature range	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	within ambient temperature range	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[3]				ns
	within ambient temperature range	—	30	200	
t_{DLSB}	Propagation delay, Low-speed mode[3]				μs
	within ambient temperature range	—	0.5	2	
t_{DHSS}	Propagation delay, High-speed mode[4]				ns
	within ambient temperature range	—	70	400	
t_{DLSS}	Propagation delay, Low-speed mode[4]				μs
	within ambient temperature range	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode [3]				μs
	within ambient temperature range	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[3]				μs
	within ambient temperature range	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0 (V_{AIO})				mV
	within ambient temperature range	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	within ambient temperature range	—	16	53	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	within ambient temperature range	—	11	30	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	within ambient temperature range	—	32	90	
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	within ambient temperature range	—	22	53	

Table continues on the next page...

Table 56. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ. [1]	Max.	Unit
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	within ambient temperature range	—	48	133	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	within ambient temperature range	—	33	80	
I_{DAC8b}	8-bit DAC current adder (enabled)	—	10	16	μA
INL	8-bit DAC integral non-linearity	–0.6	—	0.5	LSB[5]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB

1. Typical values assumed at VDDA = 5.0 V, Temp = 25 °C, unless otherwise stated.
2. Difference at input > 200mV
3. Applied ± (100 mV + Hyst) around switch point
4. Applied ± (30 mV + 2 × Hyst) around switch point
5. 1 LSB = $V_{reference}/256$

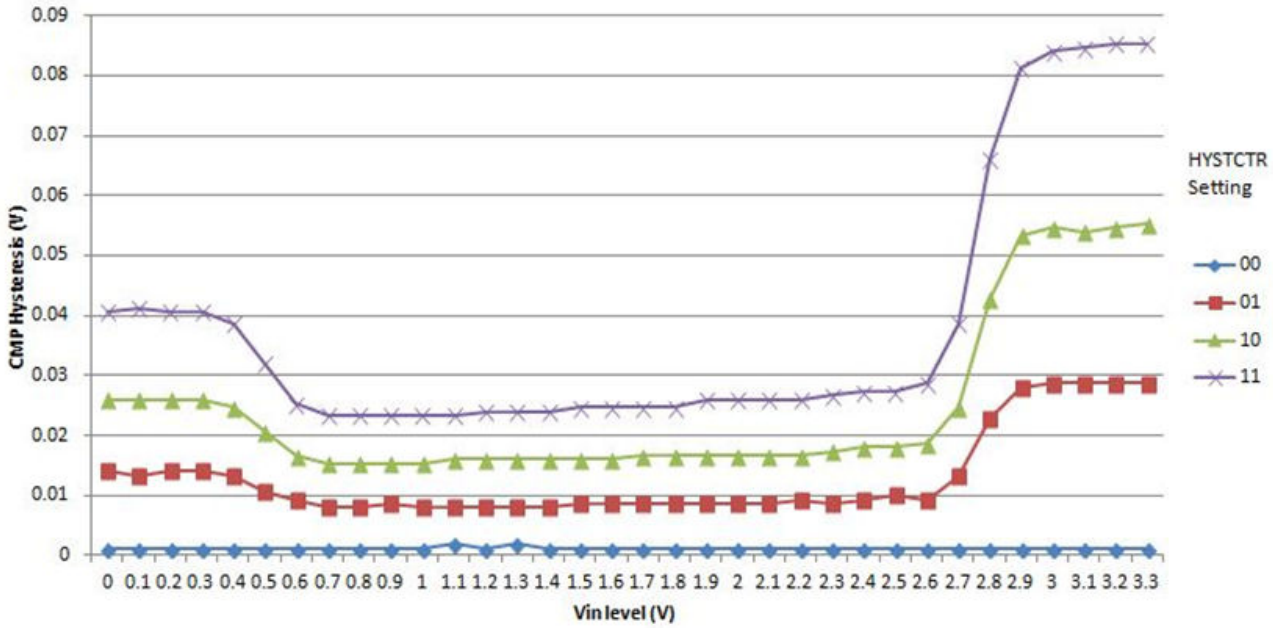


Figure 20. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

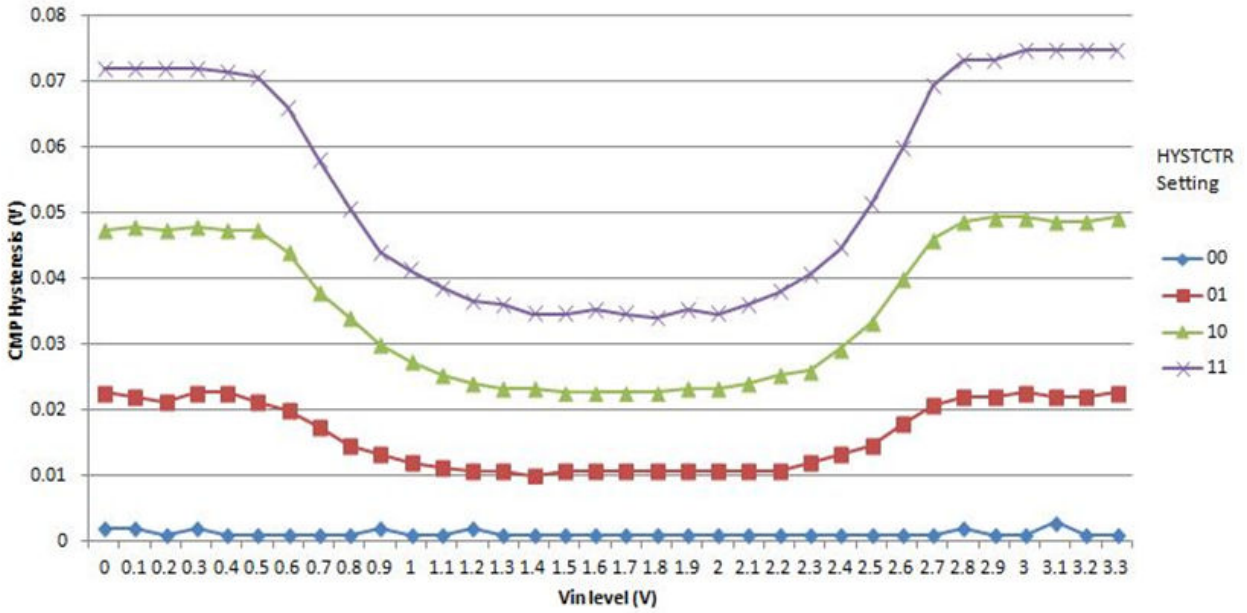


Figure 21. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

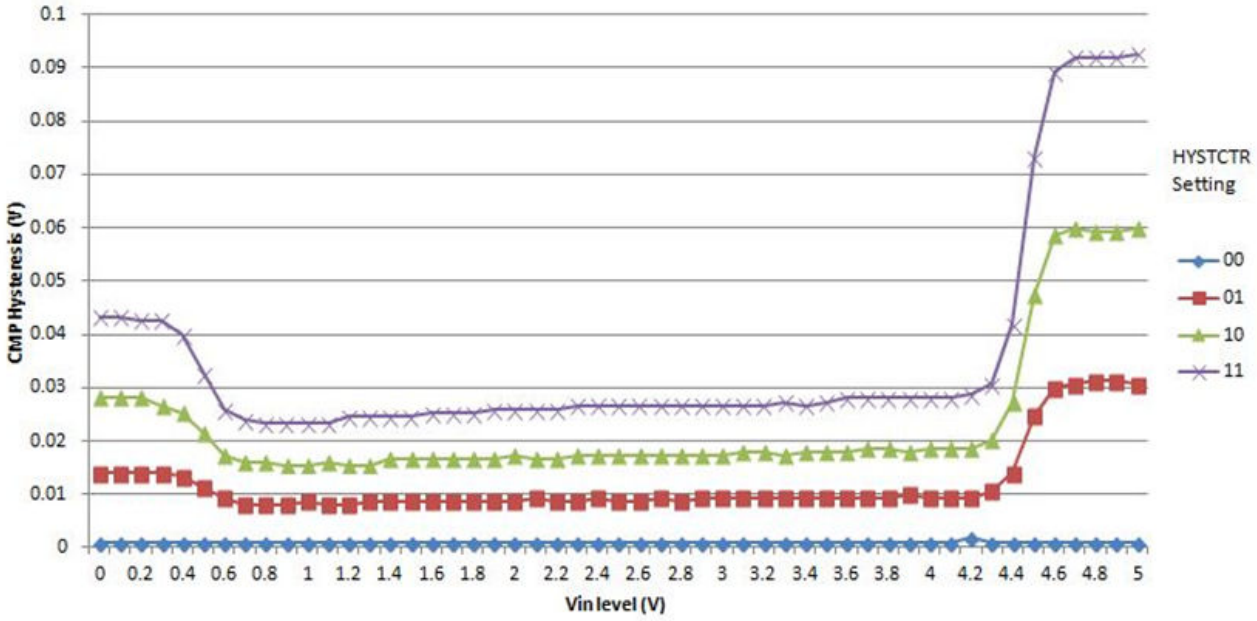


Figure 22. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 0)

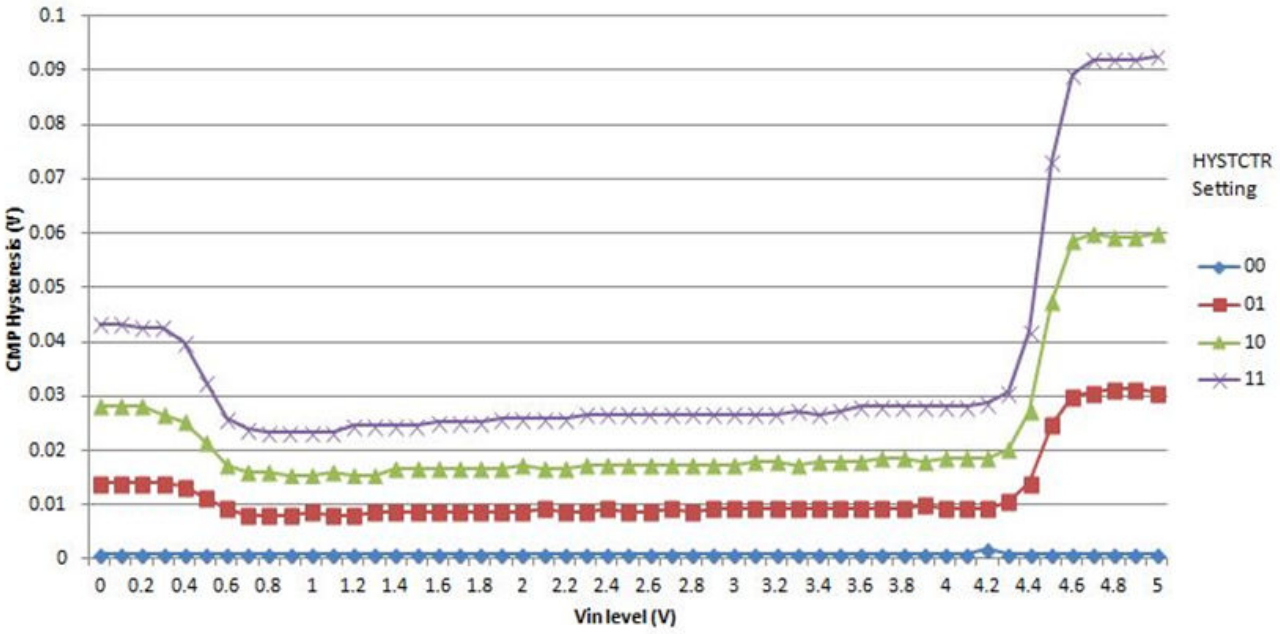


Figure 23. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 1)

5.4.6 Communication interfaces

5.4.6.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

5.4.6.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 57. LPSPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{SPSCK}	Frequency of SPSCK	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—

Table continues on the next page...

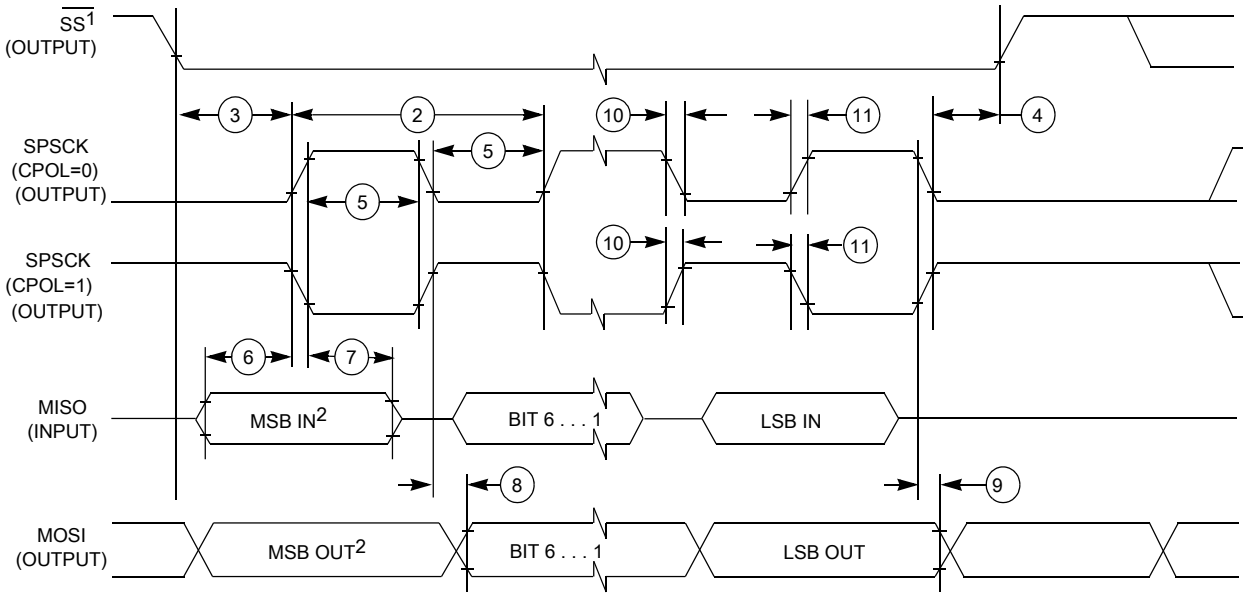
Table 57. LPSPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is LPSPI peripheral functional clock. On this device, the max value of f_{SPSCK} should not exceed 25 MHz.
2. $t_{periph} = 1/f_{periph}$

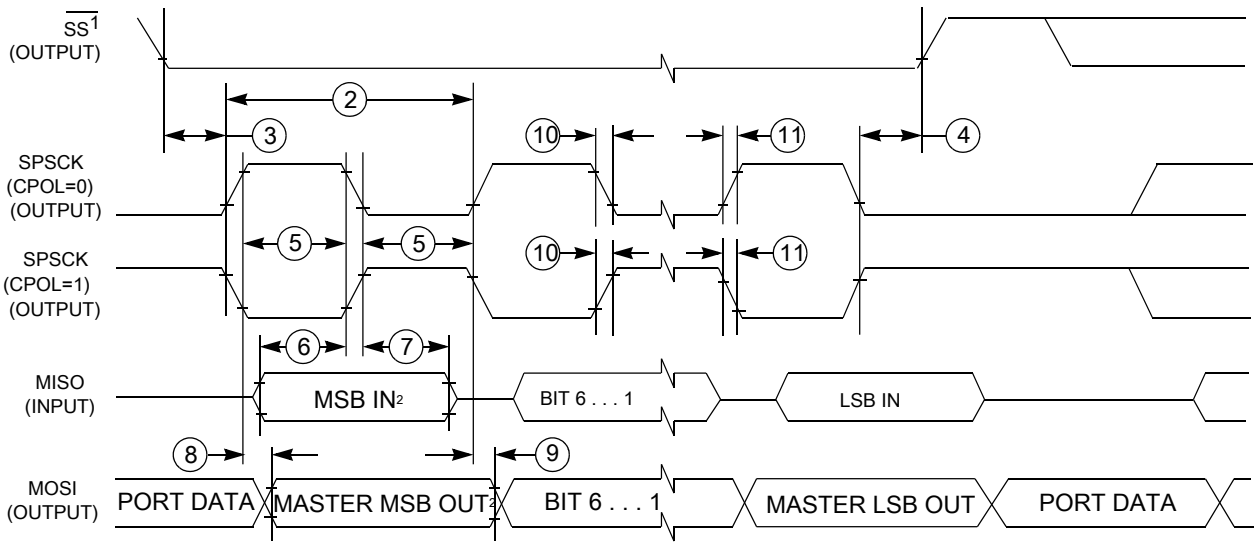
NOTE

High drive pin should be used for fast bit rate.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 24. LPSPI master mode timing (CPHA = 0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 25. LPSPI master mode timing (CPHA = 1)

Table 58. LPSPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{SPSCK}	Frequency of SPSCK	0	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is LPSPI peripheral functional clock. On this device, the max value of f_{SPSCK} should not exceed 25 MHz.
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

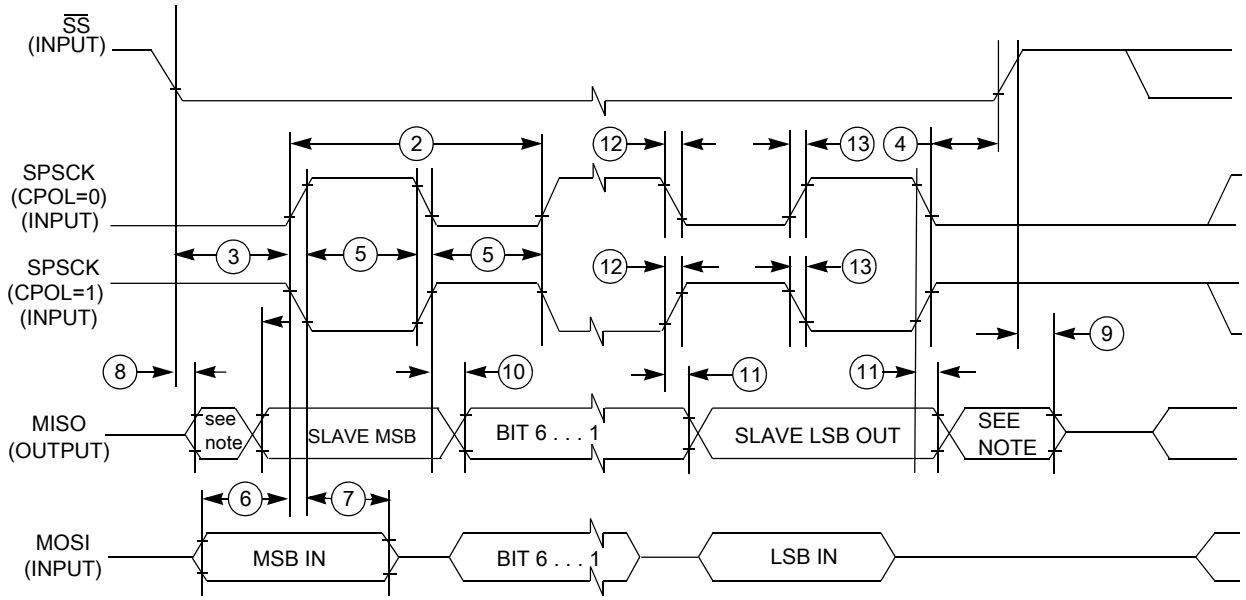


Figure 26. LPSPI slave mode timing (CPHA = 0)

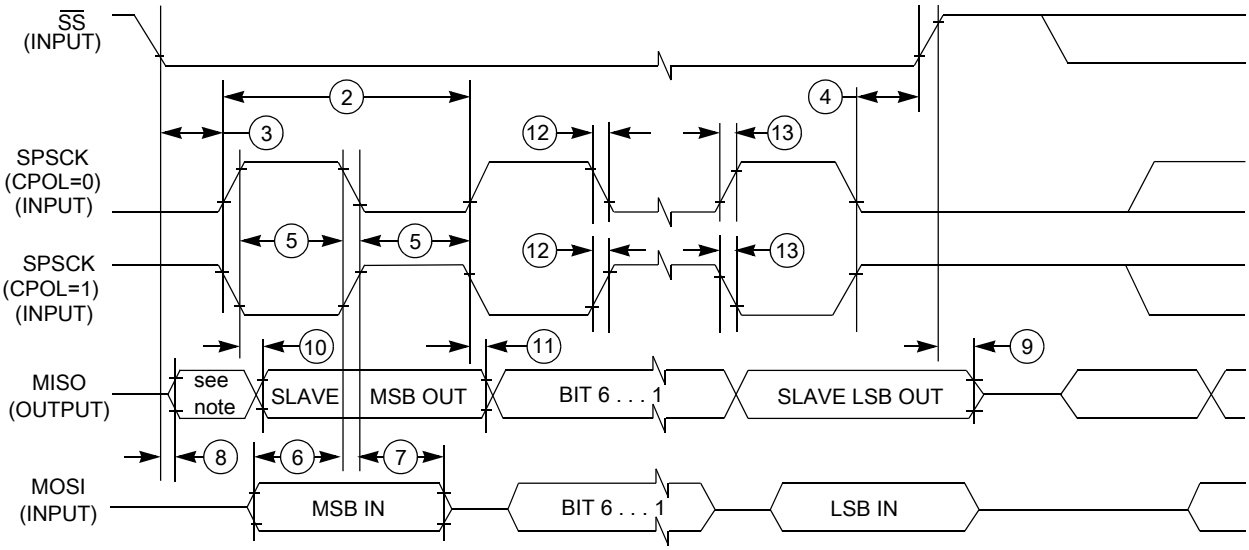


Figure 27. LPSPI slave mode timing (CPHA = 1)

5.4.6.3 LPI^{2}C

Table 59. LPI^{2}C specifications

Symbol	Description		Min.	Max.	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	1, 2, 3
		Fast mode (Fm)	0	400		
		Fast mode Plus (Fm+)	0	1000		
		Ultra Fast mode (UFm)	0	5000		
		High speed mode (Hs-mode)	0	3400		

1. Hs-mode is only supported in slave mode.
2. The maximum SCL clock frequency in Fast mode with maximum bus loading (400pF) can only be achieved with appropriate pull-up devices on the bus when using the high or normal drive pins across the full voltage range . The maximum SCL clock frequency in Fast mode Plus can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. The maximum SCL clock frequency in Ultra Fast mode can support maximum bus loading (400pF) when using the high drive pins. The maximum SCL clock frequency for slave in High speed mode can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. For more information on the required pull-up devices, see I^2C Bus Specification.
3. See the section "General switching specifications".

5.4.7 Human-machine interfaces (HMI)

5.4.7.1 Touch sensing input (TSI) electrical specifications

Table 60. TSI electrical specifications

Symbol	Description	Value			Unit
		Min	Typ	Max	
I_{DD_EN}	Power consumption in operation mode	—	500	—	µA
I_{DD_DIS}	Power consumption in disable mode	—	20	—	nA
V_{BG}	Internal bandgap reference voltage	—	1.21	—	V
V_{PRE}	Internal bias voltage	—	1.51	—	V
C_I	Internal integration capacitance	—	90	—	pF
F_{CLK}	Internal main clock frequency	—	16	—	MHz

5.4.8 Debug modules

5.4.8.1 SWD electricals

Table 61. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
V_{DDA}	Operating voltage	2.7	5.5	V
S1	SWD_CLK frequency of operation	0	25	MHz

Table continues on the next page...

Table 61. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

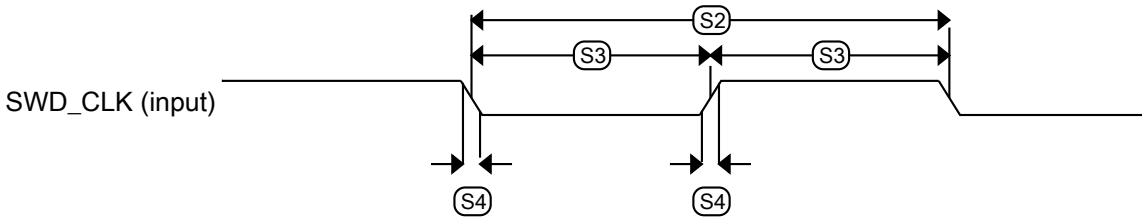


Figure 28. Serial wire clock input timing

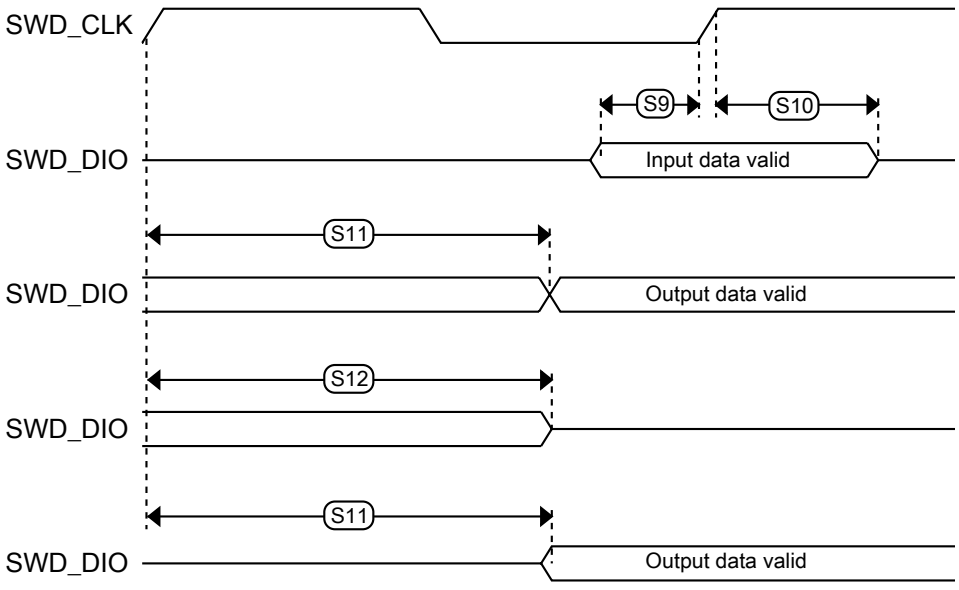


Figure 29. Serial wire data timing

6 Design considerations

6.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

6.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground. Consider to add ferrite bead or inductor to some sensitive lines.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

6.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Always route the power net as star topology, and make each power trace loop as minimum as possible.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 μF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 μF capacitors positioned as near as possible to the package supply pins.

6.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

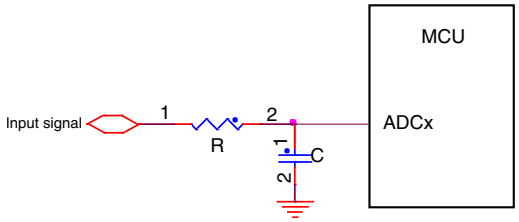


Figure 30. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. External clamp diodes can be added here to protect against transient over-voltages.

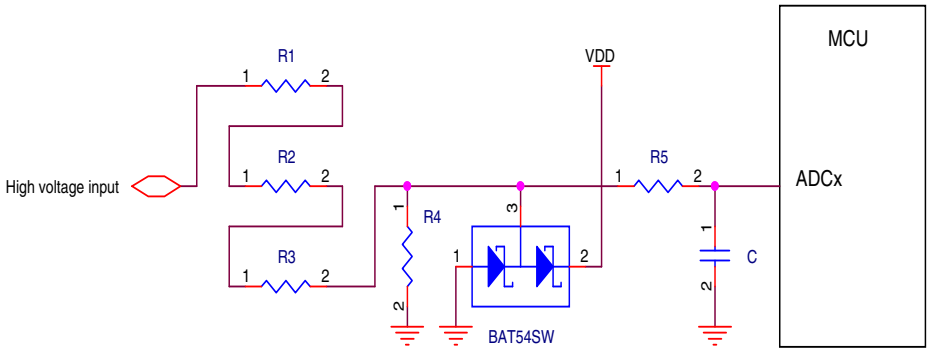


Figure 31. High voltage measurement with an ADC input

NOTE

For more details of ADC related usage, refer to AN5250: How to Increase the Analog-to-Digital Converter Accuracy in an Application.

6.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDD (Max I/O is VDD+0.3V).

CAUTION

Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

- RESET_b pin

The RESET_b pin is a pseudo open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

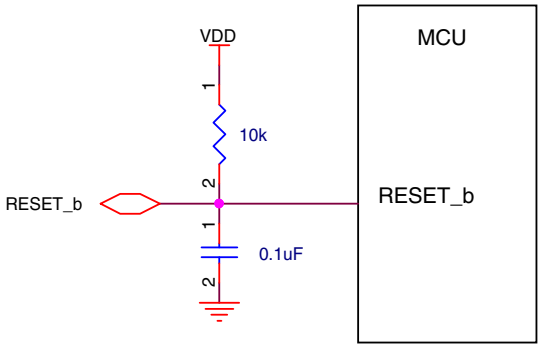


Figure 32. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

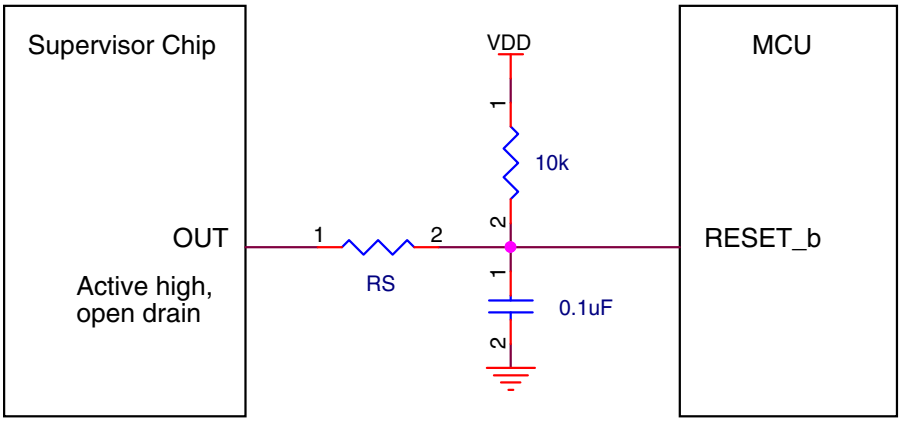


Figure 33. Reset signal connection to external reset chip

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

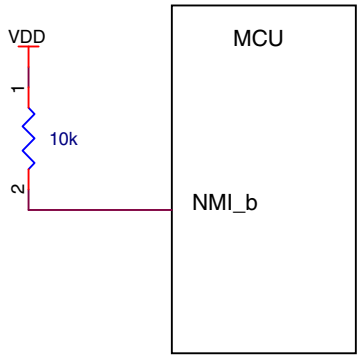


Figure 34. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

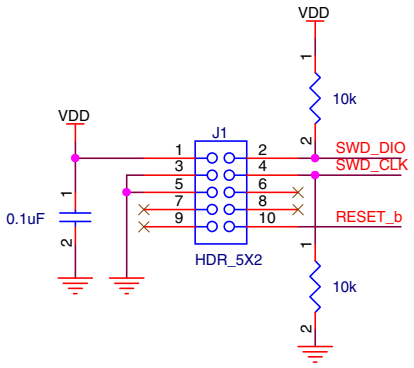


Figure 35. SWD debug interface

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

The series resistor, RS, is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2 MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2 MHz does not require any series resistance.

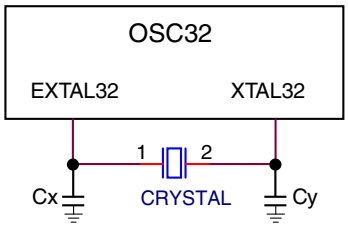


Figure 36. RTC Oscillator (OSC32) module connection – Diagram 1

Table 62. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768 kHz), high gain	Diagram 3
High frequency (1-32 MHz), low power	Diagram 2
High frequency (1-32 MHz), high gain	Diagram 3

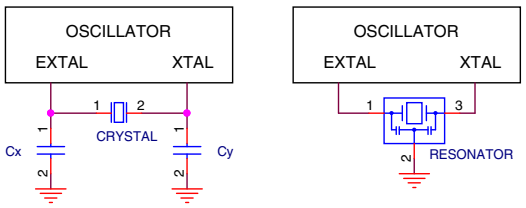


Figure 37. Crystal connection – Diagram 2

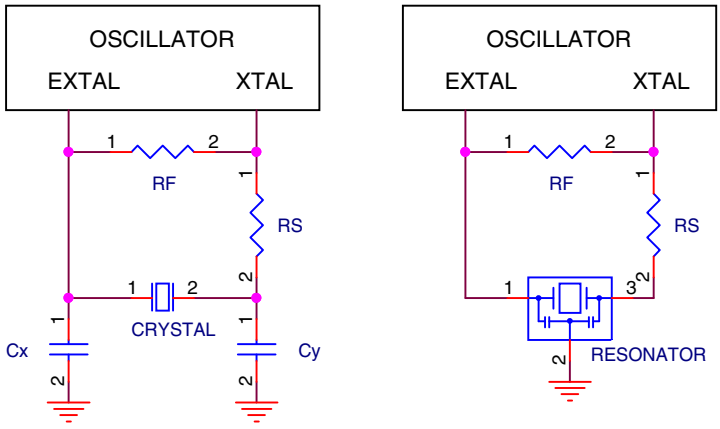


Figure 38. Crystal connection – Diagram 3

NOTE

For PCB layout, the user could consider to add the guard ring to the crystal oscillator circuit.

6.2 Software considerations

All Kinetis MCUs are supported by comprehensive NXP and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.nxp.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- Freedom Development Platform: http://www.nxp.com/freedom

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.nxp.com/kds
- Partner IDEs: http://www.nxp.com/kide

Run-time Software

- Kinetis SDK: http://www.nxp.com/ksdk
- Kinetis Bootloader: http://www.nxp.com/kboot
- ARM mbed Development Platform: http://www.nxp.com/mbed

For all other partner-developed software and tools, visit http://www.nxp.com/partners.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 63. Part number fields description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KE##	Kinetis family	• KE15, KE14
A	Key attribute	• Z = Cortex-M0+

Table continues on the next page...

Table 63. Part number fields description (continued)

Field	Description	Values
FFF	Program flash memory size	• 128 = 128 KB • 256 = 256 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 7 = 72 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKE15Z256VLL7

8 Revision history

The following table provides a revision history for this document.

Table 64. Revision history

Rev. No.	Date	Substantial Changes
2 (public release)	09/2016	Initial public release.
2.1 (internal version)	10/2016	• Updated the max value of "Frequency of operation", in the "LPSPI slave mode timing" table. • Minor correction: V_{DDE} symbol should be V_{DD}, in the "DC electrical specifications" table. • Minor update in the "Clocking block diagram" figure. • Minor update in the "Analog design" section.
2.2 (internal version)	06/2017	• Updated the "Voltage and current operating ratings" section. • Minor update in the "Pinout decoupling" figure. • Fixed the "Description" collumn of STOP and VLPS mode rows, in the "Power consumption operating behaviors" table.
2.3 (internal version)	08/2017	• Minor update in the "Clock interfaces" section of the feature list, on the front matter cover pages.

Table continues on the next page...

Table 64. Revision history (continued)

Rev. No.	Date	Substantial Changes
		• Some updates in the "External Oscillator electrical specifications (OSC32)" and "External Oscillator electrical specifications (OSC)" tables. • Some updates in the "External Oscillator frequency specifications (OSC32)" and "External Oscillator frequency specifications (OSC)" tables.
3 (public release)	07/2018	• Updated the figure "Memory map". • Minor updates in the figures "Oscillator connections scheme (OSC32)" and "Oscillator connections scheme (OSC)". • Some updates of V_{IH} and V_{IL} in the "External Oscillator electrical specifications (OSC32)" and "External Oscillator electrical specifications (OSC)" tables, and minor editorial fix. • Updated the table "Fast internal RC Oscillator electrical specifications": FIRC is trimmed to 48 MHz only, in this device. • Updated the figure "ADC input impedance equivalency diagram". • Corrected the unit as uA, in the I_{DDA_ADC} row of the table "12-bit ADC characteristics". • Footnote updated in the tables "LPSPI master mode timing" and "LPSPI slave mode timing". • Corrected the minimum and the maximum values of V_{LVRX} in the "V_{DD} supply LVR, LVD and POR operating requirements" table. • Updated the "Voltage and current operating requirements" table.
4 (public release)	06/2019	• Corrected the "Clock interfaces" section in the cover page: FIRC is trimmed to 48 MHz only in this device. Up to 50 MHz DC external square wave input clock. • Minor fix in Figure 4. • Note added after Table 5. • Statement restored in the section RTC : The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator, or clock directly from RTC_CLKIN pin. • Minor fix in Table 23. • Some major updates in Table 54. • Some minor updates in tables "LPSPI master mode timing" and "LPSPI slave mode timing", including the footnotes, in the section LPSPI electrical specifications.
4.1 (internal version)	07/2020	• Minor correction in the FTM channel numbers of the "Module Signal Description Tables" section. • Minor correction in the "Functional block diagram" figure after the cover page: GPIO and TSI blocks. • Minor correction in the "Ordering information" table: ADC channels collumn.
4.2 (public release)	03/2021	• Added errata for Mask 2N36S, in the "Related Resources" table of cover page.
4.3 (public release)	07/2021	• Updated the I_{DD} data in rows with test condition "all peripheral clock enabled", in the "Power consumption operating behaviors" table. • Updated the figures "Run mode supply current vs. core frequency" and "VLPR mode supply current vs. core frequency". • Minor update in the "TSI electrical specifications" table. • Title changed from "KE1xZ" to "KE15Z/14Z" in the cover page.

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Document Number KE1xZP100M72SF0
Revision 4.3, 07/2021

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Revision 4.3, 07/2021