

i.MX RT500 低功耗跨界处理器数据手册 (带附录)

i.MX RT500 低功耗交叉处理器数据手册 0.1 版 (带附录) 包含两个部分：

- 数据手册第 0 版，即本封面之后的正文内容。附录中所述的更改尚未在指定的页面中完成。
- 数据手册第 0 版的附录。

i.MX RT500 低功耗 跨界处理器

i.MX RT500 是一个双核微控制器系列，适用于嵌入式应用，配备 ARM Cortex-M33 CPU 和 Cadence® Xtensa® Fusion F1 音频数字信号处理器 CPU。Cortex-M33 包括两个硬件协处理器，为一系列复杂算法提供增强的性能，还有一个带 LCD 接口和 MIPI DSI PHY 的 2D 矢量 GPU。该系列提供丰富的外设和极低的功耗。该器件包含高达 5MB 的 SRAM、两个 FlexSPI (八线/四线 SPI 接口，每个 FlexSPI 接口具有 32 KB 缓存，其中一个 FlexSPI 接口具有动态解密功能)、高速 USB 主/从设备+ PHY、12 位 1MS/s ADC、模拟比较器、支持 8 个 DMIC 通道的音频子系统、带有 MIPI DSI PHY 的 2D GPU 和 LCD 控制器、SDIO/eMMC、FlexIO、AES/SHA/Crypto M33 协处理器和 PUF 密钥生成功能。

MIMXRT5XXSFFOC
MIMXRT5XXSFFOCR
MIMXRT5XXSFAWCR



249 FOWLP 7.0mm x 7.0mm x 0.725mm, 0.4mm 间距
141 WLCSP 4.525mm x 4.525mm x 0.49mm, 0.35mm 间距

控制处理器内核

- Arm Cortex-M33 处理器，运行频率高达 200 MHz
- Arm TrustZone
- Arm Cortex-M33 内置存储器保护单元 (MPU)，支持 8 个区域
- 单精度硬件浮点单元 (FPU)
- Arm Cortex-M33 内置嵌套矢量中断控制器 (NVIC)
- 不可屏蔽中断 (NMI) 输入
- Cortex-M33 的两个协处理器：针对固定和浮点 DSP 功能的硬件加速器 (PowerQuad) 和加密/FFT 引擎 (Casper)。DSP 协处理器使用一组四个专用的 2KB SRAM。加密/FFT 引擎使用一组两个 2KB SRAM，CPU 和 DMA 引擎也可通过 AHB 总线访问这两个 SRAM。
- 串行线调试，带有八个断点、四个观察点和一个调试时间戳计数器。它包括串行线输出 (SWO) 跟踪和 ETM 跟踪。
- Cortex-M33 系统滴答定时器

DSP 处理器内核

- Cadence Tensilica Fusion F1 DSP 处理器，运行频率高达 200MHz。
- 硬件浮点单元
- 串行线调试 (与 Cortex-M33 控制域 CPU 共用)

通信接口

- 9 个可配置的通用串行接口模块 (Flexcomm 接口)。每个模块都包含集成的 FIFO 和 DMA 支持功能。九个模块中的每个模块都可以配置为以下接口：
 - 具有专用分数波特率生成和流量控制握手信号的 USART。USART 可以选择采用 32kHz 的时钟，当芯片处于低功耗模式时，采用 32kHz 时钟或外部提供的时钟来运行。USART 还提供了对 LIN2.2 的部分支持。
 - 具有多地址识别和监控模式的 I2C 总线接口。它支持 400Kb/s 的快速模式和 1Mb/s 的快速加模式。在从机模式下运行时，它还支持 3.4Mb/s 的高速率。
 - 一个 SPI 接口
 - 面向数字音频输入或输出的 I2S (I2C 音频) 接口。每个 I2S 最多支持四个通道对。
- 2 个额外的高速 SPI 接口，支持 50MHz 频率运行
- 1 个额外的带开漏端口 I2C 接口
- 2 个 I3C 总线接口
- 1 个数字麦克风接口，支持多达 8 个通道，配备降频数位滤波器和语音激活检测。一对通道的数据流可以直通到 I2S。DMIC 支持 DMA。

五个 I/O 电源轨

- 五个独立电源可为不同的引脚簇供电，允许直接连接到以不同电源电压运行的片外设备。

片上存储器

- 高达 5MB 的系统 SRAM，两个 CPU、两个 DMA 引擎、图形子系统和所有其他 AHB 主机均可访问。
- 额外的 SRAM 用于 USB 数据流（16KB）、Cortex-M33 协处理器（4 x 2KB）、SDIO FIFO（2 x 512B 双端口）、PUF 安全密钥生成（2KB）、FlexSPI 缓存（每个 32KB）、SmartDMA 命令（32KB）以及各种针对图形的双端口和单端口 RAM。
- 16k 位的 OTP 熔丝
- 高达 192KB 的 ROM 存储器，用于工厂编程的驱动程序和 API
- 通过 ROM 中的内置启动加载程序软件，从高速 SPI、FlexSPI 闪存、HS USB、I2C、UART 或 eMMC 进行系统启动。FlexSPI 启动模式还包括针对非安全启动的 XIP（Execute-in-place，就地执行）启动选项。

数字外设

- 两个通用 DMA 引擎，每个引擎有 37 个通道和多达 27 个可编程请求/触发源。
 - 可以配置为一个 DMA 是安全的，另一个是非安全的，和/或可以指定一个由 M33 CPU 使用，另一个由 DSP 使用
- 带有专用 32KB 代码 RAM 的智能 DMA 控制器
- USB 高速主/从控制器，配备内置 PHY 和专用 DMA 控制器。
- 两个 FlexSPI（八线/四线）接口，高达 200MHz DDR/SDR（目标）。32KB 高速缓存，具有基于可编程地址区域的可选择高速缓存策略。其中一个 FlexSPI 接口包含用于就地执行的即时解密功能，和支持双映像启动的地址重新映射功能。（两个模块都）支持 DMA。
- 两个 SD/eMMC 存储卡接口，配有专用 DMA 控制器。其中一个接口支持带 HS400/DDR 操作的 eMMC 5.0。

模拟外设

- 一个 12 位 ADC，采样速率为 1M 次/秒，搭配增强型 ADC 控制器。它支持多达 10 个单端通道或 5 个差分通道。ADC 支持 DMA。
- 温度传感器
- 模拟比较器

定时器

- 1 个 32 位 SC 定时器/PWM 模块（SCT）。多功能定时器提供大量的事件生成、匹配/比较以及复杂的 PWM 和输出控制功能。
 - 10 个通用/PWM 输出，8 个通用输入
 - 支持 DMA，可触发外部 DMA 事件
 - 支持分数匹配值，达成高分辨率
- 5 个具有 PWM 功能的通用 32 位定时器/计数器模块
- 24 位多速率定时器模块，具有 4 个通道，每个通道都能够以不同的可编程的频率产生重复中断。
- 2 个窗口式看门狗定时器（WDT），带有专用的看门狗振荡器（1 MHz 低功耗振荡器）
- 频率测量模块，可决定选择片内或片外时钟源的频率
- 具有独立电源和专用振荡器的实时时钟（RTC）。集成唤醒定时器可将芯片从低功耗模式唤醒。RTC 位于“始终开启”的电压域中。RTC 包括 8 个 32 位通用寄存器，当芯片其余部分断电时，这些寄存器可以保持其内容。
- 由看门狗振荡器运行的超低功耗微滴答定时器，具有时间戳捕获功能。可将芯片从低功耗模式唤醒。
- 2 个处理器共用的 64 位操作系统/事件定时器，具有单独的匹配/捕获和中断生成逻辑。上电复位后即启用。

时钟

- 晶体振荡器运行频率范围为 4MHz 至 26MHz。
- 双调整选项：内部 192/96MHz FRO 振荡器。可调整到 1% 的精度。
- FRO 能够使用精确的参考时钟（例如 XTAL Osc）微调至 0.1% 的精度，占空比为 46%，可支持 MIPI PHY 和 FlexSPI。
- 内置 1MHz 低功耗振荡器，精度为 5%。可用作看门狗振荡器，以及操作系统/事件定时器和其他的系统滴答的时钟。也可用作两个域的系统时钟。
- 32kHz 实时时钟（RTC）振荡器，可选用作系统时钟。
- 主系统锁相环（PLL）：
 - 支持 CPU 以最大速率运行，无需高频晶体。可运行自 FRO，晶体振荡器或 CLKIN 引脚。
 - 如果所需频率与主系统时钟的频率不同，第二个独立的 PLL 输出可为 DSP CPU 提供另一个高频时钟源。（注：主系统 PLL 的第二个 PFD 输出）
 - 另外两个 PLL 的输出可为各种外设提供所需的时钟源。
- 音频子系统的音频 PLL。

图形/多媒体

- 2D 矢量图形处理单元，运行频率高达 200MHz
- LCD 显示接口，支持智能 LCD 显示和视频模式
- MIPI DSI 接口，片上 PHY 支持高达 895.1Mbps 的传输速率
- FlexIO 可配置为向 LCD 提供并行接口

I/O 外设

- 多达 136 个通用 I/O (GPIO) 引脚，带有可配置的上拉/下拉电阻。端口可以字、半字、字节或位的方式写入。
- 镜像的安全 GPIO0。
- 单独的 GPIO 引脚可用作边沿和电平感应中断源，每个都有自己的中断向量。
- 所有 GPIO 引脚都能触发来自 GPIO_HS 模块的两个联合 (OR'd) 中断中的一个。
- 可以选择一组多达 7 个 GPIO 引脚 (来自端口 0/1) 进行布尔模式匹配，可以生成中断和/或驱动“模式匹配”输出。
- 可调节的输出驱动转换速率
- JTAG 边界扫描

安全性

- **安全隔离**：使用针对 Arm V8M 的 Trustzone 防止软件和远程攻击。AES 密钥的硬件隔离。
- **安全启动**：ROM 中的固件提供不可改变的信任根
- **安全存储**：基于物理上不可克隆功能 (PUF) 的密钥存储、用于存储代码的片外闪存的即时 AES 解密 (OTFAD)。
- **安全调试**：基于证书的调试身份验证机制
- **安全加载程序**：支持采用验签 (RSA 签名) 和保密 (AES-CTR 加密) 保护的固件更新机制。
- **安全标识**：符合 TCG DICE 规范的 128 位通用唯一标识符 (UUID)、256 位复合设备标识符 (CDI)
- **加密加速器**
 - 具有 128/192/256 位密钥强度，且可防止边侧信道分析 (差分功率分析和模板攻击) 的对称加密技术 (AES)
 - 使用 CASPER 协处理器的非对称加密加速
 - 符合 NIST SP 800-90b 的 TRNG 设计，每次调用有 512 位的输出
 - 带 SHA-256 和 SHA1 的哈希引擎

功率控制

- 主外接电源：1.8V ± 5%
- Vddcore 电源 (来自 PMIC 或内部 PMU)：可调范围为 0.6V 至 1.1V (包括保持模式)
- 模拟电源：1.71-3.6V
- 5 个 VDDIO 电源 (可共用或独立使用)：1.71 - 3.6V
- USB 电源：3.0-3.6V
- 低功耗模式：
 - 睡眠模式：CPU 时钟关闭 (每个 CPU 独立)
 - 深度睡眠模式：用户可通过 PDSLEEPCFG 选择配置
 - 深度断电模式：除“始终开启”域外，从整个芯片上去除内部电源
 - 每个单独的 SRAM 分区都可以独立断电或进入低功耗保持模式
 - DSP 域可独立于系统的其他部分单独断电。
 - 在睡眠或深度睡眠状态下，能够将同步串行接口运行行为从机或由 32 kHz RTC 振荡器提供时钟的 USART
 - 通过各种外设 (包括 RTC 和 OS/事件定时器) 的中断，从低功耗模式唤醒
- RBB/FBB 提供对功率/性能间平衡的额外控制
- 上电复位 (POR)

运行特性

- 温度范围 (环境温度)：-20°C 至 +70°C
- VDDCORE：0.7V - 1.155V
- VDDIO_0/1/2/4：1.71V - 1.89V
- VDDIO_3：1.71V - 3.6V

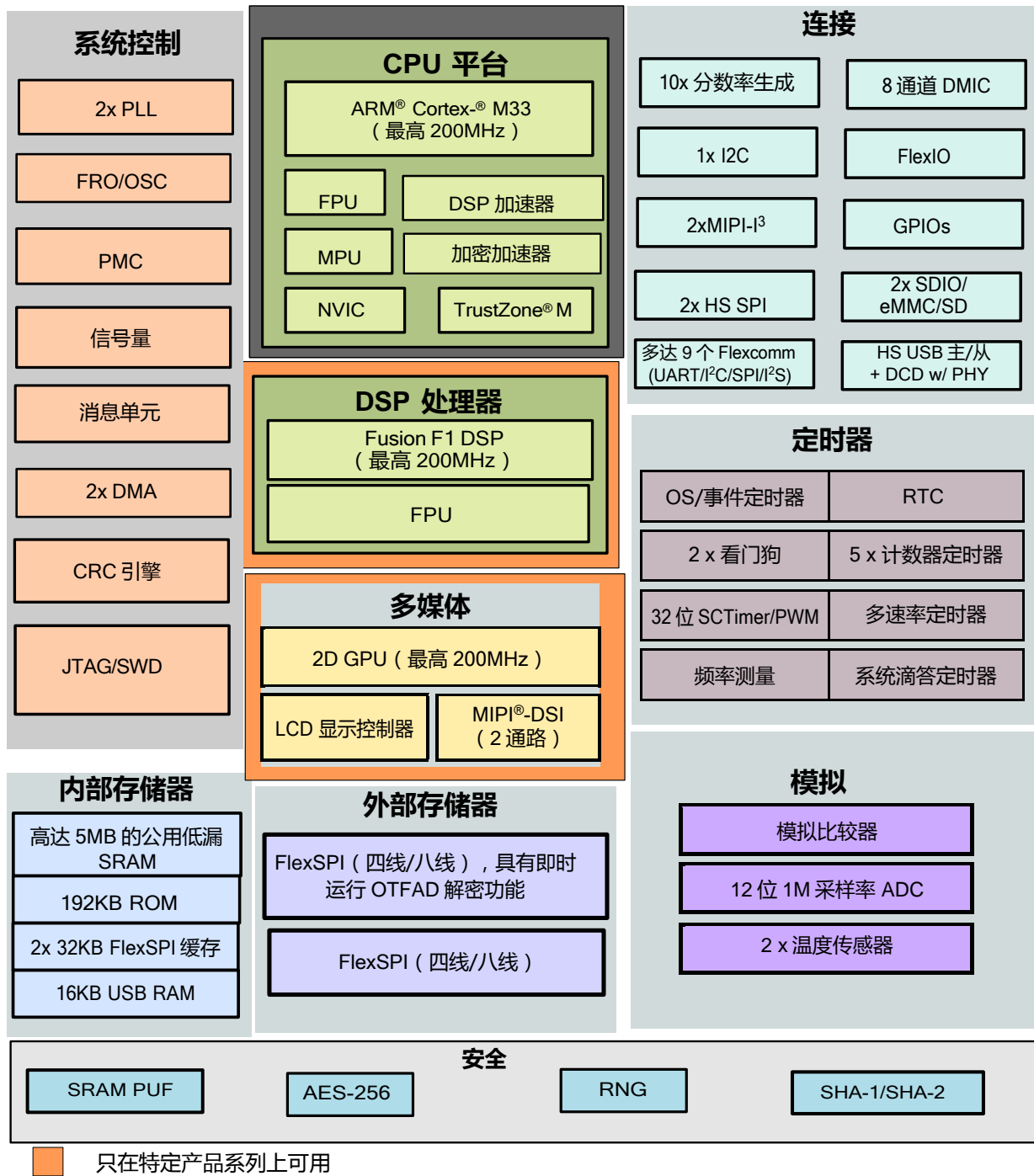


图 1. i.MX RT500 结构框图

下表提供了本数据表涵盖的可订购样品部件编号的示例。

可订购型号表

可订购的部件编号	部件编号 ¹	SRAM (MB)	DSP	图形	安全性	USB	I2S	封装
MIMXRT595SFFOC	MRT595SFFOC	5	有	有	SRAM PUF, AES256, HASH	HS	9	FOWLP249 ²
MIMXRT555SFFOC	MRT555SFFOC	5	无	有	SRAM PUF, AES256, HASH	HS	9	FOWLP249
MIMXRT533SFFOC	MRT533SFFOC	3	无	无	SRAM PUF, AES256, HASH	HS	9	FOWLP249
MIMXRT595SFFOCR	MRT595SFFOC	5	有	有	SRAM PUF, AES256, HASH	HS	9	FOWLP249 ²
MIMXRT555SFFOCR	MRT555SFFOC	5	无	有	SRAM PUF, AES256, HASH	HS	9	FOWLP249
MIMXRT533SFFOCR	MRT533SFFOC	3	无	无	SRAM PUF, AES256, HASH	HS	9	FOWLP249
MIMXRT533SFAWCR	MRT533SFAWC	3	无	无	SRAM PUF, AES256, HASH	HS	6	WLCSP141
MIMXRT555SFAWCR	MRT555SFAWC	5	无	有	SRAM PUF, AES256, HASH	HS	6	WLCSP141
MIMXRT595SFAWCR	MRT595SFAWC	5	有	有	SRAM PUF, AES256, HASH	HS	6	WLCSP141

1. 与包装上标注的一致。
2. 249 引脚扇出型晶圆级封装

器件修订编号

器件掩码集编号	SILICONREV_ID	JTAG_ID[CHIPREV]
2P43B	0x000B0002	0x2

i.MX RT 器件的包装标记由 4 组标识符组成，如下所示。

引脚 1 旋转角度

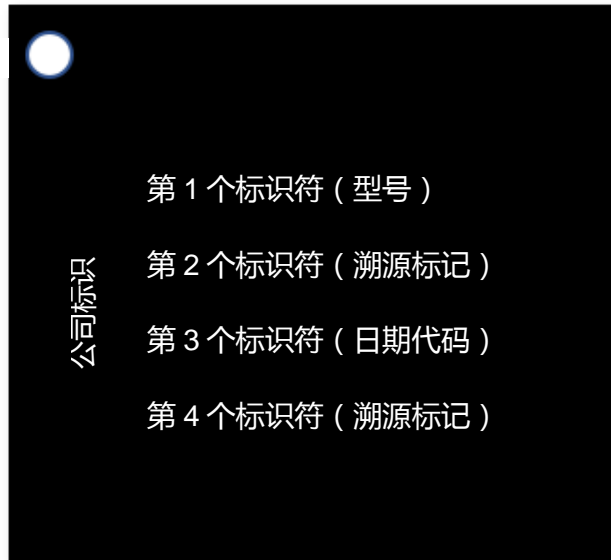


图 2. 包装标记

- 第 1 个标识符规定了部件编号，由 11 个字符组成。
- 第 2 个和第 4 个标识符规定了溯源标记。
- 第 3 个标识符规定了生产周的日期代码，是标准 5 字符格式的子集。

标准日期代码格式为 “xYYWW”：

- “x” 表示的前导数字可以忽略，而 “YYWW” 表示日期。
- “YY” 表示日历年（例如，19 对应 2019 年）。
- “ww” 表示日历年内工作周（例如，07 对应于第 7 工作周）。

请将这些信息提供给您当地的恩智浦代表，可获取更多详细信息。

下图解释此芯片的型号。

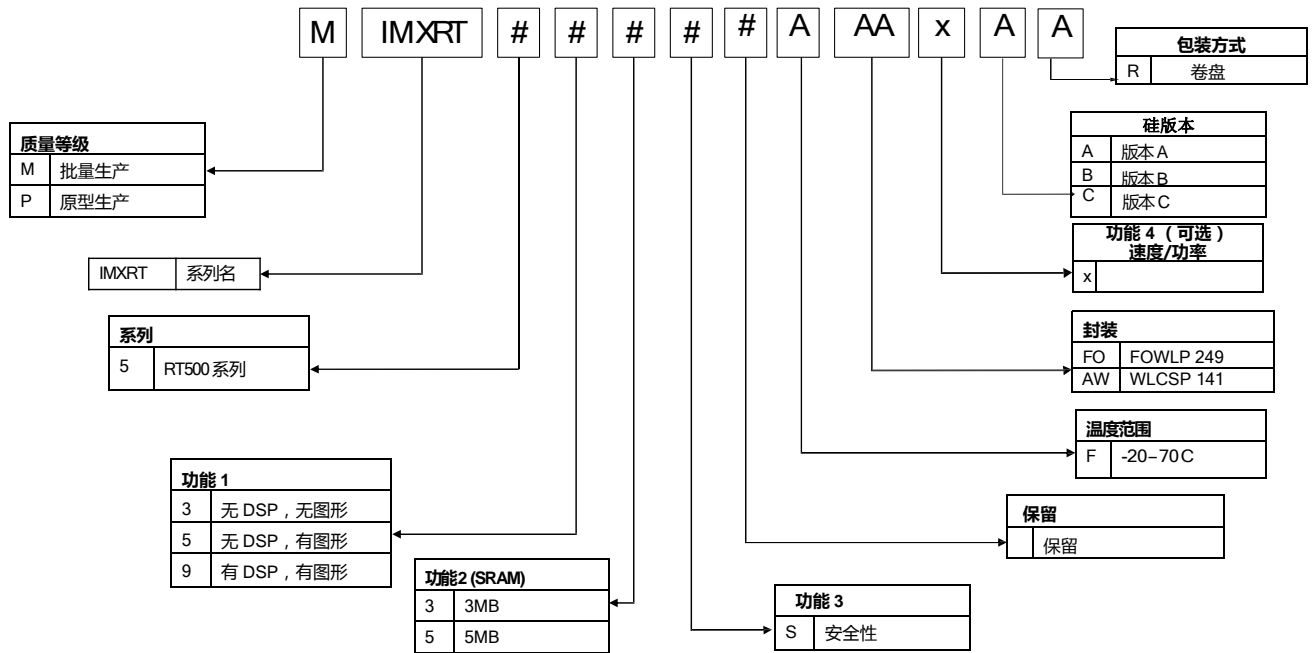


图 3. 部件编号图

相关资源

类型	说明
选型指南	Solution Advisor 是一个基于网页的工具，具有交互式应用向导和动态产品选型指南。
产品简介	产品简介包含简明的概述/综述信息，可快速评估设备的设计适用性。
参考手册	《i.MX RT500 低功耗跨界 MCU 参考手册》全面介绍了器件结构和性能（运行）。
数据手册	本文档包含了电气特性和信号连接信息。
芯片勘误表	芯片掩码集勘误表为特定设备掩码集提供附加或校正信息。

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1 Electrical characteristics

1.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See the following table for a quick reference to the individual tables and sections.

Table 1. i.MX RT500 chip-level conditions

For these characteristics	Topic appears
Absolute maximum voltage and current ratings	Absolute maximum voltage and current ratings
Thermal handling ratings	Thermal handling ratings
Moisture handling ratings	Moisture handling ratings
ESD handling ratings	ESD handling ratings
Thermal characteristics	Thermal characteristics
General operating conditions	General operating conditions
I/O parameters	I/O parameters
Power consumption operating behavior	Power consumption operating behavior

1.1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	—	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level (FOWLP)	—	3	—	1
MSL	Moisture sensitivity level (WLCSP)	—	1	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
I _{LAT}	Latch-up current at ambient temperature of 70 °C	-100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.1.4 Absolute maximum voltage and current ratings

Caution

Stress beyond those listed under the following table may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings¹

Symbol	Parameter	Conditions	Notes	Min.	Max.	Unit
VDD_AO1V8	Supply 1.8 V supply for “always on” features	-	2	-0.3	1.98	V
VDD1V8	1.8 V supply voltage for on-chip analog functions other than the ADC and comparator.	-	2	-0.3	1.98	V
VDD1V8_1	1.8 V supply voltage for on-chip digital logic	-	2	-0.3	1.98	V

Table continues on the next page...

Table 2. Absolute maximum ratings¹ (continued)

Symbol	Parameter	Conditions	Notes	Min.	Max.	Unit
VDDCORE	1.1 V input supply for core logic	On-chip regulator not used. LDO_ENABLE=0. Power supplied by an off-chip power management IC (PMIC).	2	-0.3	1.155	V
VDDIO_0/1/2/4	Supply voltage for GPIO pins	-	2	-0.3	1.98	V
VDDIO_3	Supply voltage for GPIO pins	-	2	-0.3	3.96	V
VDDA_ADC1V8	1.8 V analog supply voltage for ADC and comparator	-	2	-0.3	1.98	V
VDDA_BIAS	Bias voltage for ADC and comparator	-	2	-0.3	3.96	V
VREFP	ADC positive reference voltage	-	2	-0.3	1.98	V
USB1_VDD3V3	USB1 analog 3.3 V supply	-	2	-0.3	3.96	V
USB1_VBUS	USB1_VBUS detection	-	-	-0.3	5.6	V
MIPI_DSI_VDD11	MIPI DSI 1.1 V PHY input core voltage supply	-	-	-0.3	1.155	V
MIPI_DSI_VDD18	MIPI DSI 1.8 V PHY IO input voltage supply	-	-	-0.3	1.98	V
MIPI_DSI_VDDA_CAP	MIPI DSI 1.1 V capacitor output voltage supply	-	-	-0.3	1.155	V
I _{DD}	supply current (FOWLP249)	per supply pin, 1.71 V ≤ V _{DD} < 3.6 V	3	-	100	mA
	supply current (WCLSP141)	per supply pin, 1.71 V ≤ V _{DD} < 3.6 V	3	-	100	mA

Table continues on the next page...

Table 2. Absolute maximum ratings1 (continued)

Symbol	Parameter	Conditions	Notes	Min.	Max.	Unit
I _{SS}	ground current (FOWLP249)	per ground pin, 1.71 V ≤ V _{DD} < 3.6 V	3	-	100	mA
	ground current (WLCSP141)	per ground pin, 1.71 V ≤ V _{DD} < 3.6 V	3	-	100	mA
I _{latch}	I/O latch-up current	-(0.5V _{DD}) < V _I < (1.5V _{DD}); T _j < 105 °C		-	100	mA
P _{tot(pack)}	total power dissipation (per package)	FOWLP 249, based on package heat transfer, not device power consumption	4	-	1.86	W
	total power dissipation (per package)	WLCSP141		-	1.42	W

- In accordance with the Absolute Maximum Rating System (IEC 60134). The following applies to the limiting values:
 - This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
 - Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
 - The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in [Table 1](#).
- Maximum/minimum voltage above the maximum operating voltage (see [Table 1](#)) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.
- The peak current should not exceed the total supply current.
- Determined in accordance to JEDEC JESD51-2A natural convection environment (still air).

1.1.5 Thermal specifications

1.1.5.1 Thermal operating requirements

Table 3. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _j	Die junction temperature	-20	105	°C	1
T _A	Ambient temperature	-20	70	°C	1

- Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: T_J = T_A + R_{ΘJA} × chip power dissipation.

1.1.5.2 Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD} . The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 4. Thermal resistance¹

Symbol	Parameter	Conditions	Max/Min	Unit
249 FOWLP Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JESD51-9, 2s2p, still air	29.6	°C/W
$R_{\psi(JT)}$	thermal resistance from junction to package top	JESD51-9, 2s2p, still air	0.2	°C/W
141 WCLSP Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JESD51-9, 2s2p, still air	35.3	°C/W
$R_{\psi(JT)}$	thermal resistance from junction to package top	JESD51-9, 2s2p, still air	0.1	°C/W

1. Determined in accordance to JEDEC JESD51-2A natural convection environment (still air). Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment

1.1.6 General operating conditions

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 5. General operating conditions

Symbol	Parameter	Conditions	Min.	Typ. ¹	Max.	Unit
f_{clk}	CPU (Cortex-M33) clock frequency	-	-	-	200	MHz

Table continues on the next page...

Table 5. General operating conditions (continued)

Symbol	Parameter	Conditions	Min.	Typ. ¹	Max.	Unit
	CPU (Cortex-M33) clock frequency	For USB high-speed device and host operations	90	-	200	MHz
		For OTP programming only	-	-	120	MHz
f _{clk}	DSP clock frequency	-	-	-	200	MHz
	GPU clock frequency	-	-	-	200	MHz
VDD_AO1V8	Supply 1.8 V supply for “always on” features.	-	1.71	-	1.89	V
VDD1V8	1.8 V supply voltage for on-chip analog functions other than the ADC and comparator	-	1.71	-	1.89	V
VDD1V8_1 ²	1.8 V supply voltage for on-chip digital logic	-	1.71	-	1.89	V
VDDCORE ^{3, 4, 5, 6}	1.1 V supply for core logic. On-chip regulator not used. LDO_ENABLE = 0. Power supplied by an off-chip power management IC (PMIC).	Retention mode	0.6	-	1.155	V
		Active Mode (M33 Max Freq = 60 MHz, FBB) ⁷	0.7	-	-	V
		Active Mode (M33 Max Freq = 100 MHz, FBB)	0.8	-	-	V
		Active Mode (M33 Max Freq = 192 MHz, FBB)	0.9	-	-	V
		Active Mode (M33 Max Freq = 230 MHz ⁸ , FBB)	1.0	-	-	V
		Active Mode (M33 Max Freq = 275 MHz ⁸ , FBB)	1.1	-	-	V
VDDCORE ³	1.1 V supply for core logic. On-chip regulator not used. LDO_ENABLE = 0. Power supplied by an off-chip power management IC (PMIC).	Retention mode	0.6	-	1.155	V
		Active Mode (DSP Max Freq = 60 MHz, FBB) ⁷	0.7	-	-	V
		Active Mode (DSP Max Freq = 100 MHz, FBB)	0.8	-	-	V
		Active Mode (DSP Max Freq = 192 MHz, FBB)	0.9	-	-	V
		Active Mode (DSP Max Freq = 230 MHz ⁸ , FBB)	1.0	-	-	V
		Active Mode (DSP Max Freq = 275 MHz ⁸ , FBB)	1.1	-	-	V
VDDIO_0/1/2/4	supply voltage for GPIO rail	-	1.71	-	1.89	V

Table continues on the next page...

Table 5. General operating conditions (continued)

Symbol	Parameter	Conditions	Min.	Typ. ¹	Max.	Unit
VDDIO_3	supply voltage for GPIO rail	-	1.71	-	3.6	V
VDDA_1V8	1.8 V analog supply voltage for ADC and comparator	-	1.71	-	1.89	V
VDDA_BIAS ⁹	Bias for ADC and comparator	-	1.71	-	3.6	V
VREFP	ADC positive reference voltage	-	1.71	-	1.89	V
USB1_VDD3V3	USB1 analog 3.3 V supply	-	3.0	-	3.6	V
USB0_VBUS	USB0_VBUS detection	-	4.0 ¹⁰ or 3.0 ¹¹	5.0	5.5	V
MIPI_DSI_VDD11	MIPI DSI 1.1V digital core input voltage supply	-	0.85	-	1.155	V
MIPI_DSI_VDD18	MIPI DSI 1.8V PHY IO input voltage supply	-	1.71	-	1.89	V
MIPI_DSI_VDDA_C AP	MIPI DSI 1.1V digital core output voltage supply	-	-0.3	-	1.155	V

1. Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.
2. 1.8 V supply voltage for on-chip digital logic during active mode. In deep-sleep mode, this pin can be powered off to conserve additional current (~20 uA).
3. The maximum frequency for the specified VDDCORE voltage is the frequency of the main clock. This is before the CPU CLOCK Divider. The VDDCORE voltage has to be set according to the chosen main clock frequency.
4. When LDO_ENABLE is externally tied low, the user must boot at VDDCORE = 1.0 V or higher (Low power/Normal clock mode - OTP setting - BOOT_CLK_SPEED) or VDDCORE = 1.13 V (High Speed clock - OTP setting - BOOT_CLK_SPEED). Thereafter, the VDDCORE can be adjusted to the desired level.
5. When LDO_ENABLE is externally tied high, the on-chip regulator to the VDDCORE Core voltage in PMC is set to the default value 1.05 V (Low power/Normal clock mode - OTP setting - BOOT_CLK_SPEED) or 1.13 V (High Speed clock - OTP setting - BOOT_CLK_SPEED). Thereafter, the POWER_SetLdoVoltageForFreq API function can be used to internally configure the on-chip regulator voltage to the VDDCORE.
6. When performing any OTP read/write function, the VDDCORE voltage must be set to 1.0 V or higher when LDO_ENABLE is externally tied high or low.
7. GPU, SPI, and CTIMER are disabled.
8. Although i.MX RT500 is targeted to operate up to 200 MHz for low power operation, it can operate up to 275 MHz; however, there will be an increase in current consumption.
9. VDD_BIAS must be equal to maximum ADC input voltage or maximum comparator input voltage.
10. The USB PHY provides two options for reporting VBUS valid back to the USB controller:
 - A programmable internal VBUS_VALID comparator (the default option), or
 - An alternate VBUS_VALID_3V detector that will report VBUS valid for voltages above 3 V

USBPHY_USB1_VBUS_DETECTn[VBUSVALID_SEL] selects which option is used. If the VBUS_VALID comparator is used, USBPHY_USB1_VBUS_DETECTn[VBUSVALID_THRESH] determines the threshold voltage for a valid VBUS. The programmable range is 4.0V to 4.4V (default).

11. The USB PHY provides two options for reporting VBUS valid back to the USB controller:
- A programmable internal VBUS_VALID comparator (the default option), or
 - An alternate VBUS_VALID_3V detector that will report VBUS valid for voltages above 3 V

USBPHY_USB1_VBUS_DETECTn[VBUSVALID_SEL] selects which option is used. If the VBUS_VALID_3V detector is used, the detector voltage is not programmable.

1.1.7 I/O parameters

1.1.7.1 I/O DC parameters

T_{amb} = -20 °C to +70 °C, unless otherwise specified. Values tested in production unless otherwise specified.

Table 6. I/O DC characteristics

Sym bol	Parameter	Conditions	Notes	Min.	Typ. ¹	Max.	Unit
RESET pin, LDO_ENABLE pin, PMIC_IRQ_N pin, PMIC_MODE pins							
V _{IH}	HIGH-level input voltage			0.7 x VDD_AO1V8	-	VDD_AO1V8	V
V _{IL}	LOW-level input voltage			-0.3	-	0.3 x VDD_AO1V8	V
V _{OH}	HIGH-level output voltage	I _{OL} = -2.9 mA; 1.71 V ≤ VDD_AO1V8 < 1.89 V		0.8 x VDD_AO1V8	-	-	V
V _{OL}	LOW-level output voltage	I _{OL} = 2.9 mA; 1.71 V ≤ VDD_AO1V8 < 1.89 V		-	-	0.2 x VDD_AO1V8	V
V _{hys}	hysteresis voltage		2	-	0.06 x VDD_AO1V8	-	V
Standard I/O pins and PMIC I2C pins							
Input characteristics							
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled. 1.71 V ≤ VDD < 1.98 V		-1	-	1	μA
		V _I = 0 V; on-chip pull-up resistor disabled. 3.0 V ≤ VDD < 3.6 V		-1	-	1	μA
I _{IH}	HIGH-level input current	V _I = VDD; on-chip pull-down resistor disabled. 1.71 V ≤ VDD < 1.98 V		-1	0.5	1	μA
		V _I = VDD; on-chip pull-down resistor disabled. 3.0 V ≤ VDD < 3.6 V		-1	0.5	1	μA

Table continues on the next page...

Table 6. I/O DC characteristics (continued)

Sym bol	Parameter	Conditions	Notes	Min.	Typ. ¹	Max.	Unit
V _I	input voltage	pin configured to provide a digital function, except the following pins: V _{DDIO} = 0 V	3	0	-	3.6	V
V _{IH}	HIGH-level input voltage	1.71 V ≤ V _{DD} < 1.98 V		0.7 x V _{DDIO}	-	V _{DDIO}	V
		3.0 V ≤ V _{DD} ≤ 3.6 V		0.7 x V _{DDIO}	-	V _{DDIO}	V
V _{IL}	LOW-level input voltage	1.71 V ≤ V _{DD} < 1.98 V		-0.3	-	0.3 x V _{DDIO}	V
		3.0 V ≤ V _{DD} ≤ 3.6 V		-0.3	-	0.7	V
V _{hys}	hysteresis voltage	1.71 V ≤ V _{DD} < 1.98 V	2	0.15	-	-	V
		3.0 V ≤ V _{DD} ≤ 3.6 V	2	0.15	-	-	V
Output characteristics							
V _{OH}	HIGH-level output voltage (Normal drive)	IOH = -2.9 mA; 1.71 V ≤ V _{DD} < 1.98 V		0.8 x V _{DDIO}	-	-	V
		IOH = -4 mA; 3.0 V ≤ V _{DD} ≤ 3.6 V		0.8 x V _{DDIO}	-	-	V
V _{OH}	HIGH-level output voltage (Full drive)	IOH = -5.8 mA; 1.71 V ≤ V _{DD} < 1.98 V		0.8 x V _{DDIO}	-	-	V
		IOH = -8 mA; 3.0 V ≤ V _{DD} ≤ 3.6 V		0.8 x V _{DDIO}	-	-	V
V _{OL}	LOW-level output voltage (Normal Drive)	IOL = 2.9 mA; 1.71 V ≤ V _{DD} < 1.98 V		-	-	0.2 x V _{DDIO}	V
		IOL = 4 mA; 3.0 V ≤ V _{DD} ≤ 3.6 V		-	-	0.2 x V _{DDIO}	V
	LOW-level output voltage (Full Drive)	IOL = 5.8 mA; 1.71 V ≤ V _{DD} < 1.98 V		-	-	0.2 x V _{DDIO}	V
		IOL = 8 mA; 3.0 V ≤ V _{DD} ≤ 3.6 V		-	-	0.2 x V _{DDIO}	V
Weak input pull-up/pull-down characteristics							
I _{pd}	pull-down current	V _I = V _{DD}		34	-	180	μA
		V _I = 3.6 V	4	72	-	180	μA
I _{pu}	pull-up current	V _I = 0 V		-34	-	-180	μA
R _{pd}	pull-down resistance			20	-	50	kΩ
R _{pu}	pull-up resistance			20	-	50	kΩ

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 C), nominal supply voltage.

2. Guaranteed by design, not tested in production.

- All GPIO pins are fail safe up to 3.6 V when VDDIO supply = 0 V except following pins: PIO1_18 to PIO1_29, PIO1_30 to PIO1_31, PIO2_0 to PIO2_8, PIO2_24 to PIO2_31, PIO3_8 to PIO3_18, PIO4_11 to PIO4_17, and PIO5_15 to PIO5_18.
- Based on characterization. Not tested in production.

1.1.8 Power consumption operating behavior

NOTE

For the lowest power consumption, use the lowest SRAM partition number.

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 7. Power consumption in active mode

Symbol	Parameter	Conditions	Notes	Min.	Typ. ^{1, 2, 3}	Max.	Unit
Cortex M33 in Active mode, DSP no clock⁴							
enhanced while (1) code executed from SRAM partition 30⁵; Internal LDO disabled							
I _{DDVDDCORE}	VDDCORE supply current	HCLK = 12 MHz VDDCORE = 0.7 V	6	-	1.62	-	mA
		HCLK = 24 MHz VDDCORE = 0.7 V	6	-	2.50	-	mA
		HCLK = 48 MHz VDDCORE = 0.7 V	6	-	4.33	-	mA
		HCLK = 96 MHz VDDCORE = 0.8 V	6	-	9.35	-	mA
		HCLK = 192 MHz VDDCORE = 0.9 V	6	-	20.73	-	mA
		HCLK = 192 MHz VDDCORE = 1.0 V	6	-	23.97	-	mA
		HCLK = 192 MHz VDDCORE = 1.1 V	6	-	28.01	-	mA

- Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2/3/4 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3
- Characterized through bench measurements using typical samples.
- Compiler settings: IAR C/C++ Compiler for Arm ver 8.40.1. High, Speed, No Size Constraints. The optimization level is Low, Balanced.
- Based on the power API library from the SDK software package available on nxp.com
- SRAM partition 30 represents the worst case partition.
- FRO clock source, FBB enabled

Thermal specifications

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 8. Power consumption in active mode

Symbol	Parameter	Conditions		Min	Typ ^{1, 2, 3}	Max	Unit
Cortex M33 in Active mode, DSP no clock⁴							
CoreMark code executed from SRAM partition 30⁵							
I _{DDVDDCORE}	VDDCORE supply current	HCLK = 12 MHz VDDCORE = 0.7 V		-	1.61	-	mA
		HCLK = 24 MHz VDDCORE = 0.7 V		-	2.51	-	mA
		HCLK = 48 MHz VDDCORE = 0.7 V		-	4.26	-	mA
		HCLK = 96 MHz VDDCORE = 0.8 V		-	9.28	-	mA
		HCLK = 192 MHz VDDCORE = 0.9 V		-	20.44	-	mA
		HCLK = 192 MHz VDDCORE = 1.0 V		-	23.73	-	mA
		HCLK = 192 MHz VDDCORE = 1.1 V		-	27.87	-	mA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2/3/4 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3 V
2. Characterized through bench measurements using typical samples.
3. Compiler settings: IAR C/C++ Compiler for Arm ver 8.40. High Speed, No Size constraints. The optimization level is Low, Balanced.
4. Based on the power API library from the SDK software package available on nxp.com
5. SRAM partition 30 represents the worst case partition.

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 9. Power consumption in active mode

Symbol	Parameter	Conditions	Notes	Min	Typ ^{1, 2, 3}	Max	Unit
FFT code executed from SRAM partition 30 and 31⁴; Internal LDO disabled							
DSP in Active mode, M33 in WFI⁵							
I _{DDVDDCORE}	VDDCORE supply current	HCLK = 10 MHz VDDCORE = 0.7 V	6	-	1.80	-	mA
		HCLK = 40 MHz	6		5.30		mA

Table continues on the next page...

Table 9. Power consumption in active mode (continued)

Symbol	Parameter	Conditions	Notes	Min	Typ ^{1, 2, 3}	Max	Unit
		VDDCORE = 0.8 V					
		HCLK = 100 MHz VDDCORE = 0.8 V	6	-	10.74	-	mA
		HCLK = 150 MHz VDDCORE = 0.9 V	6	-	17.81	-	mA
		HCLK = 200 MHz VDDCORE = 0.9 V	6	-	22.94	-	mA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2/3/4 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3 V
2. Characterized through bench measurements using typical samples.
3. Compiler settings: IAR C/C++ Compiler for Arm ver 8.40. High Speed, No Size constraints. The optimization level is Low, Balanced.
4. SRAM partitions 30 and 31 represent the worst case partitions. The Fusion F1 DSP requires DRAM and IRAM in different partitions. DSP_DRAM is in partition 30, DSP_IRAM is in partition 31.
5. Based on the power API library from the SDK software package available on nxp.com
6. PLL clock source, FBB enabled

Table 10. Power consumption in sleep mode

Symbol	Parameter	Conditions	Notes	Min.	Typ.	Max.	Unit
Cortex-M33 in Sleep mode, DSP no clock¹							
I _{DDVDDCORE}	supply current	HCLK=12 MHz VDDCORE=0.7 V	2, 3, 4, 5	-	1.8	-	mA
		HCLK=12 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	4.27	-	mA
		HCLK=24 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	4.78	-	mA
		HCLK=48 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	5.78	-	mA
		HCLK=96 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	7.78	-	mA
		HCLK=192 MHz VDDCORE=0.9 V	2, 3, 4, 5	-	9.66	-	mA
		HCLK=192 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	11.74	-	mA

1. 256 KB SRAM, internal LDO enabled
2. All peripheral clocks gated
3. PLL disabled
4. FRO used as clock source
5. IAR C/C++ Compiler for Arm ver 8.4.2.1.236

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Thermal specifications

Table 11. Power consumption in deep sleep mode

Symbol	Parameter	Conditions	Notes	Min	Typ ^{1, 2}	Max ³	Unit
I _{VDD1V8}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	4	-	8.5	-	μA
I _{VDDCORE}	supply current	Deep-sleep mode; SRAM (32 KB) powered, Internal LDO disabled. Array On, Periphery Off T _{amb} = 25 °C	4	-	40.7	-	μA
		Deep-sleep mode; SRAM (32 KB) powered, Internal LDO disabled. Array On, Periphery Off T _{amb} = 70 °C	4	-	200	-	μA
I _{VDDCORE}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off T _{amb} = 25 °C	4	-	42.0	-	μA
		Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off T _{amb} = 70 °C	4	-	210	-	μA
I _{VDDCORE}	supply current	Deep-sleep mode; SRAM (5 MB) powered, Internal LDO disabled. Array On, Periphery Off T _{amb} = 25 °C	4	-	74	120	μA
		Deep-sleep mode; SRAM (5 MB) powered, Internal LDO disabled. Array On, Periphery Off T _{amb} = 70 °C	4	-	432	-	μA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). All power supplies = 1.8 V, except USB1_VDD3V3=3.3 V
2. Characterized through bench measurements using typical samples.
3. Guaranteed by characterization, not tested in production.
4. VDDCORE = 0.6 V, RBB Enabled

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 12. Power consumption in deep sleep mode

Symbol	Parameter	Conditions	Min	Typ ^{1, 2}	Max ³	Unit
I _{VDD_AO1V8}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.79	-	μA
I _{VDDIO_0}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	2.4	-	μA
I _{VDDIO_1}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	1.7	-	μA
I _{VDDIO_2}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.35	-	μA
I _{VDDIO_3}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.8	-	μA
I _{VDDIO_4}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.36	-	μA

Table continues on the next page...

Table 12. Power consumption in deep sleep mode (continued)

Symbol	Parameter	Conditions	Min	Typ ^{1, 2}	Max ³	Unit
I _{VDDA_1V8}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	11.8	-	μA
I _{VREFP}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.02	-	μA
I _{USB1_VDD3V3}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	1.10	-	μA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). All power supplies = 1.8 V, except USB1_VDD3V3=3.3 V
2. Characterized through bench measurements using typical samples.
3. Guaranteed by characterization, not tested in production.

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 13. Power consumption in deep power-down mode and full deep power-down modes

Symbol	Parameter	Conditions	Min	Typ ^{1, 2}	Max ³	Unit
I _{VDD_AO1V8}	supply current	Full Deep power-down mode; Internal LDO disabled. RTC Off $T_{amb} = 25\text{ °C}$	-	0.51	-	μA
		Full Deep power-down mode; Internal LDO disabled. RTC Off $T_{amb} = 70\text{ °C}$	-	1.79	-	μA
I _{VDDIO_0}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	2.4	-	μA
I _{VDDIO_1}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	1.68	-	μA
I _{VDDIO_2}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.45	-	μA
I _{VDDIO_3}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.37	-	μA
I _{VDDIO_4}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.44	-	μA
I _{VDD1V8}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	7.8	-	μA
I _{VREFP}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.01	-	μA
I _{USB1_VDD3V3}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	1.1	-	μA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). All power supplies = 1.8 V, except USB1_VDD3V3=3.3V
2. Characterized through bench measurements using typical samples.
3. Guaranteed by characterization, not tested in production.

1.1.9 CoreMark data

Table 14. Coremark data

Parameters	Conditions	Notes	Typ. ^{1, 2, 3}	Unit
ARM Cortex-M33 in active mode				
CoreMark Score	CoreMark code executed from SRAM; HCLK = 12 MHz	4	3.85	(Iterations/s) / MHz
	HCLK = 24 MHz	4	3.85	(Iterations/s) / MHz
	HCLK = 48 MHz	4	3.85	(Iterations/s) / MHz
	HCLK = 96 MHz	5	3.85	(Iterations/s) / MHz
	HCLK = 192 MHz	5	3.85	(Iterations/s) / MHz

1. Characterized through bench measurements using typical samples.
2. Compiler settings: IAR C/C++ Compiler for Arm ver 8.22.2, optimization level 3, optimized for time on.
3. VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2/3/4 = VDDA_ADC1V8 = VREFP = 1.8 V. VDDA_BIAS = USB1_VDD3V3 = 3.3 V
4. Clock source FRO. PLL disabled
5. Clock source external clock to XTALIN (bypass mode). PLL enabled.

1.2 System power and clocks

1.2.1 Power sequence

Following power-on sequence should be followed when using the internal LDO in i.MX RT500:

1. VDD_AO1V8, VDD1V8, and VDD1V8_1 pins should be powered first. There is no power sequence requirement between powering the VDD_AO1V8 and VDD1V8 pins.
2. VDDA_ADC1V8 and VREFP can be powered concurrently with VDD_AO1V8 and VDD1V8 or later
3. VDDIO_x and VDDA_BIAS pins can be powered concurrently with VDD_AO1V8 and VDD1V8 if these pins are 1.8 V range or later if these pins are 3.3 V range. If the VDDIO_x is not powered concurrently with the VDD1V8, the delta voltage between VDDIO_x and VDD1V8 must be 1.89 V or less.

The VDDCORE pin will be supplied from the internal LDO and the LDO is powered from the VDD1V8. An external capacitor (4.7 uF) must be connected on the VDDCORE pin. USB1_VDD3V3 can be powered at any time, independent of the other supplies.

Following power-on sequence should be followed when using an external PMIC or external IC to drive the VDDCORE pin (internal LDO is disabled, see timing diagram below):

1. VDD_AO1V8, VDD1V8, and VDD1V8_1 pins should be powered first. There is no power sequence requirement between powering the VDD_AO1V8 and VDD1V8 pins.
2. VDDA_ADC1V8 and VREFP can be powered concurrently with VDD_AO1V8 and VDD1V8 or later.
3. VDDIO_x and VDDA_BIAS pins can be powered concurrently with VDD1V8 if these pins are 1.8 V range or later if these pins are 3.3 V range. If the VDDIO_x is not powered concurrently with the VDD1V8, the delta voltage between VDDIO_x and VDD1V8 must be 1.89 V or less.
4. Power up the VDDCORE. The external RESETN should be held low until VDDCORE is valid in the timing diagram. VDDCORE should not be ramped up until after all the other supplies have completed ramp up.

USB1_VDD3V3 can be powered at any time, independent of the other supplies.

Sequence of operations is handled internally so there is no specific timing requirement between the supplies. The time delays caused by any of the bypass capacitors will have no effect on the operation of the part. The internal POR detectors on VDD_AO1V8, VDD1V8 pins, and the Low Voltage Detector on VDDCORE pin, require a fall time of at least 10 μ s (preliminary) to trigger. There is no restriction on the rise time, except for the sequencing defined above.

Table 15. Power-on characteristics

Symbol	Timing Parameter	Description	Min.	Max.	Unit
A	VDDIO_x valid to VDDCORE valid	The delay from when the IO pad voltages become valid to core voltage valid	10	-	μ s
B	VDDCORE valid to De-assertion of RESETN	The delay from when the VDD core is valid to when the RESETN can be released	20	-	μ s
AA	Mode pin valid	When the mode pins becomes valid. On power-on, the mode pins are reset to 00 and are controlled via a	-	2	μ s

Table 15. Power-on characteristics

Symbol	Timing Parameter	Description	Min.	Max.	Unit
		POR circuit in the always-on domain. The timing is from when the VDD_AO1V8 is valid to when the mode pins are reset to 00.			

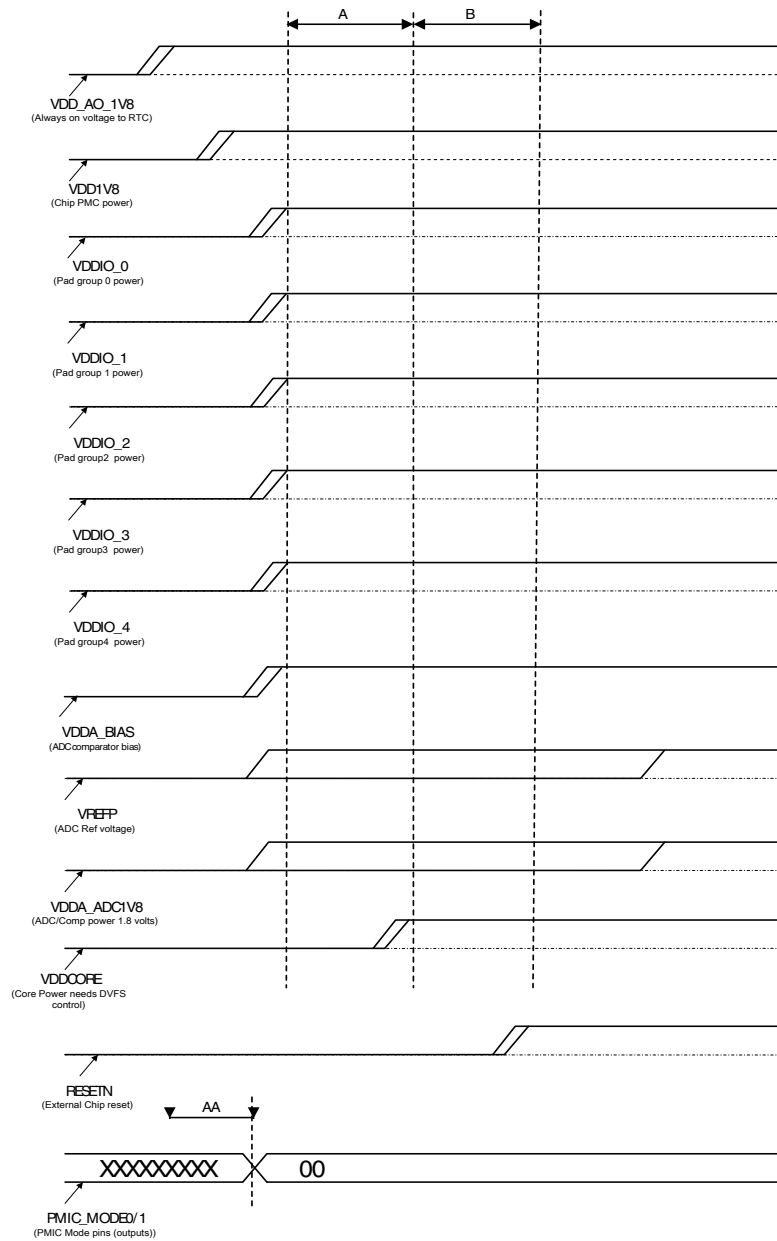


Figure 4. Power-up ramp

1.2.2 Free-running oscillator FRO-192/96M specifications

Table 16. FRO-192M specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$f_{fro192m}$	FRO-192M frequency (nominal)		192		MHz
$\Delta f_{fro192m}$	Frequency deviation <ul style="list-style-type: none"> • 1T trim (Open loop) 	—	—	± 1	% %

Table continues on the next page...

Thermal specifications

Table 16. FRO-192M specifications (continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{startup}	Start-up time	—	75	—	μs
jit_{cyc}	Cycle to cycle jitter	—	105	—	ps
I_{fro192m}	Current consumption	—	45	111	μA
V_{min}	Minimum voltage	0.8 ¹	—	—	V

1. $V_{\text{min}} = 0.8\text{ V}$ is derived from FRO192 MHz divided by 2/4/8.

NOTE

Any divided versions of the FRO that are not being used anywhere should be turned off to save power.

Table 17. FRO-96M specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{fro96m}	FRO-96M frequency (nominal)	96			MHz
Δf_{fro96m}	Frequency deviation • 1T trim (Open loop)	—	—	± 1	% %
t_{startup}	Start-up time	—	120	—	μs
jit_{cyc}	Cycle to cycle jitter	—	180	—	ps
I_{fro96m}	Current consumption	—	23	63	μA
V_{min}	Minimum voltage	0.7 ¹	—	—	V

1. $V_{\text{min}} = 0.7\text{ V}$ is derived from FRO96 MHz divided by 2/4/8.

1.2.3 Crystal oscillator

$T_{\text{amb}} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$; $1.71\text{ V} \leq V_{\text{DD}} \leq 1.89\text{ V}$.^{1, 2}

Table 18. Crystal oscillator characteristics

Symbol	Parameter	Min.	Typ. ³	Max.	Unit
f_{range}	oscillator frequency range	4	-	32	MHz
Rf	feedback resistor high gain mode only ⁴	-	1	-	$\text{M}\Omega$
ESR	Equivalent series resistance	-	-	80	Ω

1. Parameters are valid over operating temperature range unless otherwise specified.

2. See [XTAL oscillator](#)

3. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

4. CLKCTL0_SYSOSCCTL0[LP_ENABLE] = 1 sets High Gain Mode, which requires a 1 MΩ feedback resistor.

1.2.4 RTC oscillator

See [RTC oscillator](#) for connecting the RTC oscillator to an external clock source.

$$T_{amb} = -20\text{ °C to }+70\text{ °C}; 1.71 \leq V_{DD} \leq 1.89$$

Table 19. RTC oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ. ¹	Max.	Unit
f ₁	input frequency	-	-	32.768	-	kHz
ESR	Equivalent series resistance	-	-	50	100K	kΩ
t _{start_xtal} ²	Crystal oscillator start-up time	-	-	250	-	ms
t _{start_bypass} ²	Bypass oscillator start-up time	-	-	1	-	ms
V _{pp} ³	Peak-to-Peak amplitude of oscillation	With oscillator bypass mode enabled	0.7	-	VDD_AO1V8	V

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
2. Proper PCB layout procedures must be followed to achieve specifications.
3. In bypass mode, using an input square wave only on RTCXIN with RTXOUT floating.

1.2.5 External Clock Input (CLKIN) pin

$$T_{amb} = -20\text{ °C to }+70\text{ °C}; 1.71\text{ V to }1.89\text{ V}$$

Table 20. Dynamic characteristic: CLKIN

Symbol	Parameter	Conditions	Min.	Typ. ¹	Max	Unit
F _i	input frequency	-	-	-	50	MHz

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages

1.2.6 Internal low-power oscillator (1 MHz)

The IRC is trimmed to ±10% accuracy over the entire voltage and temperature range.

$$T_{amb} = -20\text{ °C to }+70\text{ °C}; 1.71 \leq V_{DD} \leq 1.89\text{ V}$$

Table 21. LPOSC characteristics

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
f _{osc} (RC)	LPOSC clock frequency	-	0.9	1	1.1	MHz

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

1.3 System modules

1.3.1 Reset timing parameters

The following figure shows the reset timing and [Table 22](#) lists the timing parameters.

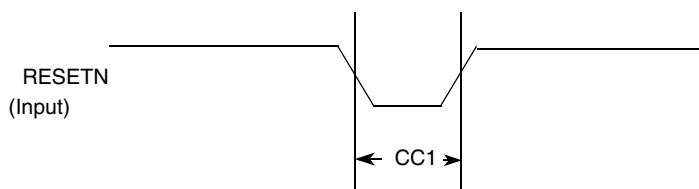


Figure 5. Reset timing diagram

Table 22. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid	40	-	ns

1.3.2 Serial Wire Debug (SWD) timing specifications

Table 23. SWD timing specifications

Symbol	Description	Min.	Max.	Min.— VLPR mode	Max.— VLPR mode	Unit
J1	SWD_CLK frequency of operation	0	25	0	10	MHz
J2	SWD_CLK cycle period	1000/J1	—	1000/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	20	—	ns
J4	SWD_CLK rise and fall times	—	3	—	3	ns

Table continues on the next page...

Table 23. SWD timing specifications (continued)

Symbol	Description	Min.	Max.	Min.— VLPR mode	Max.— VLPR mode	Unit
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	19	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	37	—	37	ns
J12	SWD_CLK high to SWD_DIO high-Z	2	—	2	—	ns

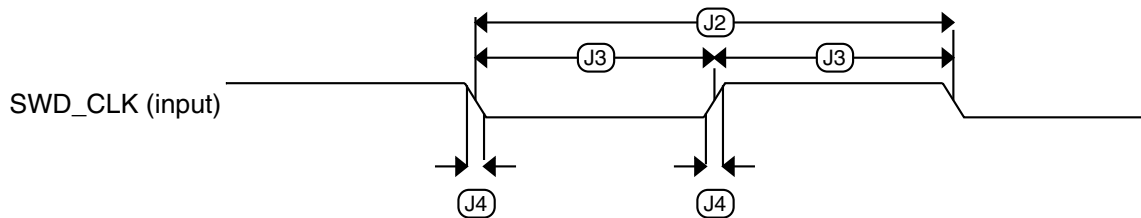


Figure 6. Serial wire clock input timing

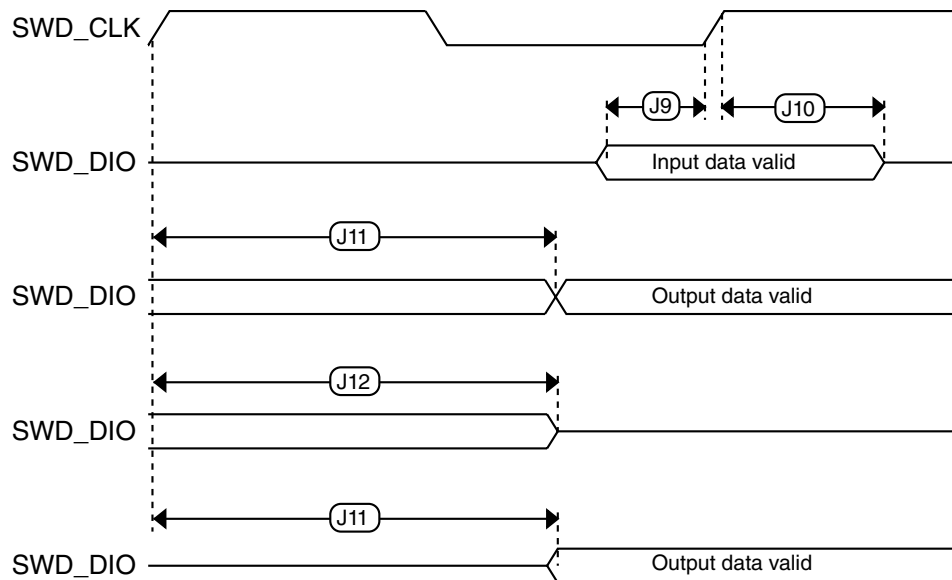


Figure 7. Serial wire data timing

1.3.3 JTAG timing specifications

Table 24. JTAG timing specifications

Symbol	Parameter	Min.	Max.	Min.— VLPR mode	Max.— VLPR mode	Unit
J1	TCLK frequency of operation					
	• Boundary Scan	0	10	0	10	MHz
	• JTAG	0	25	0	10	MHz
J2	TCLK cycle period	1000/J1	—	1000/J1	—	ns
J3	TCLK clock pulse width					
	• Boundary Scan	50	—	50	—	ns
	• JTAG	20	—	20	—	ns
J4	TCLK rise and fall times	—	3	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	5	—	5	—	ns
J7	TCLK low to boundary scan output data valid	—	28	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	10.5	—	19	—	ns
J10	TMS, TDI input data hold time after TCLK rise	2.5	—	2	—	ns
J11	TCLK low to TDO data valid	—	19	—	19	ns
J12	TCLK low to TDO high-Z	2	—	2	—	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	8	—	ns

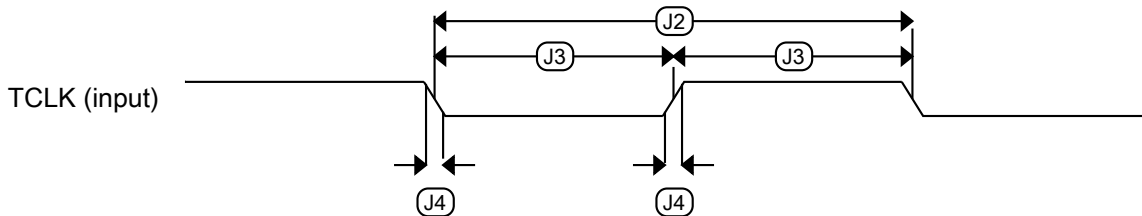


Figure 8. Test clock input timing

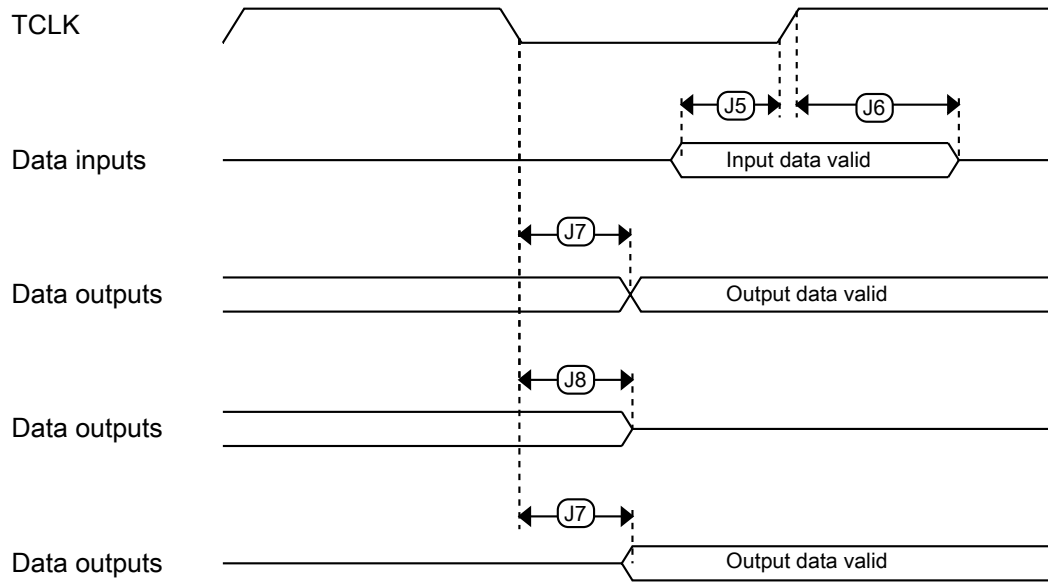


Figure 9. Boundary scan (JTAG) timing

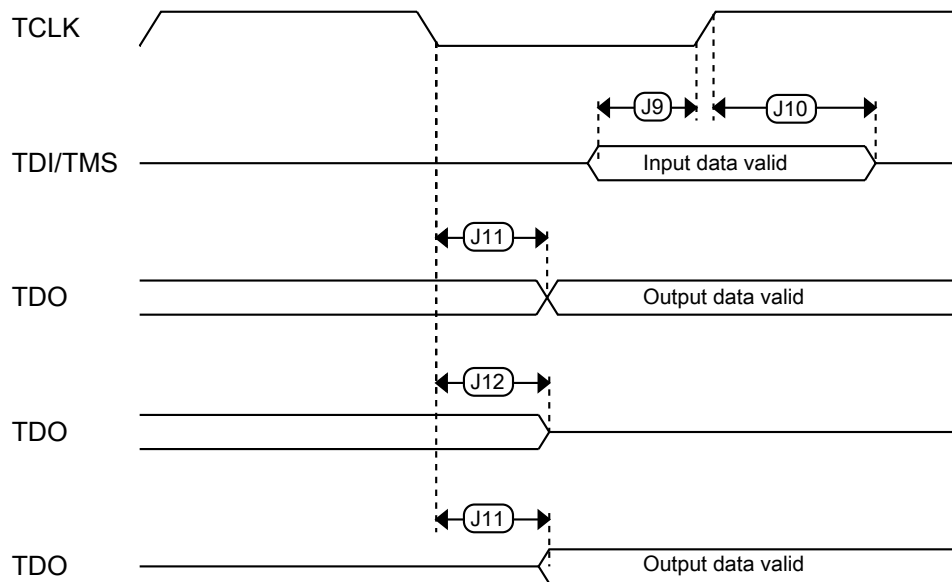


Figure 10. Test Access Port timing

Thermal specifications

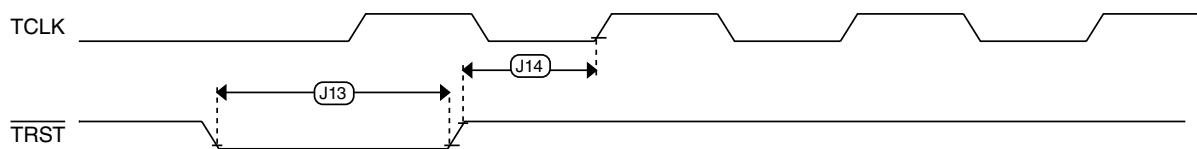


Figure 11. $\overline{\text{TRST}}$ timing

1.3.4 Wake-up process

$V_{DD} = 3.3 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; using FRO as the system clock.

Table 25. Typical wake-up times from low power modes

Symbol	Parameter	Conditions	Notes	Min.	Typ. ¹	Max.	Unit
t_{wake}	wake-up time	from sleep mode, 200 MHz	2, 3	-	150	-	μs
t_{wake}	wake-up time	from deep-sleep mode, using RESETN.	4	-	120	-	μs
t_{wake}	wake-up time	from deep-sleep mode, using PMIC_IRQ_N	4	-	120	-	μs
t_{wake}	wake-up time	from full deep power-down mode, using RESETN	4	-	8.64	-	ms
t_{wake}	wake-up time	from full deep power-down mode, using PMIC_IRQ_N	4	-	8.64	-	ms

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 C), nominal supply voltages.
2. The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.
3. FRO disabled, all peripherals off. PLL disabled.
4. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the Wake-Up pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

1.4 External memory interface

1.4.1 FlexSPI Flash interface

Tamb = -20 °C to +70 °C, VDDIO_x = 1.71 V to 1.89 V; VDDCORE = 1.13 V; CL = 5 pF balanced loading on all pins; Full Drive Mode on all pins, Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Table 26. Dynamic characteristics: FlexSPI flash interface1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SDR mode						
f _{clk}	clock frequency	Transmit	—	—	200	MHz
		RX clock source = 0	—	—	60	MHz
		RX clock source = 1	—	—	116	MHz
		RX clock source = 3	—	—	200	MHz
t _{DS}	data set-up time	RX clock source = 0 (internal dummy read strobe and loopbacked internally)	6	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad)	1	—	—	ns
		source = 3 (external DQS, Flash provides read strobe)	0	—	0.6	ns
t _{DH}	data hold time	RX clock source = 0 (internal dummy read strobe and loopbacked internally)	1	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad)	0	—	—	ns
		source = 3 (external DQS, Flash provides read strobe)	0	—	—	ns
t _{V(Q)}	data output valid time		0	—	3	ns
DDR Mode (with and without DQS)						
f _{clk}	clock frequency	Transmit	—	—	200	MHz

Table continues on the next page...

Table 26. Dynamic characteristics: FlexSPI flash interface¹ (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		RX clock source = 0	—	—	30	MHz
		RX clock source = 1	—	—	58	MHz
		RX clock source = 3, with external DQS.	—	—	200	MHz
t_{DS}	data set-up time	RX clock source = 0 (internal dummy read strobe and loopbacked internally)	6	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad)	1	—	—	ns
		source = 3 (external DQS, Flash provides read strobe)	0	—	0.6	ns
t_{DH}	data hold time	RX clock source = 0 (internal dummy read strobe and loopbacked internally)	1	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad)	0	—	—	ns
		source = 3 (external DQS, Flash provides read strobe)	0	—	—	ns
$t_{V(O)}$	data output valid time		0	—	—	ns

1. Based on simulation; not tested in production.

Following are the FlexSPI timing diagrams for SDR and DDR input and output timing modes.

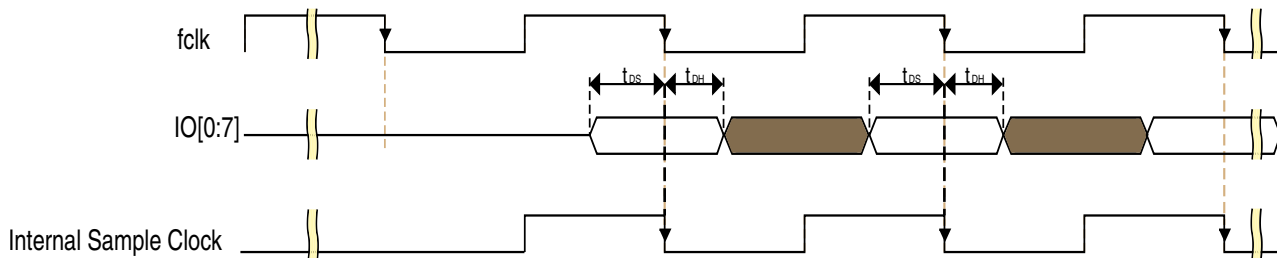


Figure 12. SDR mode (input timing, mode 0 and 1)

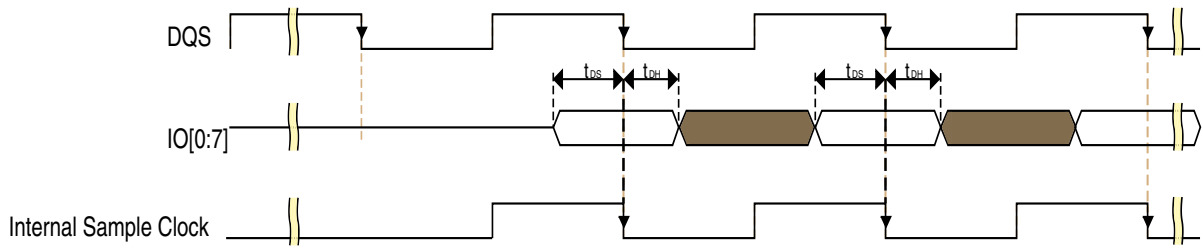


Figure 13. SDR mode (input timing, mode 3)

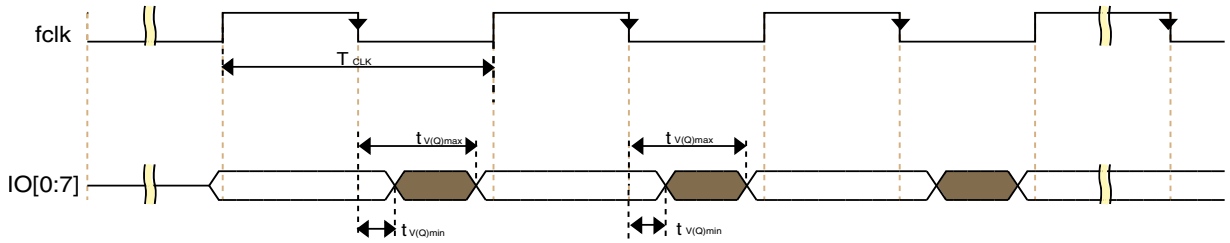


Figure 14. SDR mode (output timing, mode 0 and 1)

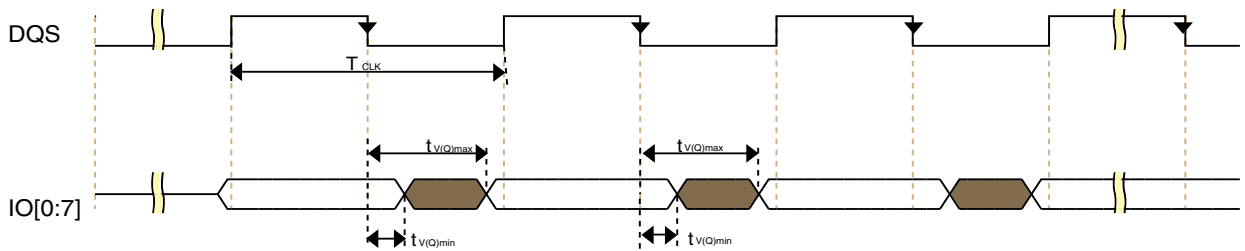


Figure 15. SDR mode (output timing, mode 3)

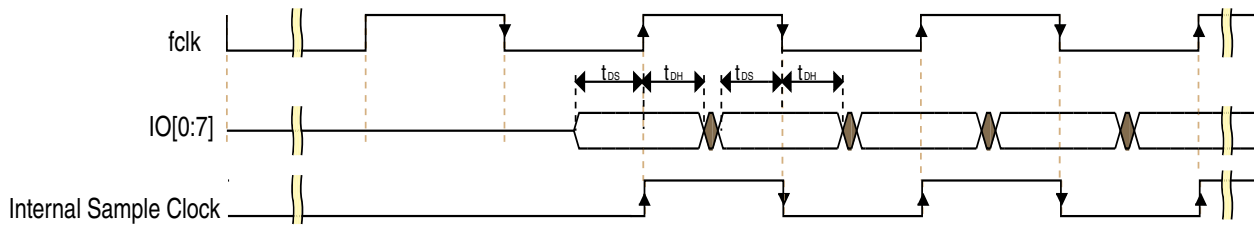


Figure 16. DDR mode (input timing, mode 0 and 1)

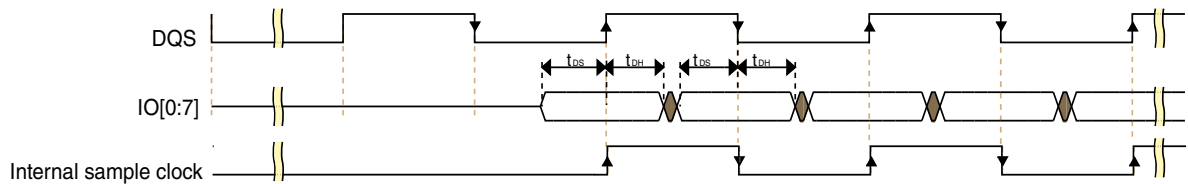


Figure 17. DDR mode (input timing, mode 3)

External memory interface

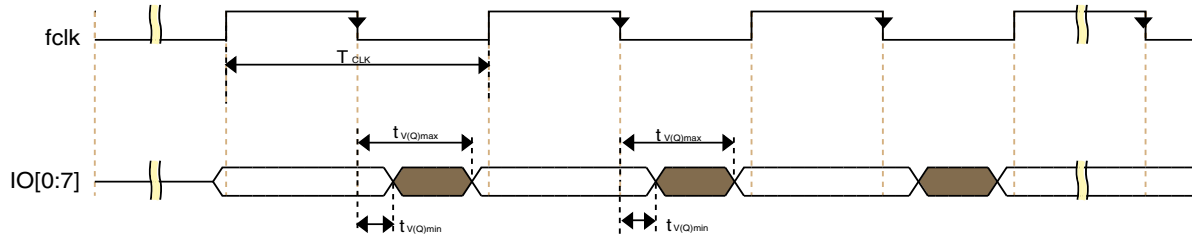


Figure 18. DDR mode (output timing, mode 0 and 1)

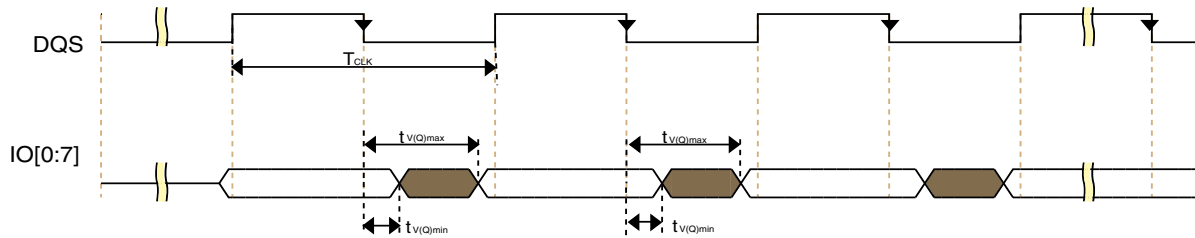


Figure 19. DDR mode (output timing, mode 3)

1.5 Display and graphics

1.5.1 LCDIF

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $V_{DD} = 2.7\text{ V}$ to 3.6 V ; $C_L = 30\text{ pF}$. Simulated values.

Table 27. LCDIF characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	-	60	MHz
$t_{v(Q)}$	data output valid time	on all LCD output pins	0.3	-	4.5	ns

1.5.2 MIPI DSI timing

The i.MX RT500 conforms to the MIPI D-PHY electrical specifications MIPI DSI Version 1.01 and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) for MIPI display port x2 lanes.

1.5.3 Flexible IO controller (FlexIO)

Table 28. FlexIO timing specifications

Symbol	Description	Min	Typ.	Max.	Unit	Notes
t_{ODS}	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0	—	1.957	ns	1
t_{IDS}	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0	—	1.403	ns	1

1. Assumes pins muxed on same VDD_IO domain with same load

1.6 Analog characteristics

1.6.1 12-bit ADC characteristics

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$; $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$; $V_{SSA} = V_{REFN} = \text{GND}$. ADC calibrated at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Table 29. 12-bit ADC static characteristics

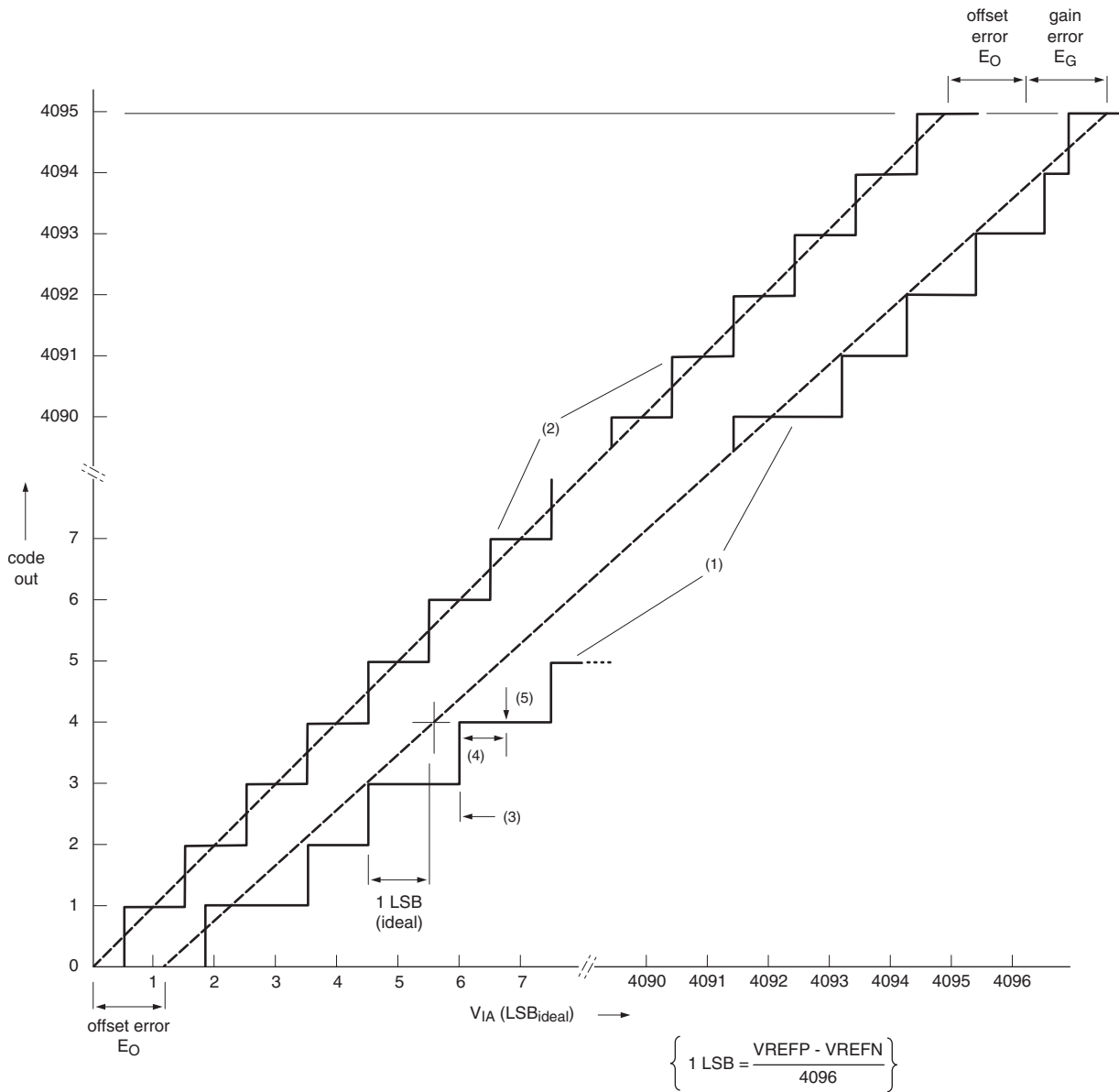
Symb ol	Parameter	Conditions	Notes	Min	Typ ¹	Max	Unit
VADIN	analog input voltage		See Figure 21	VREFN	-	VREFP	V
$f_{clk(ADC)}$	ADC clock frequency				-	60	MHz
f_s	sampling frequency			-	-	1	Msamples/s
$C_{sample s}$	Sample cycles			3.5	-	131.5	
$C_{compare}$	Fixed compare cycles			-	17.5	-	cycles
$C_{conversion}$	Conversion cycles			$C_{conversion} = C_{samples} + C_{compare}$			cycles
CADIN	Analog input capacitance		² , See Figure 21	-	4.5	-	pF
RADIN	Input resistance		See Figure 21	-	500	-	Ω
RAS	Analog source resistance		³	-	-	5	k Ω
E_D	differential linearity error		^{4, 5}	-	$<\pm 1$	-	LSB
$E_{L(adj)}$	integral non-linearity	$f_{clk(ADC)} = 22\text{ MHz}$ Sample Time select (STS bit in CMDH register) = 0	^{4, 6}	-	$<\pm 1.1$	-	LSB

Table continues on the next page...

Table 29. 12-bit ADC static characteristics (continued)

Symbol	Parameter	Conditions	Notes	Min	Typ ¹	Max	Unit
E_O	offset error		4, 7	-	$<\pm 1$	-	LSB
$V_{err(FS)}$	full-scale error voltage		4, 8	-	± 0.3	-	%

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
2. CADIN represents the external capacitance on the analog input channel for sampling speeds of 1.0 Msamples/s. No parasitic capacitances included.
3. This resistance is external to the MCU. To achieve the best results, the analog source resistance must be kept as low possible. The results in this data sheet were derived from a system that had less than 15 Ω analog source resistance. See [Figure 1](#)
4. Based on characterization; not tested in production.
5. The differential linearity error (ED) is the difference between the actual step width and the ideal step width. See [Figure 1](#).
6. The integral non-linearity ($EL_{(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 1](#).
7. The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 1](#).
8. The full-scale error voltage or gain error (EG) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 1](#).



- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential linearity error (E_D).
- (4) Integral non-linearity ($E_{L(adj)}$).
- (5) Center of a step of the actual transfer curve.

Figure 20. 12-bit ADC characteristics

1.6.1.1 ADC input impedance

The following figure shows the ADC input impedance for this device.

External memory interface

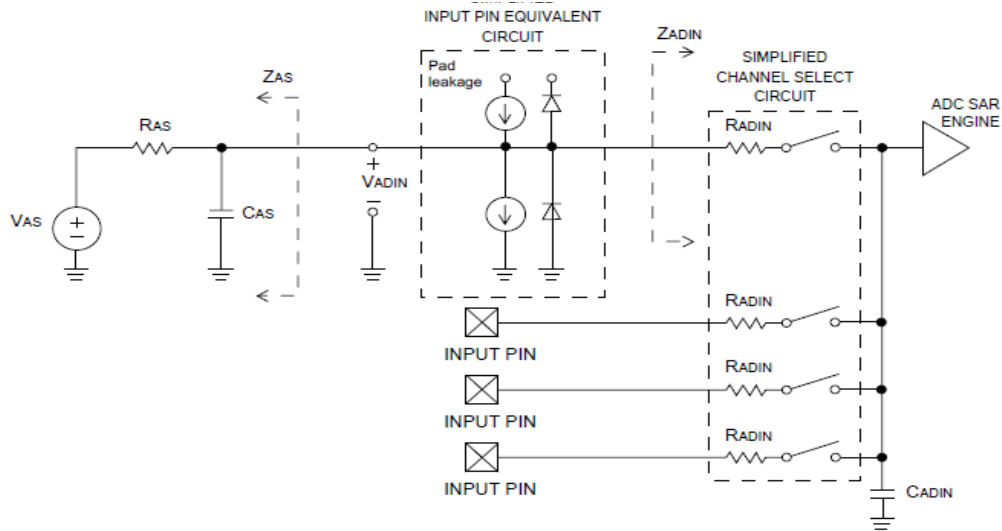


Figure 21. ADC input impedance

1.6.2 Temperature sensor

Table 30. Temperature sensor static and dynamic characteristics
(VDDA_BIAS = 3.3 V, All other supplies = 1.8 V)

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
DT _{sen}	sensor temperature accuracy	T _{amb} = -20 °C to 70 °C	1	-	-	2.77	°C
E _L	linearity error	T _{amb} = -20 °C to 70 °C		-	-	2.79	°C

1. Absolute temperature accuracy. Based on characterization. Not tested in production

Table 31. Temperature sensor Linear-Least-Square (LLS) fit parameters
(VDDA_BIAS = 3.3 V, All other supplies = 1.8 V)

Fit parameter	Conditions	Notes	Min	Typ	Max	Unit
LLS slope	T _{amb} = -20 °C to 70 °C	1, 2	-	-1.5738	-	mV/°C
LLS intercept at 0° C	T _{amb} = -20 °C to 70 °C	1, 2	-	809.55	-	mV
LLS intercept at 25 °C	T _{amb} = -20 °C to 70 °C	1, 2	-	770.4	-	mV

1. Based on characterization, Not tested in production.

2. Equation: $Temp = 25 - ((V_{temp} - V_{temp25})/m)$ Where: VTEMP is the voltage of the temperature sensor channel at the ambient temperature VTEMP is the voltage of the temperature sensor channel at 25°C and VDD = 1.8 V m is the voltage versus temperature slope in V/°C.

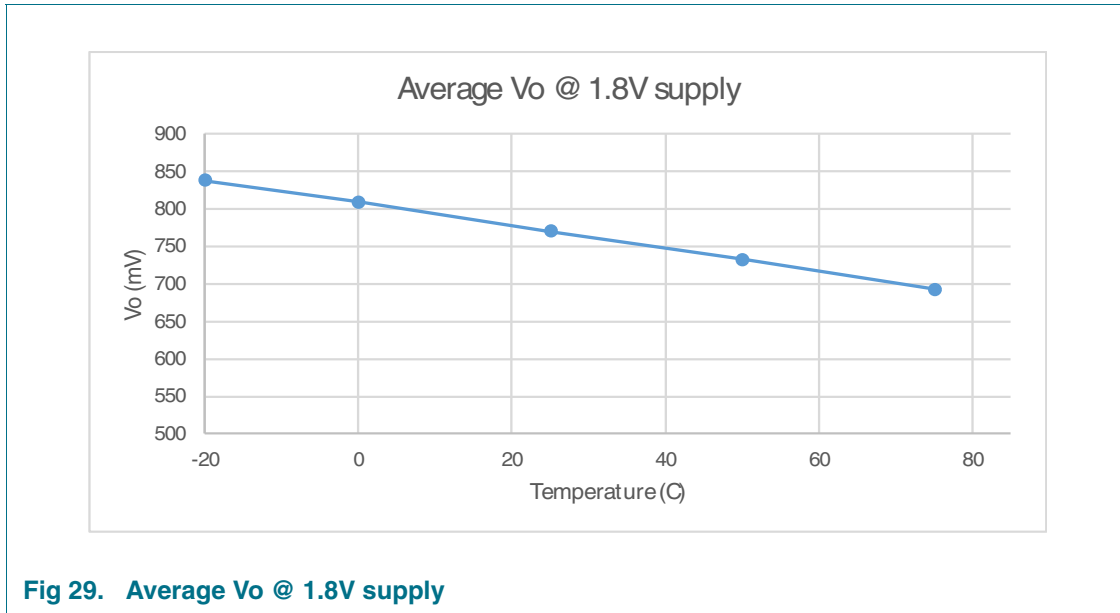


Figure 22. Average Vo @ 1.8V supply

1.6.3 Comparator characteristics

$T_{amb} = -20\text{ C to }+70\text{ C}$; $V_{DD} = 1.8\text{ V to }3.6\text{ V}$.

Table 32. Comparator characteristics

Symbol	Parameter	Conditions	Notes	Min.	Typ. ¹	Max.	Unit
Static characteristics							
Voffset	offset voltage	$V_{IC} = 0.1\text{ V}$; $V_{DD} = 1.8\text{ V}$		—	6	—	mV
		$V_{IC} = 0.9\text{ V}$; $V_{DD} = 1.8\text{ V}$		—	7	—	mV
		$V_{IC} = 1.7\text{ V}$; $V_{DD} = 1.8\text{ V}$		—	9	—	mV
Dynamic characteristics							
t_{PD}	propagation delay	HIGH to LOW; $V_{DD} = 1.8\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ $V_{IC} = 0.1\text{ V}$; 100 mV overdrive input	2	—	2	—	μs
		$V_{IC} = 0.1\text{ V}$; rail-to-rail input		—	915	—	ns
		$V_{IC} = 0.9\text{ V}$; 100 mV overdrive input	2	—	525	—	ns
		$V_{IC} = 0.9\text{ V}$; rail-to-rail input		—	600	—	ns

Table continues on the next page...

Table 32. Comparator characteristics (continued)

Symbol	Parameter	Conditions	Notes	Min.	Typ. ¹	Max.	Unit
		$V_{IC} = 1.7\text{ V}$; 100 mV overdrive input	2	—	500	—	ns
		$V_{IC} = 1.7\text{ V}$; rail-to-rail input		—	350	—	ns
t_{PD}	propagation delay	HIGH to LOW; $V_{DD} = 1.8\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{IC} = 0.1\text{ V}$; 100 mV overdrive input	2	—	270	—	ns
		$V_{IC} = 0.1\text{ V}$; rail-to-rail input		—	310	—	ns
		$V_{IC} = 0.9\text{ V}$; 100 mV overdrive input	2	—	340	—	ns
		$V_{IC} = 0.9\text{ V}$; rail-to-rail input		—	210	—	ns
		$V_{IC} = 1.7\text{ V}$; 100 mV overdrive input	2	—	150	—	ns
		$V_{IC} = 1.7\text{ V}$; rail-to-rail input		—	125	—	ns
t_{PD}	propagation delay	LOW to HIGH; $V_{DD} = 1.8\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{IC} = 0.1\text{ V}$; 100 mV overdrive input		—	5.8	—	μs
		$V_{IC} = 0.1\text{ V}$; rail-to-rail input		—	470	—	ns
		$V_{IC} = 0.9\text{ V}$; 100 mV overdrive input	2	—	750	—	ns
		$V_{IC} = 0.9\text{ V}$; rail-to-rail input		—	600	—	ns
		$V_{IC} = 1.7\text{ V}$; 100 mV overdrive input	2	—	5.5	—	μs
		$V_{IC} = 1.7\text{ V}$; rail-to-rail input		—	1.25	—	μs
t_{PD}	propagation delay	LOW to HIGH; $V_{DD} = 1.8\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{IC} = 0.1\text{ V}$; 100 mV overdrive input		—	105	—	ns
		$V_{IC} = 0.1\text{ V}$; rail-to-rail input		—	115	—	ns
		$V_{IC} = 0.9\text{ V}$; 100 mV overdrive input	2	—	110	—	ns
		$V_{IC} = 0.9\text{ V}$; rail-to-rail input		—	120	—	ns
		$V_{IC} = 1.7\text{ V}$; 100 mV overdrive input	2	—	110	—	ns

Table continues on the next page...

Table 32. Comparator characteristics (continued)

Symbol	Parameter	Conditions	Notes	Min.	Typ. ¹	Max.	Unit
		$V_{IC} = 1.7\text{ V}$; rail-to-rail input		—	120	—	ns
V_{hys}	hysteresis voltage ³	HYSTCRT[1:0] = 01	—	—	13	—	mV
		HYSTCRT[1:0] = 10		—	27	—	mV
		HYSTCRT[1:0] = 11		—	35	—	mV

1. Characterized on typical samples, not tested in production
2. 100 mV overdrive corresponds to a square wave from 50 mV below the reference (V_{IC}) to 50 mV above the reference.
3. Input hysteresis is relative to the reference input channel and is software programmable.

1.7 Communication interfaces

1.7.1 USART interface

Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 20 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 20.0 Mbit/s.

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (HCLK), and capacitive loading.

$T_{amb} = -20\text{ °C}$ to 70 °C ; $V_{DD} = 1.71\text{ V}$ to 1.89 V ; $C_L = 20\text{ pF}$ balanced loading on all pins; Input slew = 1 ns , SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Table 33. USART interface characteristics¹

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USART master (in synchronous mode)						
$t_{su(D)}$	data input set-up time	-	0.087	-	-	ns
$t_{h(D)}$	data input hold time	-	0.03	-	-	ns
$t_{v(Q)}$	data output valid time	-	14.058	-	16.412	ns
USART slave (in synchronous mode)						
$t_{su(D)}$	data input set-up time	-	0.087	-	-	ns
$t_{h(D)}$	data input hold time	-	0.03	-	-	ns

Table continues on the next page...

Table 33. USART interface characteristics¹ (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{v(Q)}$	data output valid time	-	0	-	3.684	ns

1. Based on simulation; not tested in production

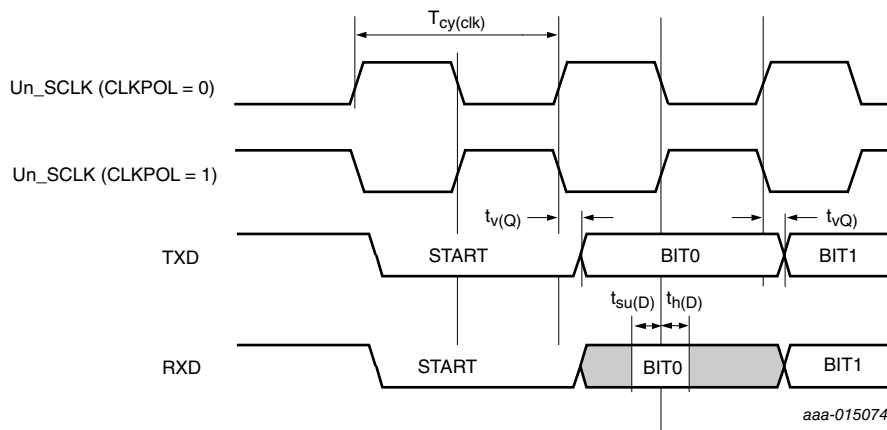


Figure 23. USART timing

1.7.2 I²C-bus

$T_{amb} = -20\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}; 1.71\text{ V} \leq V_{DD} \leq 1.89\text{ V.}^1$

Table 34. I²C-bus pins¹

Symbol	Parameter	Notes	Conditions	Min.	Max.	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	2, 3, 4, 5	Both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	$20 \times (V_{DD}/3.6V)$	300	ns
t_{LOW}	LOW period of the SCL clock	6	Standard-mode	4.7	-	μs
			Fast-mode	1.3	-	μs
			Fast-mode Plus	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock	6	Standard-mode	4	-	μs
			Fast-mode	0.6	-	μs

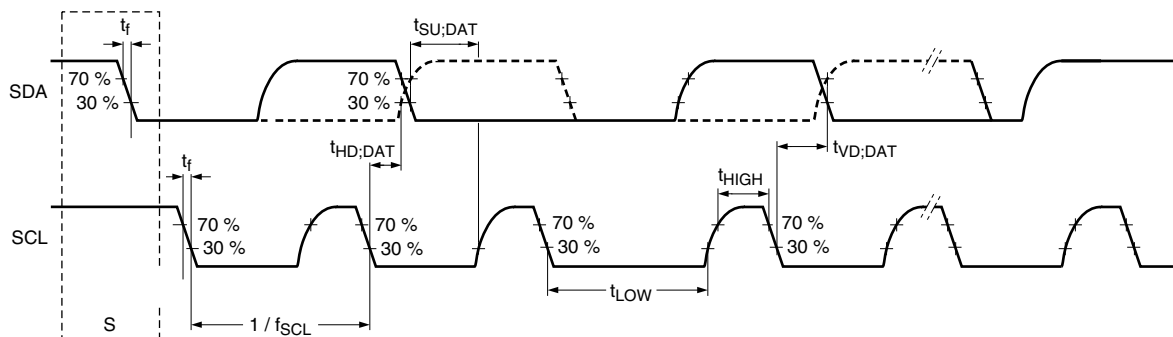
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1. Parameters are valid over operating temperature range unless otherwise specified. See the I2C-bus specification UM10204 for details.

Table 34. I²C-bus pins¹ (continued)

Symbol	Parameter	Notes	Conditions	Min.	Max.	Unit
$t_{HD;DAT}$	data hold time	7, 2, 8	Fast-mode Plus	0.26	-	μs
			Standard-mode	0	-	μs
			Fast-mode	0	-	μs
			Fast-mode Plus	0	-	μs
$t_{SU;DAT}$	data set-up time	9, 10	Standard-mode	4.7	-	ns
			Fast-mode	0.6	-	ns
			Fast-mode Plus	0.26	-	ns

- Guaranteed by design. Not tested in production.
- A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}(\text{min})$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.
- The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f .
- In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- The MSTTIME register allows programming of certain times for the clock (SCL) high and low times. Please see i.MX RT500 Low-Power Crossover MCU Reference Manual for further details.
- $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
- The maximum $t_{HD;DAT}$ could be $3.45 \mu\text{s}$ and $0.9 \mu\text{s}$ for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
- $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.
- A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT} = 250 \text{ ns}$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r(\text{max}) + t_{SU;DAT} = 1000 + 250 = 1250 \text{ ns}$ (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

Figure 24. I²C bus pins clock timing

1.7.3 I²S-bus interface

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $V_{DD} = 1.71\text{ V}$ to 1.89 V ; $C_L = 30\text{ pF}$ balanced loading on all pins; Input slew = 1.0 ns , SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Table 35. I²S-bus interface pins1, 2

Symbol	Parameter	Conditions	Notes	Min.	Typ. ³	Max.	Unit
Common to master and slave							
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK ⁴					
				$(T_{cyc}/2) - 1$	-	$(T_{cyc}/2) + 1$	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK ⁴					
				$(T_{cyc}/2) - 1$	-	$(T_{cyc}/2) + 1$	ns
Master							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SD A	5				
				6.798	-	17.505	ns
		on pin I2Sx_WS					
				5	-	16.055	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SD A	5	1.3	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SD A	5	2.9	-	-	ns
Slave							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SD A	5	13.8		23.6	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SD A	5	4.7	-	-	ns
		on pin I2Sx_WS		0.9	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SD A	5	0	-	-	ns
		on pin I2Sx_WS		0	-	-	ns

1. Based on simulation; not tested in production.
2. The Flexcomm Interface function clock frequency should not be above 48 MHz. See the data rates section in the I2S chapter in the i.MX RT500 Low-Power Crossover MCU Reference Manual (IMXRT500RM) to calculate clock and sample rates.
3. Typical ratings are not guaranteed.
4. Based on simulation. Not tested in production.
5. Clock Divider register (DIV) = 0x0.

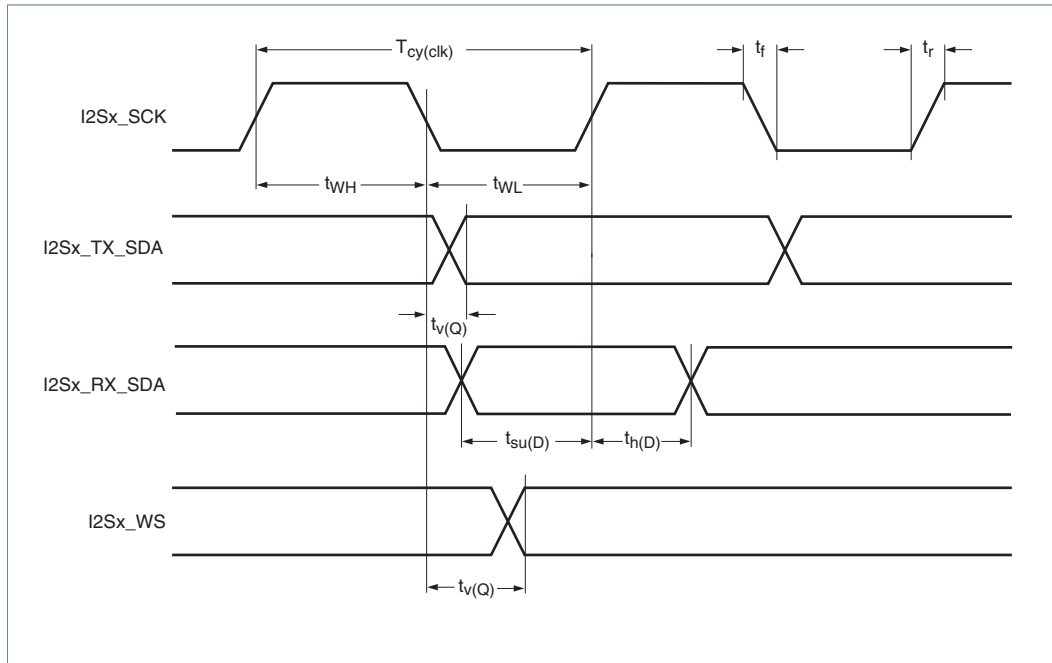


Figure 25. I²S-bus timing (master)

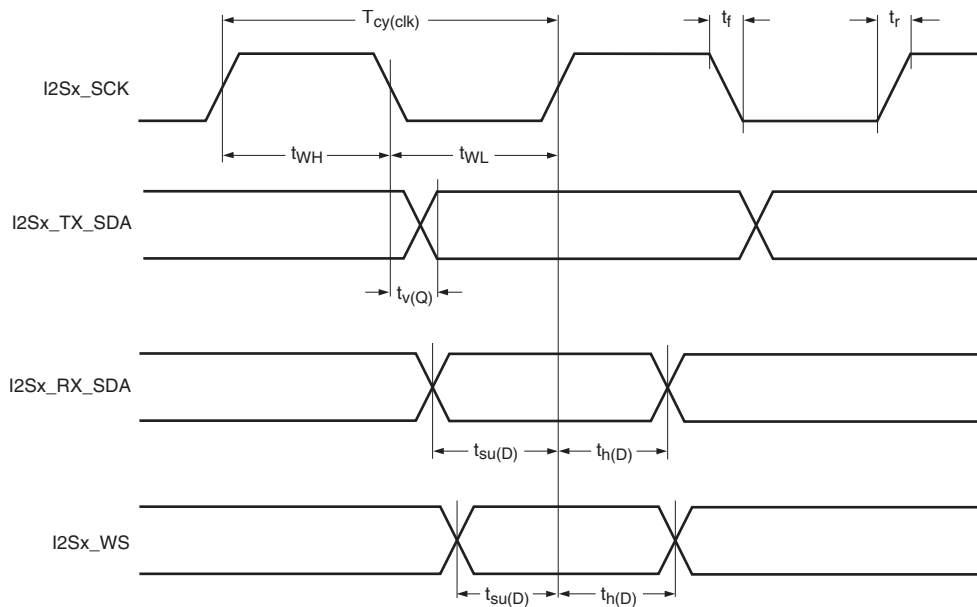


Figure 26. I²S-bus timing (slave)

1.7.4 SPI interfaces (Flexcomm interfaces 0-8)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (HCLK), and capacitive loading.

External memory interface

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 25 Mbit/s and the maximum supported bit rate for SPI slave mode (transmit/receive) is 25 Mbit/s.

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $1.71\text{ V} \leq V_{DD} \leq 1.89\text{ V}$; $C_L = 10\text{ pF}$ balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

Table 36. SPI interfaces¹

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI master						
t_{DS}	data set-up time	-	5.0	-	-	ns
t_{DH}	data hold time	-	0	-	-	ns
$t_{v(Q)}$	data output valid time	-	0	-	13.0	ns
SPI slave						
t_{DS}	data set-up time	-	5.0	-	-	ns
t_{DH}	data hold time	-	0	-	-	ns
$t_{v(Q)}$	data output valid time	-	0	-	13	ns

1. Based on simulation; not tested in production

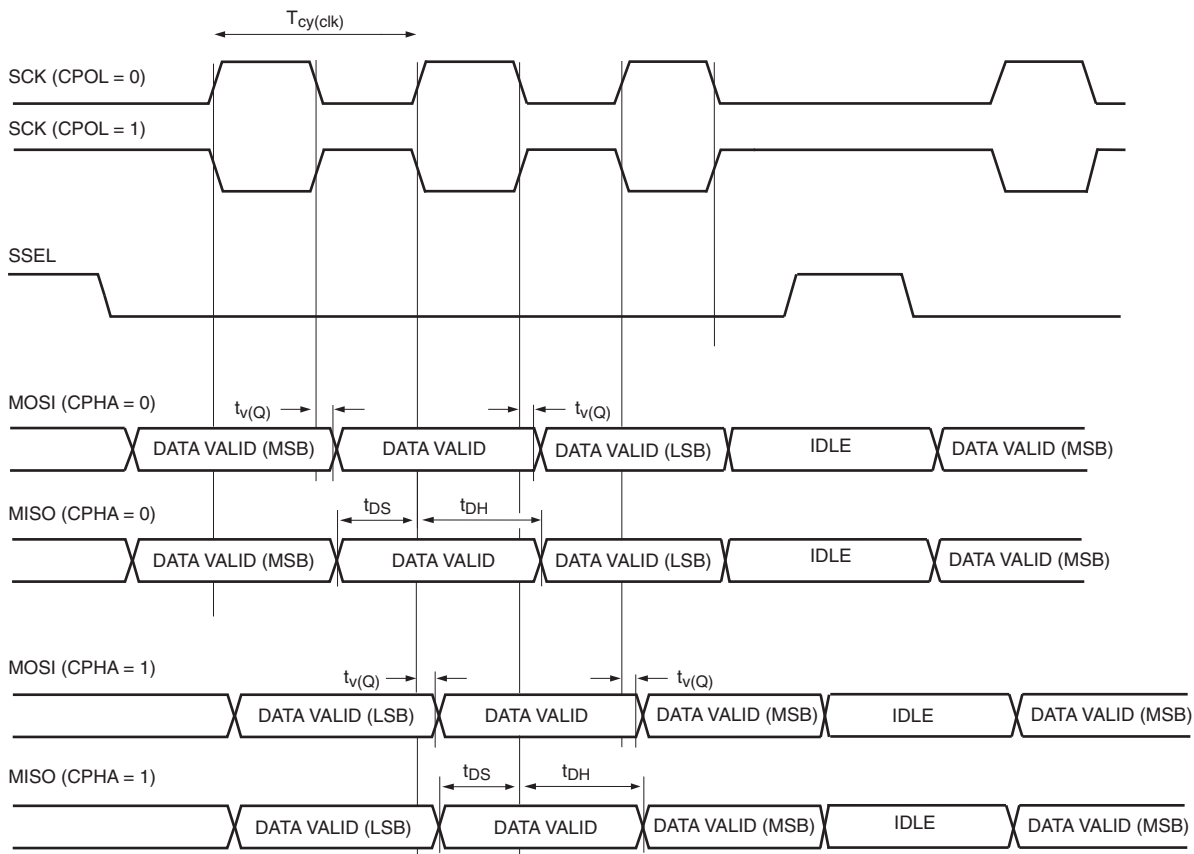


Figure 27. SPI master timing

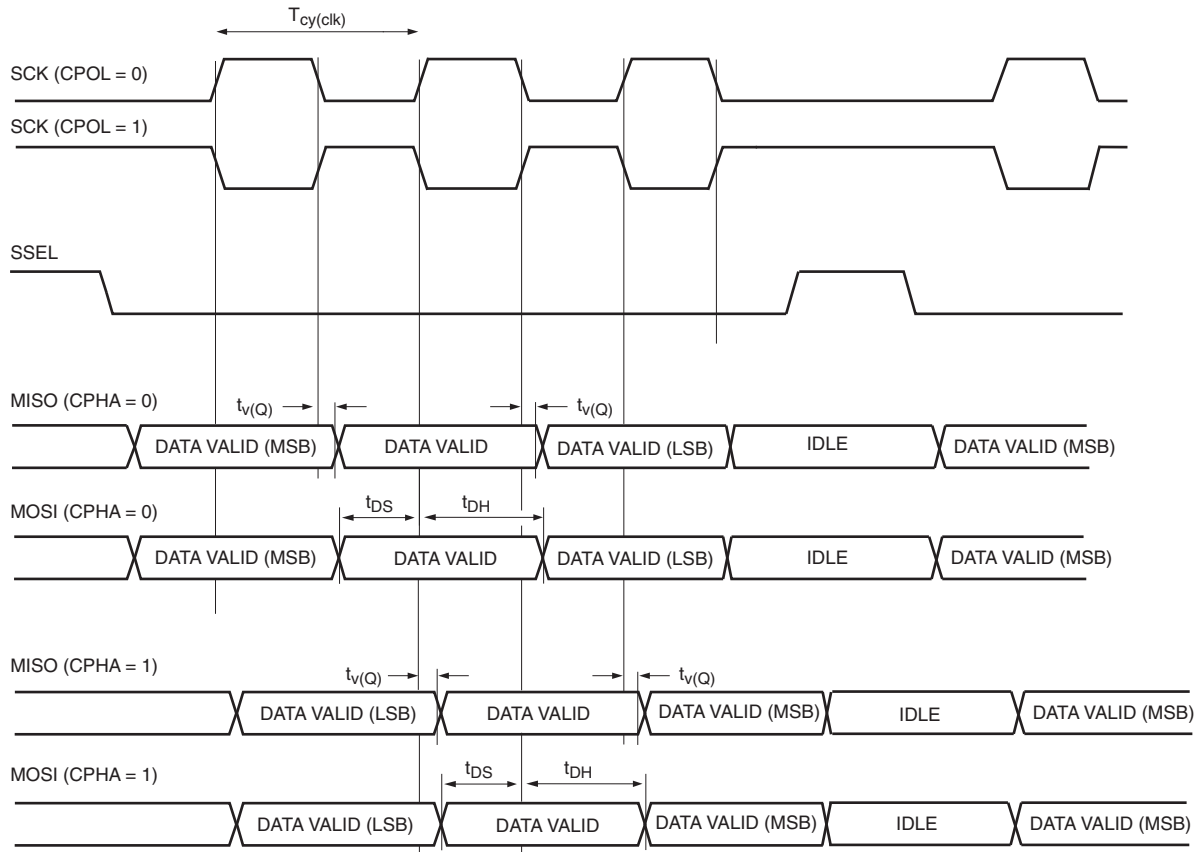


Figure 28. SPI slave timing

1.7.5 High-Speed SPI interface (Flexcomm interface 14)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (HCLK), and capacitive loading.

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 50 Mbit/s.

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI slave mode (receive) is 50 Mbit/s and for SPI slave mode (transmit) is 35 Mbit/s.

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $1.71\text{ V} \leq V_{DD} \leq 1.89\text{ V}$; $C_L = 10\text{ pF}$ balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

Table 37. High-Speed SPI interfaces¹

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI master						
t_{DS}	data set-up time	-	4.0	-	-	ns
t_{DH}	data hold time	-	0	-	-	ns
$t_{V(Q)}$	data output valid time	-	0	-	6.0	ns
SPI slave						
t_{DS}	data set-up time	-	3.0	-	-	ns
t_{DH}	data hold time	-	0	-	-	ns
$t_{V(Q)}$	data output valid time	-	0	-	10.0	ns

1. Based on simulation; not tested in production

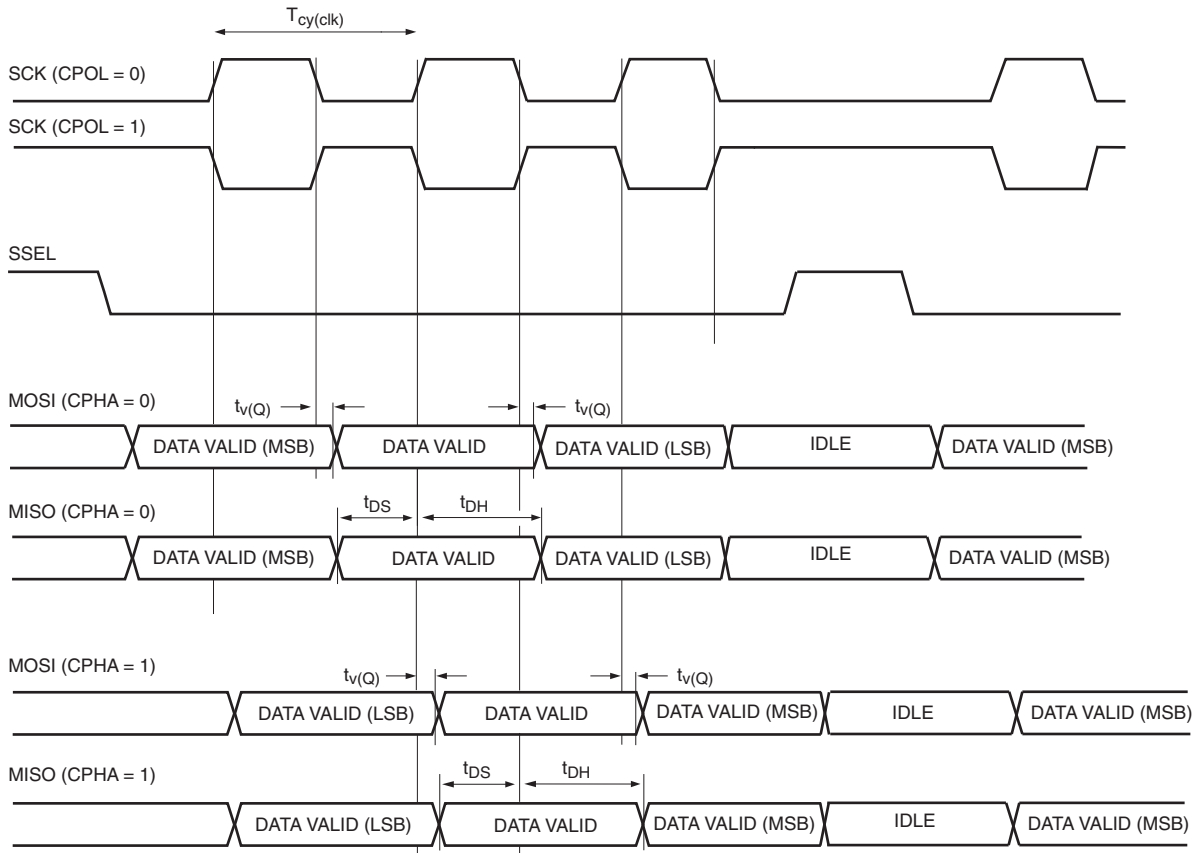


Figure 29. SPI master timing

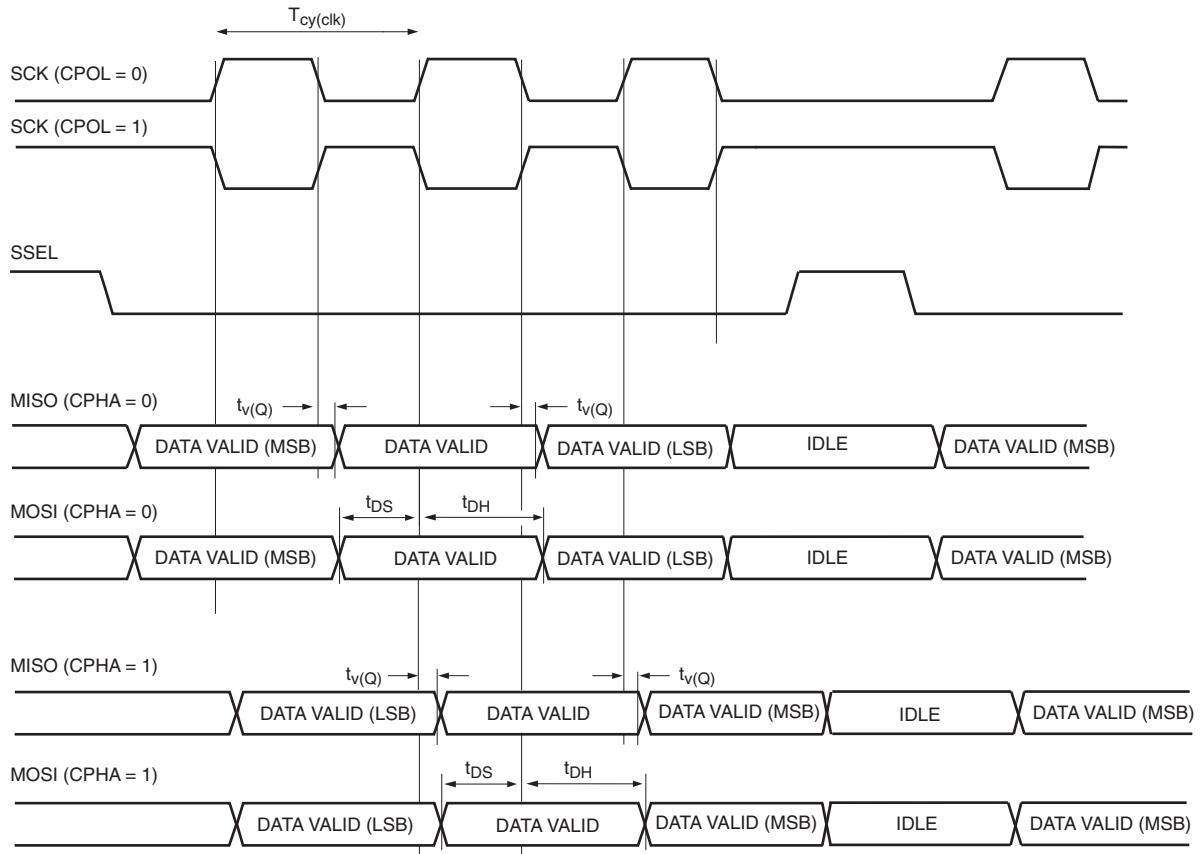


Figure 30. SPI slave timing

1.7.6 SD/MMC and SDIO

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $V_{DD} = 1.71\text{ V}$ to 1.89 V ; $V_{DDCORE} = 1.13\text{ V}$; $CL = 10\text{ pF}$. $DLL_CTRL = 0x200$, Full Drive Mode on all pins, Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production.

Table 38. SD/MMC and SDIO characteristics (Default Speed (DS), High Speed (HS) SDR-12 and SDR-25)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode. DS/ SDR-12 (12.5 MB/s)	-	-	12.5	MHz
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, HS/ SDR-25 (25 MB/s)	-	-	25	MHz

Table continues on the next page...

Table 38. SD/MMC and SDIO characteristics (Default Speed (DS), High Speed (HS) SDR-12 and SDR-25) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	7.5	-	-	ns
		on pins SD_CMD as inputs	7.5	-	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	1.0	-	-	ns
		on pins SD_CMD as inputs	1.0	-	-	ns
$t_{v(O)}$	data output valid time	on pins SD_DATn as outputs	-	-	7.5	ns
		on pins SD_CMD as outputs	-	-	7.5	ns

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $V_{DD} = 1.71\text{ V}$ to 1.89 V ; $V_{DDCORE} = 1.13\text{ V}$; $CL = 10\text{ pF}$. $DLL_CTRL = 0x200$, Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production.

Table 39. SD/MMC and SDIO characteristics ((SDR-50, SDR-104, HS-200 (MMC))

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, SDR-50 (50 MB/s)	-	-	100	MHz
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, SDR-104 (104 MB/s)	-	-	200	MHz
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, HS-200 (MMC) (200 MB/s)	-	-	200	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	7.5	-	-	ns
		on pins SD_CMD as inputs	7.5	-	-	ns

Table continues on the next page...

Table 39. SD/MMC and SDIO characteristics ((SDR-50, SDR-104, HS-200 (MMC)) (continued))

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0	-	-	ns
		on pins SD_CMD as inputs	0	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs	0	-	7.5	ns
		on pins SD_CMD as outputs	0	-	7.5	ns

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $V_{DD} = 1.71\text{ V}$ to 1.89 V ; $V_{DDCORE} = 1.13\text{ V}$; $CL = 10\text{ pF}$. $DLL_CTRL = 0x200$, Full Drive Mode on all pins, Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production. HS-400 supported on SD port 0 only.

Table 40. SD/MMC and SDIO characteristics ((DDR-50, HS DDR (MMC))

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, DDR-50 (50 MB/s)	-	-	50	MHz
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, HS-DDR (104 MB/s)			52	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	4.8	-	-	ns
		on pins SD_CMD as inputs	4.8	-	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0	-	-	ns
		on pins SD_CMD as inputs	0	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs	0	-	5.0	ns
		on pins SD_CMD as outputs	0	-	5.0	ns

External memory interface

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $V_{DD} = 1.71\text{ V}$ to 1.89 V ; $V_{DDCORE} = 1.13\text{ V}$; $CL = 10\text{ pF}$. $DLL_CTRL = 0x200$, Full Drive Mode on all pins, Input slew = 1 ns , SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production. HS-400 supported on SD port 0 only.

Table 41. SD/MMC and SDIO characteristics (HS-400(MMC))

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, HS-400 (400 MB/s)	-	-	200	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	0.5	-	-	ns
		on pins SD_CMD as inputs	0.5	-	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0	-	-	ns
		on pins SD_CMD as inputs	0	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs	0	-	1.0	ns
		on pins SD_CMD as outputs	0	-	1.0	ns

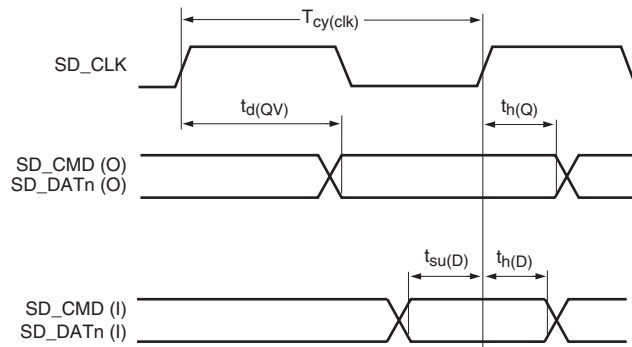


Figure 31. SD/MMC and SDIO timing

1.7.7 DMIC subsystem

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $V_{DD} = 2.7\text{ V}$ to 3.6 V ; $C_L = 20\text{ pF}$ balanced loading on all pins; Input slew = 1 ns , SLEW set to standard mode for all pins; Bypass bit = 0; Parameters sampled at the 50% level of the rising or falling edge.

Table 42. Dynamic characteristics¹

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{DS}	data set-up time	-	13	-	-	ns
t_{DH}	data hold time	-	0	-	-	ns

1. Based on simulated values.

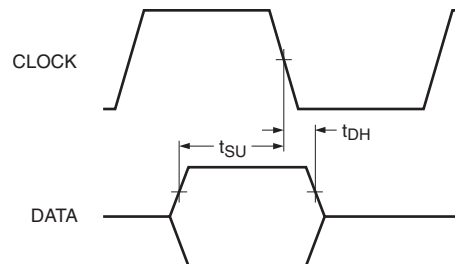


Figure 32. DMIC timing diagram

1.7.8 USB interface characteristics

This section describes the USB1 port High Speed/Full Speed (HS/FS) transceiver. The USB HS/FS meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification.

1.7.9 USB DCD electrical specifications

Table 43. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC} , V_{DM_SRC}	USB_DP and USB_DM source voltages (up to 250 μA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	μA
I_{DM_SINK} , I_{DP_SINK}	USB_DM and USB_DP sink currents	50	100	150	μA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	$\text{k}\Omega$
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

1.7.10 USB High Speed Transceiver and PHY specifications

This section describes the High Speed USB PHY parameters. The high speed PHY is capable of full speed signaling as well.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
 - Title: 5V Short Circuit Withstand Requirement Change
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
 - Title: Pull-up/Pull-down resistors
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
 - Title: Suspend Current Limit Changes
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
 - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
 - Revision 1.2, December 7, 2010

USB0_VBUS pin is a detector function which is 5v tolerant and complies with the above specifications without needing any external voltage division components.

1.7.11 Improved Inter-Integrated Circuit Interface (MIPI-I3C) specifications

Unless otherwise specified, MIPI-I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

Table 44. MIPI-I3C specifications when communicating with legacy I²C devices

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	0	0.4	0	1	MHz
t_{SU_STA}	Set-up time for a repeated START condition	600	—	260	—	ns
Hold time (repeated)	t_{HD} ; STA	600	—	260	—	ns

Table continues on the next page...

Table 44. MIPI-I3C specifications when communicating with legacy I²C devices (continued)

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
START condition						
t _{LOW}	LOW period of the SCL clock	1300	—	500	—	ns
t _{HIGH}	HIGH period of the SCL clock	600	—	260	—	ns
t _{SU_DAT}	Data set-up time	100	—	50	—	ns
t _{HD_DAT}	Data hold time for I ² C bus devices	—	—	—	—	ns
t _f	Fall time of SDA and SCL signals	20*(V _{dd} /5.5 v)	300	20*(V _{dd} /5.5 v)	120	ns
t _r	Rise time of SDA and SCL signals	20	300	—	120	ns
t _{SU_STO}	Set-up time for STOP condition	600	—	260	—	ns
t _{BUF}	Bus free time between STOP and START condition	1.3	—	0.5	—	μs
t _{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns

Table 45. MIPI-I3C open drain mode specifications

Symbol	Characteristic	Min.	Max.	Unit	Notes
t _{LOW_OD}	LOW period of the SCL clock	200	—	ns	
t _{DIG_OD_L}	t _{LOW_OD} + t _{rDA_OD} (min)	—	ns		
t _{HIGH}	HIGH period of the SCL clock	—	41	ns	
t _{rDA_OD}	Fall time of SDA signal	t _{CF}	12	ns	1
t _{SU_OD}	Data set-up time during open drain mode	3	—	ns	
t _{CAS}	Clock after START (S) Condition <ul style="list-style-type: none"> • ENTAS0 • ENTAS1 • ENTAS2 • ENTAS3 	38.4 n	1 μ 100 μ 2 m 50 m	s s s s	
t _{CBP}	Clock before STOP (P) condition	t _{CAS} (min)/2	—	ns	
t _{MMO} Overlap	Current master to secondary master overlap time during handoff	t _{DIG_OD_L}	—	ns	
t _{AVAL}	Bus available condition	1	—	μs	
t _{IDLE}	Bus idle condition	1	—	ms	
t _{MMLock}	Time interval where new master not driving SDA low	t _{AVAL}	—	μs	

1. C_b = total capacitance of the one bus line in pF.

Table 46. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{SCL}	SCL Clock Frequency	0.01	12.5	13	MHz	
t_{LOW}	LOW period of the SCL clock	24	—	—	ns	
t_{DIG_L}		32	—	—	ns	
t_{HIGH_MIXED}	HIGH period of the SCL clock for a mixed bus	24	—	—	ns	
$t_{DIG_H_MIXED}$		32	—	45	ns	1
t_{HIGH}	HIGH period of the SCL clock	24	—	—	ns	
t_{DIG_H}		32	—	—	ns	
t_{SCO}	Clock in to data out for a slave	—	—	12	ns	
t_{CR}	SCL clock rise time	—	—	$150 * 1 / f_{SCL}$ (capped at 60)	ns	
t_{CF}	SCL clock fall time	—	—	$150 * 1 / f_{SCL}$ (capped at 60)	ns	
t_{HD_PP}	SDA signal data hold • Master mode • Slave mode	$t_{CR}+3$ and $t_{CF}+3$ 0	— —	— —	ns	
t_{SU_PP}	SDA signal setup	3	—	—	ns	
t_{CASr}	Clock after repeated START (Sr)	t_{CAS} (min)	—	—	ns	
t_{CBSr}	Clock before repeated START (Sr)	t_{CAS} (min)/2	—	—	ns	
C_b	Capacitive load per bus line	—	—	50	pF	

1. When communicating with an I3C Device on a mixed Bus, the $t_{DIG_H_MIXED}$ period must be constrained in order to make sure that I²C devices do not interpret I3C signaling as valid I²C signaling.

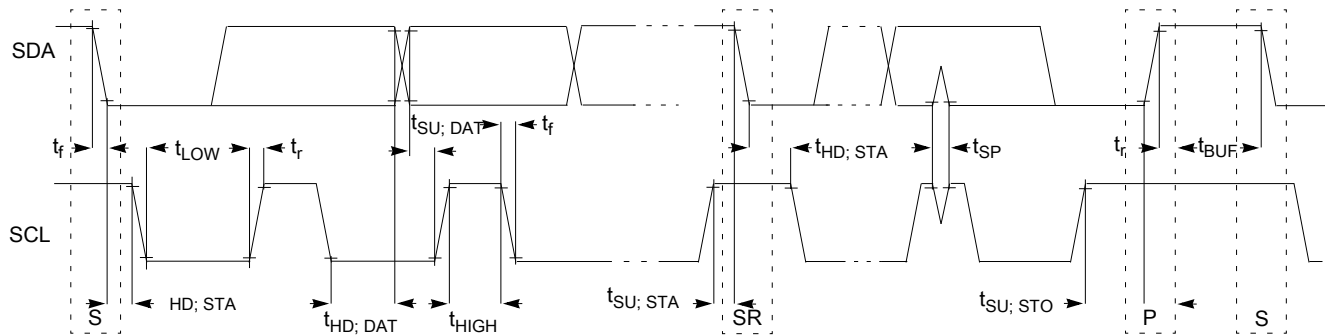


Figure 33. Timing definition for devices on the I²C bus

1.8 Timer modules

1.8.1 SCTimer/PWM output timing

$T_{amb} = -20\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; $1.71\text{ V} \leq V_{DD} \leq 1.89\text{ V}$ $C_L = 20\text{ pF}$. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 50% level of the rising or falling edge; values guaranteed by design.

Table 47. SCTimer/PWM output dynamic characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{sk(o)}$	output skew time	-	0	-	2.8	ns

2 Architectural overview

The Arm Cortex-M33 includes two AHB-Lite buses: the code bus and the system bus.

The i.MX RT500 uses a multi-layer AHB matrix to connect the Arm Cortex-M33 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

2.1 Detailed block diagram

The following figure shows the detailed block diagram for i. MX RT500

Architectural overview

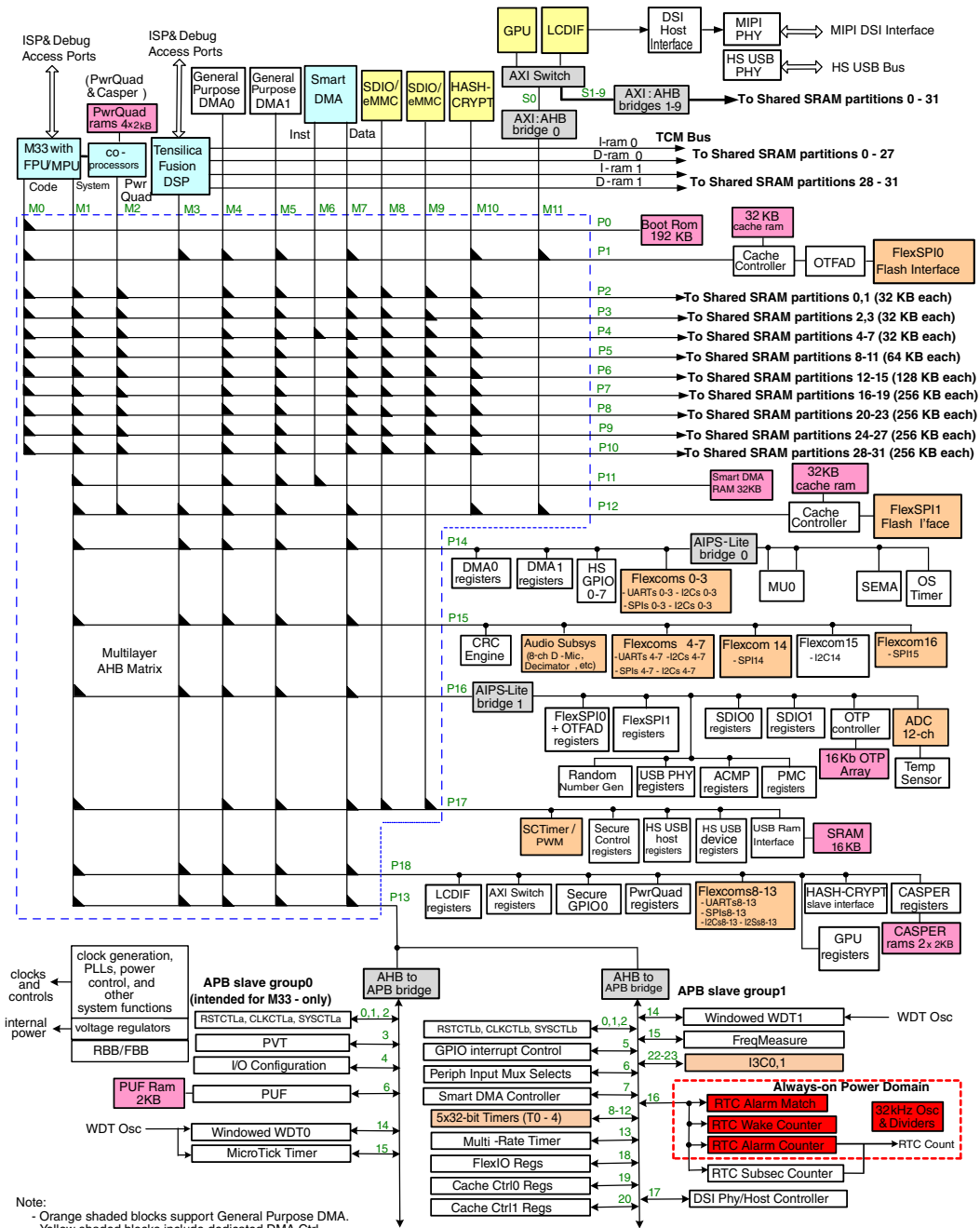


Figure 34. i.MX RT500 detailed block diagram

2.2 Shared system SRAM

The entire system TCM SRAM space (accessed in single cycle) of up to 5 MB is divided into up to 32 separate partitions, which are accessible to both CPUs, both DMA engines, and all other AHB bus masters. The Fusion CPU TCMI (Instruction) & TCMD

(Data) interfaces and the Graphics (GPU/LCD) subsystem each access the RAM via separate, dedicated 64-bit interfaces. All other masters, including the Cortex-M33 processor and the DMA engines, access RAM via the main 32-bit AHB bus. All of these accesses are single-cycle with the exception of the GPU/LCD. Hardware interface modules arbitrate access to each RAM partition between the main AHB bus, the graphics AHB bus and the Fusion Tightly-Coupled-Memory buses.

Under software control, each of the 32 individual SRAM partitions can be used exclusively as code or as data, dedicated either CPU, or shared among the various masters. Each partition can be independently placed in a low-power retention mode or powered off entirely.

2.3 RT500 modules list

The i.MX RT500 contains a variety of digital and analog modules. The following table describes briefly about these modules.

Table 48. i.MX RT500 modules list

Block Name	Block Mnemonic	Subsystem	Brief description
Arm core modules			
ARM Cortex M33 processor	MCU	Core module	The Arm Cortex-M33 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The Arm Cortex-M33 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses. M33 includes ARM's TrustZone M for enhanced security as well as a co-processor interface. This interface is used on this device to provide hardware acceleration for DSP functions (Powerquad co-processor) and Security/cryptography operations (CASPER co-processor). A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its

Table continues on the next page...

Table 48. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			successor is being decoded, and a third instruction is being fetched from memory.
Arm Cortex-M33 integrated Floating Point Unit (FPU)	FPU	Core modules	The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions. The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.
Memory Protection Unit	MPU	Core module	The Cortex-M33 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application. The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system. The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.
Nested Vectored Interrupt Controller (NVIC) for Cortex-M33	NVIC	Core modules	The NVIC is an integral part of the Cortex-M33. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.
System Tick timer (SysTick)	SysTick	Core modules	The Arm Cortex-M33 includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the FRO or the Cortex-M33 core clock.
Memories			
On-Chip static RAM	SRAM	Memories	The i.MX RT500 supports up to 5 MB SRAM with separate bus master access

Table continues on the next page...

Table 48. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			for higher throughput and individual power control for low-power operation.
On-chip ROM	ROM	Memories	The 192 KB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API): <ul style="list-style-type: none"> • In-Application Programming (IAP) and In-System Programming (ISP). • ROM-based USB drivers (HID, CDC, MSC). Supports flash updates via USB. • Supports booting from valid Octal/Quad SPI, eMMC, USB, USART, SPI, and I2C. • Legacy, Single, and Dual image boot. • OTP API for programming OTP memory. • Random Number Generator (RNG) API.
One-Time Programmable memory	OTP	Memories	The i.MX RT500 contains up to 16 kbits one-time-programmable memory used for part configuration, key storage (as an alternative to PUF) and other uses.
Clock sources			
192 MHz Free Running Oscillator (FRO)	FRO	System control	The 192 MHz FRO oscillator provides a high-frequency clock source that can be used without the need for a high-power PLL for many applications. This oscillator is factory trimmed to $\pm 1\%$ accuracy but can optionally be tuned to $\pm 0.1\%$ accuracy using an accurate, known reference clock such as the crystal oscillator. The 192 MHz FRO, or a divided version of it, may be used as the main system clock and for many other purposes.
1 MHz Low Power Oscillator	LPO	System Control	The 1 MHz oscillator provides an ultra low-power, low-frequency clock source that can be used to clock a variety of functions including the Watchdog Timer (WWDT) and the OS/EVENT Timer. It can also be used as the main system clock for low-power operation. On Reset, the device boots using this 1 MHz oscillator. The 1 MHz Low Power oscillator is accurate to $\pm 5\%$ over temperature.
Crystal Oscillator	-	System Control	The main crystal oscillator on the i.MX RT500 can be used with crystal frequencies from 4 MHz to 26 MHz. The

Table continues on the next page...

Table 48. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			crystal oscillator may be used to drive a PLL to achieve higher clock rates.
32 KHz Crystal Oscillator	-	System Control	The 32KHz oscillator resides in the "always-on" domain and is used to drive the Real Time Clock. It is also available for use for a variety of other purposes including low-power UART operation or as the main system clock for very low frequency operation
System Control (PLLs)			
System PLL (PLL0)	PLL0	System Control	The system PLL accepts an input clock frequency in the range of 32.768 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). Generates four independent outputs (PFD0-3).
Audio PLL (PLL1)	PLL1	System Control	The audio PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The PLL can be enabled or disabled by software.
I/O Muxing			
General Purpose I/O (GPIO)	GPIO	Pin Muxing	The i.MX RT500 provides up to six GPIO ports with a total of up to 136 GPIO pins. Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin. It can optionally contribute to one of two GPIO group interrupts, with selection of polarity, level or edge detection.
Pin Interrupt and Pattern Match (PINT)	-	I/O Mux	The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can optionally be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or

Table continues on the next page...

Table 48. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			pattern match engine are located on the I/O+ bus for fast single-cycle access.
Communication peripherals			
High-speed USB Host/ Device interface (USB1)	USB1	Communication interfaces	The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The device controller enables 480 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.
Flex SPI Controller (FlexSPI)	FlexSPI	Communication interfaces	Two FlexSPI Interface modules, supporting Octal and Quad SPI memory devices are provided. The first FlexSPI instance is primarily intended for code execution from off-chip SPI flash memory. The second instance is primarily intended to access data from RAMs like HyperRAM or pSRAM (particularly for graphics). The second instance is accessible by the DSP processor as well as the M33. Target will be for both interfaces to support up to 200 MHz DDR/SDR The FlexSPI interfaces support HyperFlash, HyperRAM and Xccela memory types, among others. The first FlexSPI interface (FlexSPI0) supports execute-in-place and on-the-fly decryption using the latest OTFAD module. It also provides a mechanism to shift a designated range of addresses to a different region of off-chip memory to support dual-image boot. Both FlexSPI Interfaces include a 32 KB cache with an CACHE64 AHB-cache controller. Additional logic is provided at the CACHE64 interface to enable different caching policies for different address regions. These policies include: <ul style="list-style-type: none"> • Write-back • Write-through • Non-cached

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Table 48. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
SD/eMMC interfaces	uSDHC	Communication interfaces	Two uSDHC SDIO/MMC card interfaces are provided. One instance of this interface (SDIO0) supports the eMMC 5.0 standard including HS400 DDR mode. The other instance supports 100 MHz SDR, 50 MHz DDR.
Flexcomm Interface	FlexComm	Communication interfaces	Following are the features of FlexComm: <ul style="list-style-type: none"> • USART with asynchronous operation or synchronous master or slave operation. • SPI master or slave, with up to 4 slave selects. • I2C, including separate master, slave, and monitor functions. • Two I2S functions using Flexcomm Interface 6 and Flexcomm Interface 7. • Data for USART, SPI, and I2S traffic uses the Flexcomm Interface FIFO. The I2C function does not use the FIFO.
I3C interface	I3C	Communication interface	Two I3C master/slave interfaces are provided, both of which support DDR.
Counter/Timer modules			
General-purpose 32-bit timers/external event counter	-	Counter/Timers	The i.MX RT500 includes five general-purpose 32-bit timer/counters. The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.
SCTimer/PWM	SCT/PWM	Counters/Timers	The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers. The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

Table continues on the next page...

Table 48. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			<ul style="list-style-type: none"> • State variable • Limit, halt, stop, and start conditions. • Values of Match/Capture registers, plus reload or capture control values. <p>In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:</p> <ul style="list-style-type: none"> • Clock selection • Inputs • Events • Outputs • Interrupts
Windowed Watchdog Timer (WWDT)	WWDT	Timers	The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window. A separate Watchdog Timer is provided for each of the two CPUs.
Real Time Clock Timer	RTC Timer	Timers	The RTC timer is a 32-bit timer which counts down from a preset value to zero. At zero, the preset value is reloaded and the counter continues. The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock.
Multi-Rate Timer	MRT	Timers	The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.
OS/Event Timer	-	Timers	An OS/EVENT Timer module provides a common timebase between the two CPUs for event synchronization and timestamping. The OS/EVENT Timer is comprised of a shared, free-running counter readable by each CPU and individual match and capture registers for each CPU. The shared and local counters in this module are implemented using Gray code. This will enable them to be read asynchronously by the processing domains. The main counter in the OS/EVENT Timer module begins counting immediately following power-up and continues counting through any subsequent system resets (except those caused by a new POR).

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Table 48. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
Micro-Tick Timer	MTR	Timers	A 32-bit MicroTick timer that runs from the 1 MHz low-power oscillator. This timer can wake up the device from reduced power modes up to deep-sleep, with extremely low power consumption. The MicroTick timer has an added timestamp feature in the form of 4 capture registers.
Graphics Peripherals			
2D Graphics Processing Unit (GPU)	GPU2D	Graphics	A 2D graphics engine is provided. The GPU is used to generate graphics data for display by the LCD Display Controller. The GPU supports displays up to 640x480.
MIPI DSI Controller with on-chip PHY	MIPI-DSI	Graphics	LCD Display Controller, with on-chip MIPI DSI Phy provides transfer rates up to 895.1 Mbps to support 1024x480 displays with 24-bit color at 60 frames per second. A parallel DBI interface is also provided (alternative to the serial PHY).
Flexio	FlexIO	Graphics/Multimedia	The Flexio module under "Others" category can be used to interface to an LCD with a parallel interface.
Other Digital Peripherals			
DMA Controller	DMA	Other	The DMA controller allows peripheral-to-memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination. Two identical DMA controllers are provided on i.MX RT500. The user may elect to dedicate one of these to the Cortex M-33 CPU and the other for use by the DSP CPU and/or one may be used as a secure DMA the other non-secure.
DMIC Subsystem	DMIC	Other	DMIC subsystem includes: <ul style="list-style-type: none"> • Pulse-Density Modulation (PDM) data input for left and/or right channels on 1 or 2 buses. • Flexible decimation. • 16 entry FIFO for each channel. • DC blocking or unaltered DC bias can be selected. • Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then

Table continues on the next page...

Table 48. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			<p>automatically returning to deep-sleep mode.</p> <ul style="list-style-type: none"> Data can be streamed directly to I2S on Flexcomm Interface 7.
Smart DMA Engine	Smart DMA Controller	Other	Smart DMA Controller with dedicated 32 KB code RAM
Flexible Input/Output	FlexIO	Others	The Flexible Input/Output (FlexIO) module is capable of supporting a wide range of protocols including, but not limited to: UART, I2C, SPI, I2S, camera interface, display interface, PWM waveform generation, and so on
Cyclic Redundancy Check(CRC) engine	CRC	Other	The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.
Analog Peripherals			
12-bit Analog to Digital Converter	ADC	Analog	The ADC supports a resolution of 12-bit and fast conversion rates of up to 1 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the Arm TXEV interrupt.
Temperature Sensor	-	Analog	<p>The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ± 5 °C over the full temperature range (-20 °C to +70 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines. After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input. For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.</p>

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Table 48. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
Analog Comparator	CMP	Analog	The Comparator (CMP) module provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail to rail operation).
Security			
Security Subsystem	-	Security	Comprises of: <ul style="list-style-type: none"> • Trust Zone M • AES256 Decryption Engine. • SHA-1, SHA-2 HASH Engine. • Physical Unclonable Function (PUF) Key Generation • CASPAR security Cortex-M33 co-processor • OTP memory • Random number generator (RNG) • On-the-Fly Decryption on FlexSPI interface
On-The-Fly AES Decryption	OTFAD	Security	The On-The-Fly AES Decryption (OTFAD) module provides an advanced hardware implementation that minimizes any incremental cycles of latency introduced by the decryption in the overall external memory access time. The OTFAD engine also includes complete hardware support for a standard AES key unwrap mechanism to decrypt a key BLOB data instruction containing the parameters needed for up to 4 unique AES contexts.
True Random Number Generator	TRNG	Security	The True Random Number Generator (TRNG) module is used to generate high quality, cryptographically secure, random data. The TRNG module is capable of generating its own entropy using an integrated ring oscillator.

3 Application information

3.1 Current consumption vs. memory partitions

The following figure shows the current consumption vs memory partitions:

M33 active, running enhanced-while(1) code in different partitions.

Typical silicon, VDDCore=1.1V, Temperature=25°C, FBB, HCLK=192MHz (FRO).

All memories array/periphery ON (PDRUNCFG2/3) and only one partition clocked (AHB_SRAM_ACCESS_DISABLE register).

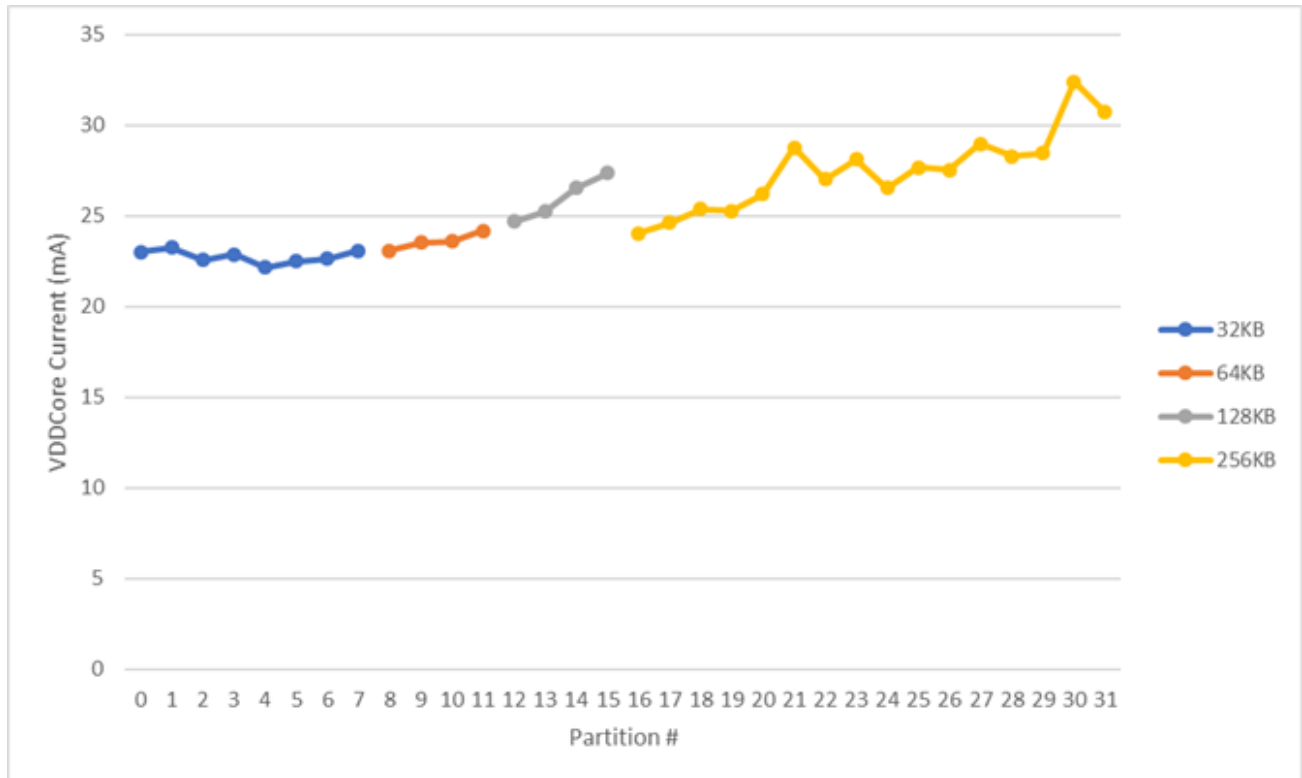


Figure 35. Current consumption vs. memory partitions

3.2 Standard I/O pin configuration

The following figure shows the possible pin modes for standard I/O pins:

The default configuration for standard I/O pins is Z mode. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

Application information

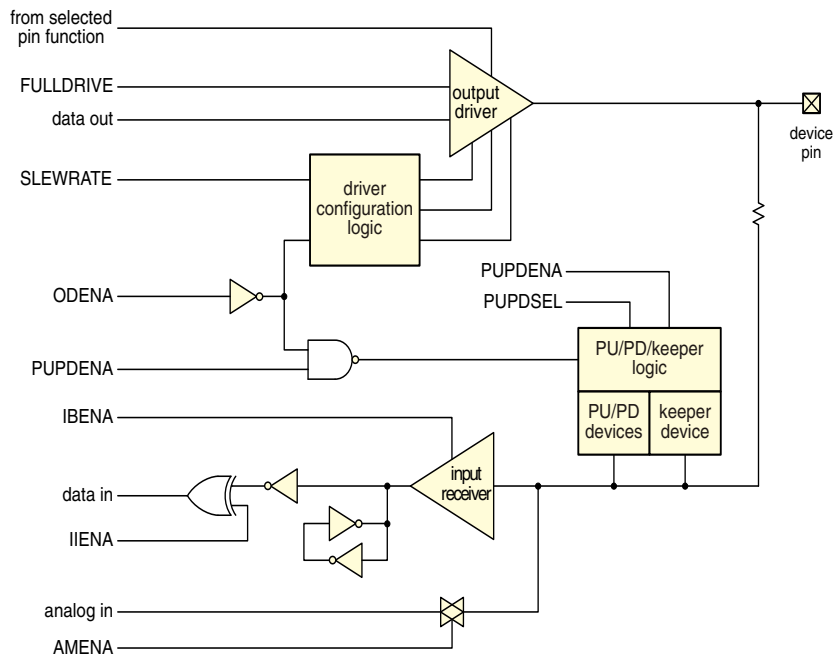


Figure 36. Pin configuration

3.3 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in [Table 6](#) for a given input voltage V_I . For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in [Table 6](#), but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see [Table 6](#) for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

3.4 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on RTCXIN and RTCXOUT. See the following figure.

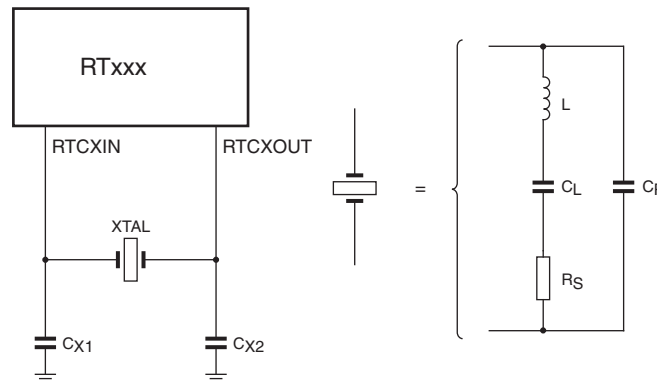


Figure 37. RTC oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (C_L), series resistance (R_S), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - C_{\text{Pad}} - 2C_{\text{STRAY}}$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF, for each pad).

C_{STRAY} - stray capacitance between RTCXIN and RTCXOUT pins.

For example:

$$C_L = 9 \text{ pF}$$

$$C_{X1} = C_{X2} = 2C_L - C_{\text{Pad}} - 2C_{\text{STRAY}}$$

$$C_{X1} = C_{X2} = 2 \cdot 9 - 3 - 0 = 15 \text{ pF}$$

Although C_{STRAY} can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors.

Therefore, it is recommended to fine tune the values of external load capacitors on

actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to the CLOCKOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

To use bypass mode on RTC, remove the crystal, drive an external clock to RTCIN pin, and float the RTCOUT pin.

3.4.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

3.5 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_X and C_Y need to be connected externally on XTALIN and XTALOUT. See the figure below.

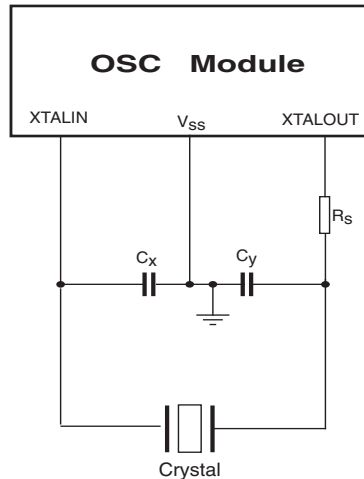


Figure 38. XTAL oscillator connection - Low-Power Mode

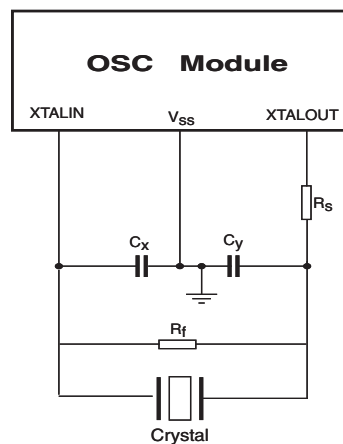


Figure 39. XTAL oscillator connection - High Gain Mode

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_x = C_y = 2C_L - C_{\text{Pad}} - 2C_{\text{STRAY}}$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF, for each pad).

C_{STRAY} – stray capacitance between XTALIN and XTALOUT pins.

For example:

Application information

$$C_L = 9 \text{ pF}$$

$$C_x = C_y = 2C_L - C_{\text{Pad}} - 2C_{\text{STRAY}}$$

$$C_x = C_y = 2 \cdot 9 - 3 - 0 = 15 \text{ pF}$$

Although C_{STRAY} can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors.

Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

To use bypass mode on system oscillator, set bit 1 to "1" in the system oscillator control 0 (CLKCTL0_SYSOSCCTL0), float the XTALIN pin, and drive XTALOUT with < 0.7 V to 1.8 V.

For oscillator high gain mode, a larger voltage swing is used at the crystal pin. This gives a higher noise immunity within the oscillator and less edge to edge jitter of the internal clock. When high gain mode is not required, power used by the crystal oscillator can be reduced by using low power mode.

NOTE

High gain mode requires a 1 megaohm resistor (RF) to be inserted.

3.5.1 XTAL Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors C_X , C_Y , and C_{X3} , in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

3.5.2 Thermally compensated crystal oscillator (TCXO)

In the TXCO circuit, only the oscillator should be connected to the XTALIN pin while the XTALOUT pin remains floating when driving the device with a TXCO. See the following figure.

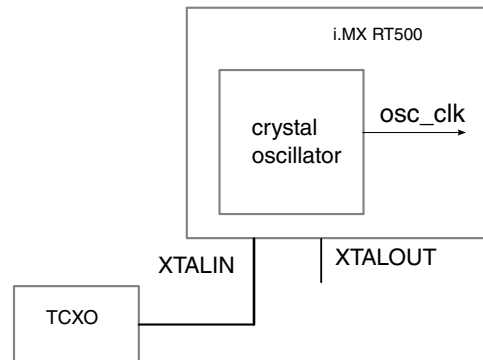


Figure 40. Thermally compensated crystal oscillator

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Vmax	Maximum XTAL input voltage	-	-	-	VDD1V8	V
Vpp min	Min voltage for XTALIN		500	-	-	mV
VPP nom	Voltage where Jitter in = jitter out		800	-	-	mV
CXTALIN	XTALIN input Impedance		-	5	-	pF
Fmax	Maximum input frequency	-	-	-	32	MHz

3.6 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see [Figure 41](#)) or bus-powered device (see [Figure 42](#)).

On the i.MX RT500, the USB_VBUS pin is 5 V tolerant pin regardless of whether USB1_VDD3V3 or VDD pins are present or not.

Application information

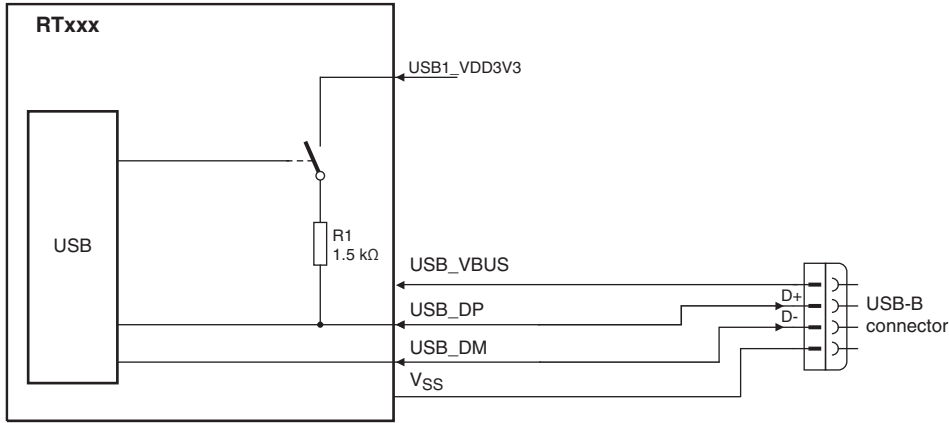


Figure 41. USB interface on a self-powered device where USB_VBUS = 5 V

The internal pull-up (1.5 kΩ) can be enabled by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required.

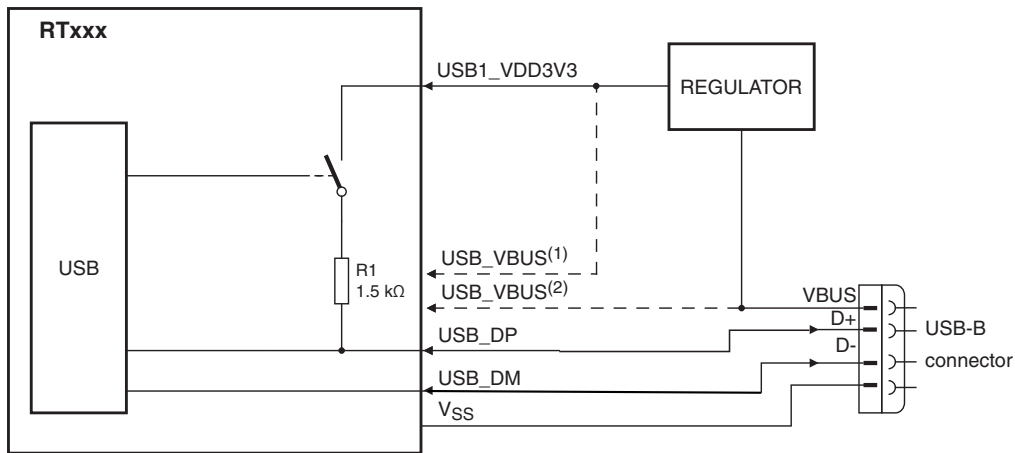


Figure 42. USB interface on a bus-powered device

In the figure above, two options exist for connecting VBUS to the USB_VBUS pin:

1. Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.
2. Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply USB1_VDD3V3

4 Abbreviations

Table 49. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
FRO oscillator	Internal Free-Running Oscillator, tuned to the factory specified frequency
GPIO	General Purpose Input/Output
FRO	Free Running Oscillator
LSB	Least Significant Bit
MCU	MicroController Unit
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

5 Pinouts

5.1 Signal multiplexing and pinouts

The table below shows the pin functions available on each pin, and for each package. These functions are selectable using IOCON control registers.

Some functions, such as ADC or comparator inputs, are available only on specific pins when digital functions are disabled on those pins. By default, the GPIO function is selected except on pins PIO2_25 and PIO2_26, which are the serial wire debug pins. This allows debug to operate through reset.

Most pins have all pull-ups, pull-downs, and inputs turned off at reset. This prevents power loss through pins prior to software configuration. Due to special pin functions, some pins have a different reset configuration: If the Boot ROM OTP is configured to

Pinouts

use the ISP Select pins at boot, then these pins PIO1_15, PIO3_28, and PIO3_29 have pull-ups enabled by ROM; otherwise these pull-ups are not enabled at boot. The SWD pins PIO2_25 and PIO2_26 have the input buffers enabled at reset.

The state of pins PIO1_15, PIO3_28, and PIO3_29 at Reset determine the boot source for the part (if configured in the Boot ROM OTP) or if the ISP handler is invoked.

The JTAG functions TRST, TCK, TMS, TDI, and TDO, are selected on pins PIO0_7 to PIO0_11 by hardware when the part is in boundary scan mode.

5.2 i.MXRT500 Pinouts: 249 FOWLP package

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
F14	PIO0_0	PIO0_0	PIO0_0	FC0_SCK			CTIMER0_ MAT0	I2S_BRID GE_CLK_I N	GPIO_INT _BMAT		SEC_PIO0 _0	
G16	PIO0_1	PIO0_1	PIO0_1	FC0_TXD_ SCL_MIS O_WS			CTIMER0_ MAT1	I2S_BRID GE_WS_I N			SEC_PIO0 _1	
H16	PIO0_2	PIO0_2	PIO0_2	FC0_RXD_ _SDA_MO SI_DATA			CTIMER0_ MAT2	I2S_BRID GE_DATA _IN			SEC_PIO0 _2	
H15	PIO0_3	PIO0_3	PIO0_3	FC0_CTS_ SDA_SSE L0			CTIMER0_ MAT3	FC1_SSEL 2			SEC_PIO0 _3	
H14	PIO0_4	PIO0_4	PIO0_4	FC0_RTS_ SCL_SSE L1			CTIMER_I NP0	FC1_SSEL 3		CMP0_OU T	SEC_PIO0 _4	
F16	PIO0_5 / ADC0_0	PIO0_5	PIO0_5	FC0_SSEL 2	SCT0_GPI 0	SCT0_OU T0	CTIMER_I NP1				SEC_PIO0 _5	
F17	PIO0_6 / ADC0_8	PIO0_6	PIO0_6	FC0_SSEL 3	SCT0_GPI 1	SCT0_OU T1	CTIMER0_ MAT0				SEC_PIO0 _6	
J15	PIO0_7 / TRST	PIO0_7	PIO0_7	FC1_SCK	SCT0_GPI 4	SCT0_OU T4	CTIMER1_ MAT0	I2S_BRID GE_CLK_ OUT			SEC_PIO0 _7	
H12	PIO0_8 / TCK	PIO0_8	PIO0_8	FC1_TXD_ SCL_MIS O_WS	SCT0_GPI 5	SCT0_OU T5	CTIMER1_ MAT1	I2S_BRID GE_WS_O UT			SEC_PIO0 _8	
H17	PIO0_9 / TMS	PIO0_9	PIO0_9	FC1_RXD_ _SDA_MO SI_DATA	SCT0_GPI 6	SCT0_OU T6	CTIMER1_ MAT2	I2S_BRID GE_DATA _OUT			SEC_PIO0 _9	
K16	PIO0_10 / TDI	PIO0_10	PIO0_10	FC1_CTS_ SDA_SSE L0	SCT0_GPI 7	SCT0_OU T7	CTIMER1_ MAT3	FC0_SSEL 2			SEC_PIO0 _10	
K15	PIO0_11 / TDO	PIO0_11	PIO0_11	FC1_RTS_ SCL_SSE L1	SCT0_GPI 0	SCT0_OU T8	CTIMER_I NP2	FC0_SSEL 3			SEC_PIO0 _11	

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
E14	PIO0_12 / ADC0_1	PIO0_12	PIO0_12	FC1_SSEL2	SCT0_GPI2	SCT0_OUT2	CTIMER1NP3				SEC_PIO0_12	
F15	PIO0_13 / ADC0_9	PIO0_13	PIO0_13	FC1_SSEL3	SCT0_GPI3	SCT0_OUT3	CTIMER0MAT1				SEC_PIO0_13	
B12	PIO0_14	PIO0_14	PIO0_14	FC2_SCK	SCT0_GPI0	SCT0_OUT0	CTIMER2MAT0	I2S_BRIDGE_CLK_IN			SEC_PIO0_14	
B15	PIO0_15	PIO0_15	PIO0_15	FC2_TXD_SCL_MISO_WS	SCT0_GPI1	SCT0_OUT1	CTIMER2MAT1	I2S_BRIDGE_WS_IN			SEC_PIO0_15	
A16	PIO0_16	PIO0_16	PIO0_16	FC2_RXD_SDA_MOSI_DATA	SCT0_GPI2	SCT0_OUT2	CTIMER2MAT2	I2S_BRIDGE_DATA_IN			SEC_PIO0_16	
B17	PIO0_17	PIO0_17	PIO0_17	FC2_CTS_SDA_SSEL0	SCT0_GPI3	SCT0_OUT3	CTIMER2MAT3	FC5_SSEL2			SEC_PIO0_17	
B16	PIO0_18	PIO0_18	PIO0_18	FC2_RTS_SCL_SSEL1	SCT0_GPI6	SCT0_OUT6	CTIMER1NP4	FC5_SSEL3			SEC_PIO0_18	
F13	PIO0_19 / ADC0_2	PIO0_19	PIO0_19	FC2_SSEL2	SCT0_GPI4	SCT0_OUT4	CTIMER1NP5	UTICK_CAP0			SEC_PIO0_19	
A14	PIO0_21	PIO0_21	PIO0_21	FC3_SCK	SCT0_GPI5	SCT0_OUT5	CTIMER3MAT0	CTIMER1NP11	TRACECLK		SEC_PIO0_21	
B14	PIO0_22	PIO0_22	PIO0_22	FC3_TXD_SCL_MISO_WS	SCT0_GPI6	SCT0_OUT6	CTIMER3MAT1	CTIMER1NP7	TRACEDATA[0]		SEC_PIO0_22	
C13	PIO0_23	PIO0_23	PIO0_23	FC3_RXD_SDA_MOSI_DATA	SCT0_GPI7	SCT0_OUT8	CTIMER3MAT2	CTIMER0MAT3	TRACEDATA[1]		SEC_PIO0_23	
D13	PIO0_24	PIO0_24	PIO0_24	FC3_CTS_SDA_SSEL0	SCT0_GPI2	SCT0_OUT9	CTIMER3MAT3	FC2_SSEL2	TRACEDATA[2]	CLKOUT	SEC_PIO0_24	

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
C12	PIO0_25	PIO0_25	PIO0_25	FC3_RTS_ SCL_SSE L1		FREQME_ GPIO_CLK	CTIMER_I NP6	FC2_SSEL 3	TRACEDA TA[3]	CLKIN	SEC_PIO0 _25	
A12	PIO0_28	PIO0_28	PIO0_28	FC4_SCK			CTIMER4_ MAT0	I2S_BRID GE_CLK_ OUT			SEC_PIO0 _28	
B11	PIO0_29	PIO0_29	PIO0_29	FC4_TXD_ SCL_MIS O_WS			CTIMER4_ MAT1	I2S_BRID GE_WS_O UT			SEC_PIO0 _29	
D14	PIO0_30	PIO0_30	PIO0_30	FC4_RXD_ _SDA_MO SI_DATA			CTIMER4_ MAT2	I2S_BRID GE_DATA _OUT			SEC_PIO0 _30	
D12	PIO0_31	PIO0_31	PIO0_31	FC4_CTS_ SDA_SSE L0	SCT0_GPI 0	SCT0_OU T6	CTIMER4_ MAT3	FC3_SSEL 2			SEC_PIO0 _31	
A10	PIO1_0	PIO1_0	PIO1_0	FC4_RTS_ SCL_SSE L1	SCT0_GPI 1	SCT0_OU T7	CTIMER_I NP8	FC3_SSEL 3				
K2	PIO1_3	PIO1_3	PIO1_3	FC5_SCK					HS_SPI1_ SCK			
K1	PIO1_4	PIO1_4	PIO1_4	FC5_TXD_ SCL_MIS O_WS					HS_SPI1_ MISO			
L2	PIO1_5	PIO1_5	PIO1_5	FC5_RXD_ _SDA_MO SI_DATA					HS_SPI1_ MOSI			
N4	PIO1_6	PIO1_6	PIO1_6	FC5_CTS_ SDA_SSE L0	SCT0_GPI 4	SCT0_OU T4		FC4_SSEL 2	HS_SPI1_ SSELN0			
M1	PIO1_7	PIO1_7	PIO1_7	FC5_RTS_ SCL_SSE L1	SCT0_GPI 5	SCT0_OU T5	CTIMER_I NP9	FC4_SSEL 3	HS_SPI1_ SSELN1			
M5	PIO1_10	PIO1_10	PIO1_10	MCLK		FREQME_ GPIO_CLK	CTIMER_I NP10			CLKOUT		

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
K13	PIO1_11	PIO1_11	PIO1_11	HS_SPI0_SCK			CTIMER2_MAT0					
K14	PIO1_12	PIO1_12	PIO1_12	HS_SPI0_MISO			CTIMER2_MAT1					
K17	PIO1_13	PIO1_13	PIO1_13	HS_SPI0_MOSI			CTIMER2_MAT2					
L16	PIO1_14	PIO1_14	PIO1_14	HS_SPI0_SSELN0			CTIMER2_MAT3					
M16	PIO1_15 / ISP0	PIO1_15	PIO1_15	HS_SPI0_SSELN1			CTIMER3_MAT0					
T17	PIO1_18	PIO1_18	PIO1_18	FLEXSPI0_SCLK	SCT0_GPI0		CTIMER3_MAT3					
U16	PIO1_19	PIO1_19	PIO1_19	FLEXSPI0_SS0_N	SCT0_OUT0		CTIMER4_MAT0			CLKOUT		
T15	PIO1_20	PIO1_20	PIO1_20	FLEXSPI0_DATA0	SCT0_GPI1		CTIMER4_MAT1					
T14	PIO1_21	PIO1_21	PIO1_21	FLEXSPI0_DATA1	SCT0_OUT1		CTIMER4_MAT2					
R13	PIO1_22	PIO1_22	PIO1_22	FLEXSPI0_DATA2	SCT0_GPI2		CTIMER4_MAT3					
R12	PIO1_23	PIO1_23	PIO1_23	FLEXSPI0_DATA3	SCT0_OUT2		CTIMER_INP8					
N12	PIO1_24	PIO1_24	PIO1_24	FLEXSPI0_DATA4	SCT0_GPI3							
R14	PIO1_25	PIO1_25	PIO1_25	FLEXSPI0_DATA5	SCT0_OUT3							
P14	PIO1_26	PIO1_26	PIO1_26	FLEXSPI0_DATA6	SCT0_GPI4							
P13	PIO1_27	PIO1_27	PIO1_27	FLEXSPI0_DATA7	SCT0_OUT4							
U14	PIO1_28	PIO1_28	PIO1_28	FLEXSPI0_DQS	SCT0_GPI5							

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
U12	PIO1_29	PIO1_29	PIO1_29	FLEXSPI0 _SS1_N	SCT0_OU T5	UTICK_CA P2	CTIMER1 NP13	FLEXSPI0 _SCLK_N				
R5	PIO1_30	PIO1_30	PIO1_30	SD0_CLK	SCT0_GPI 0							
R6	PIO1_31	PIO1_31	PIO1_31	SD0_CMD	SCT0_GPI 1							
U4	PIO2_0	PIO2_0	PIO2_0	SD0_D[0]	SCT0_GPI 2							SmartDMA _PIO0
T4	PIO2_1	PIO2_1	PIO2_1	SD0_D[1]	SCT0_GPI 3							SmartDMA _PIO1
T7	PIO2_2	PIO2_2	PIO2_2	SD0_D[2]	SCT0_OU T0							SmartDMA _PIO2
U6	PIO2_3	PIO2_3	PIO2_3	SD0_D[3]	SCT0_OU T1							SmartDMA _PIO3
P6	PIO2_4	PIO2_4	PIO2_4	SD0_WR_ PRT	SCT0_OU T2			SD0_DS				SmartDMA _PIO4
P5	PIO2_5	PIO2_5	PIO2_5	SD0_D[4]	SCT0_OU T3			FC8_SCK				SmartDMA _PIO5
R4	PIO2_6	PIO2_6	PIO2_6	SD0_D[5]	SCT0_GPI 4		CTIMER1_ MAT0	FC8_TXD_ SCL_MIS O_WS				SmartDMA _PIO6
P4	PIO2_7	PIO2_7	PIO2_7	SD0_D[6]	SCT0_GPI 5		CTIMER1_ MAT1	FC8_RXD_ _SDA_MO SI_DATA				SmartDMA _PIO7
T6	PIO2_8	PIO2_8	PIO2_8	SD0_D[7]	SCT0_OU T4		CTIMER1_ MAT2	FC8_CTS_ SDA_SSE L0				SmartDMA _PIO8
T3	PIO2_9	PIO2_9	PIO2_9	SD0_CAR D_DET_N	SCT0_OU T5		CTIMER1_ MAT3	FC8_CTS_ SDA_SSE L1				SmartDMA _PIO9
N5	PIO2_10	PIO2_10	PIO2_10	SD0_RES ET_N	SCT0_GPI 6		CTIMER2_ MAT0	FC8_SSEL 2				SmartDMA _PIO10

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
R2	PIO2_11	PIO2_11	PIO2_11	SD0_VOLT	SCT0_GPI7		CTIMER2_MAT1	FC8_SSEL3				SmartDMA_PIO11
E15	PIO2_14 / CMP0_A	PIO2_14	PIO2_14		SCT0_OUT8		CTIMER1_NP1			32KHZ_CLKOUT		SmartDMA_PIO14
D17	PIO2_15 / CMP0_D	PIO2_15	PIO2_15		SCT0_OUT9					CLKIN		SmartDMA_PIO15
N3	PIO2_24	PIO2_24	PIO2_24	SWO					GPIO_INT_BMAT			SmartDMA_PIO24
M2	PIO2_25	PIO2_25	PIO2_25	SWCLK								SmartDMA_PIO25
M4	PIO2_26	PIO2_26	PIO2_26	SWDIO								SmartDMA_PIO26
M3	PIO2_27	PIO2_27	PIO2_27	USB1_OVERCURRENTN								SmartDMA_PIO27
P1	PIO2_28	PIO2_28	PIO2_28	USB1_PORTPWRN								SmartDMA_PIO28
B10	PIO2_29	PIO2_29	PIO2_29	I3C0_SCL	SCT0_OUT0			CLKOUT				SmartDMA_PIO29
D10	PIO2_30	PIO2_30	PIO2_30	I3C0_SDA	SCT0_OUT3			CLKIN		CMP0_OUT		SmartDMA_PIO30
C14	PIO2_31 / CMP0_B	PIO2_31	PIO2_31	I3C0_PUR	SCT0_OUT7	UTICK_CAPP3	CTIMER1_NP15	SWO				SmartDMA_PIO31
T2	USB1_VBUS	USB1_VBUS										
K5	USB1_VDD3V3	USB1_VDD3V3										
T1	USB1_DM	USB1_DM										
U2	USB1_DP	USB1_DP										
E4	PMIC_MODE1	PMIC_MODE1										
D3	PMIC_MODE0	PMIC_MODE0										

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
K6	PMIC_I2C_SDA	PMIC_I2C_SDA										
K4	PMIC_I2C_SCL	PMIC_I2C_SCL										
D5	PMIC_IRQ_N	PMIC_IRQ_N										
C5	LDO_ENABLE	PMIC_LDO_ENABLE										
B4	XTALIN	XTALIN										
A4	XTALOUT	XTALOUT										
A2	RTCXIN	RTCXIN										
B3	RTCXOUT	RTCXOUT										
C4	RESETN	RESETN										
F12	VREFP	VREFP										
G12	VREFN	VREFN										
D16	PIO3_1	PIO3_1	PIO3_1	PDM_CLK_23	PDM_DAT_A23			FC0_TXD_SCL_MISO_WS	I3C1_SCL			
C16	PIO3_2	PIO3_2	PIO3_2	PDM_CLK_45	PDM_DAT_A45			FC0_RXD_SDA_MOSI_DATA	I3C1_SDA			
D15	PIO3_3	PIO3_3	PIO3_3	PDM_CLK_67	PDM_DAT_A67	LCD_D23		FC0_CTS_SDA_SSEL0	I3C1_PUR	CMP0_OUT		
A8	PIO3_8	PIO3_8	PIO3_8	SD1_CLK	LCD_D9		CTIMER0_MAT0		FC10_SCK			
B8	PIO3_9	PIO3_9	PIO3_9	SD1_CMD	LCD_D10		CTIMER0_MAT1		FC10_TXD_SCL_MISO			

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
C8	PIO3_10	PIO3_10	PIO3_10	SD1_D[0]	LCD_D11		CTIMER0_ MAT2		FC10_RX D_SDA_M OSI			
C10	PIO3_11	PIO3_11	PIO3_11	SD1_D[1]	LCD_D12		CTIMER0_ MAT3		FC10_CTS _SDA_SS ELN0			
A6	PIO3_12	PIO3_12	PIO3_12	SD1_D[2]	LCD_D13		CTIMER_I NP0		FC10_RTS _SCL_SS ELN1			
B7	PIO3_13	PIO3_13	PIO3_13	SD1_D[3]	LCD_D14		CTIMER_I NP1		FC10_SSE LN2			
D9	PIO3_14 / CMP0_E	PIO3_14	PIO3_14	SD1_WR_ PRT	LCD_D15		CTIMER3_ MAT0	SD1_DS	FC10_SSE LN3			
E10	PIO3_15	PIO3_15	PIO3_15	SD1_D[4]	LCD_D16		CTIMER3_ MAT1	FC5_SCK				
C9	PIO3_16	PIO3_16	PIO3_16	SD1_D[5]	LCD_D17		CTIMER3_ MAT2	FC5_TXD_ SCL_MIS O_WS				
D8	PIO3_17	PIO3_17	PIO3_17	SD1_D[6]	LCD_D18		CTIMER3_ MAT3	FC5_RXD_ _SDA_MO SI_DATA				
B6	PIO3_18	PIO3_18	PIO3_18	SD1_D[7]	LCD_D19		CTIMER4_ MAT0	FC5_CTS_ SDA_SSE L0				
C6	PIO3_19	PIO3_19	PIO3_19	SD1_CAR D_DET_N	LCD_D20		CTIMER4_ MAT1	MCLK				
D6	PIO3_20	PIO3_20	PIO3_20	SD1_RES ET_N	LCD_D21		CTIMER4_ MAT2					
E5	PIO3_21	PIO3_21	PIO3_21	SD1_VOL T	LCD_D22		CTIMER4_ MAT3		GPIO_INT _BMAT			
R16	PIO3_25	PIO3_25	PIO3_25	FC6_SCK								
T16	PIO3_26	PIO3_26	PIO3_26	FC6_TXD_ SCL_MIS O_WS								

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
N14	PIO3_27	PIO3_27	PIO3_27	FC6_RXD_ SDA_MO SI_DATA								
N13	PIO3_28 / ISP1	PIO3_28	PIO3_28	FC6_CTS_ SDA_SSE L0								
M13	PIO3_29 / ISP2	PIO3_29	PIO3_29	FC6_RTS_ SCL_SSE L1								
N15	PIO4_0	PIO4_0	PIO4_0	FC7_SCK			FREQME_ GPIO_CLK			CLKOUT		
M15	PIO4_1	PIO4_1	PIO4_1	FC7_TXD_ SCL_MIS O_WS						CLKIN		
M17	PIO4_2	PIO4_2	PIO4_2	FC7_RXD_ SDA_MO SI_DATA								
M14	PIO4_3	PIO4_3	PIO4_3	FC7_CTS_ SDA_SSE L0								
P17	PIO4_4	PIO4_4	PIO4_4	FC7_RTS_ SCL_SSE L1				FC1_SCK				
P16	PIO4_5	PIO4_5	PIO4_5	FC7_SSEL 2				FC1_TXD_ SCL_MIS O_WS				
P15	PIO4_6	PIO4_6	PIO4_6	FC7_SSEL 3				FC1_RXD_ SDA_MO SI_DATA				
D2	MIPI_DSI_ CLKP	MIPI_DSI_ CLKP										
D1	MIPI_DSI_ CLKN	MIPI_DSI_ CLKN										

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
B1	MIPI_DSI_ D0P	MIPI_DSI_ D0P										
C2	MIPI_DSI_ D0N	MIPI_DSI_ D0N										
E3	MIPI_DSI_ D1P	MIPI_DSI_ D1P										
F3	MIPI_DSI_ D1N	MIPI_DSI_ D1N										
J8	MIPI_DSI_ VDD11	MIPI_DSI_ VD11										
F8	MIPI_DSI_ VDD18	MIPI_DSI_ VDD18										
F5	MIPI_DSI_ VDDA_CA P	MIPI_DSI_ VDDA_CA P										
F4	MIPI_DSI_ VSS	MIPI_DSI_ VSS										
H2	PIO4_11	PIO4_11	PIO4_11	FC2_SCK	FLEXSPI1_ SCLK		SD1_CLK					
H1	PIO4_12	PIO4_12	PIO4_12	FC2_TXD_ SCL_MIS O_WS	FLEXSPI1_ DATA0		SD1_CMD					
G2	PIO4_13	PIO4_13	PIO4_13	FC2_RXD_ SDA_MO SI_DATA	FLEXSPI1_ DATA1		SD1_D[0]					
F1	PIO4_14	PIO4_14	PIO4_14	FC2_CTS_ SDA_SSE L0	FLEXSPI1_ DATA2		SD1_D[1]					
K3	PIO4_15	PIO4_15	PIO4_15	FC2_RTS_ SCL_SSE L1	FLEXSPI1_ DATA3		SD1_D[2]					
H3	PIO4_16	PIO4_16	PIO4_16	FC2_SSEL 2	FLEXSPI1_ DQS		SD1_D[3]					

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
F2	PIO4_17	PIO4_17	PIO4_17	FC2_SSEL 3	FLEXSPI1 _SS1_N	FLEXSPI1 _SCLK_N	SD1_WR_ PRT					
E13	PIO4_18 / ADC0_6	PIO4_18	PIO4_18		FLEXSPI1 _SS0_N		SD1_D[4]					
R8	PIO4_20	PIO4_20	PIO4_20	DBI_CSX			SD1_D[6]		FC11_SC K		FLEXIO_D 0	
P10	PIO4_21	PIO4_21	PIO4_21	DBI_DCX			SD1_D[7]		FC11_TXD _SCL_MIS O		FLEXIO_D 1	
U10	PIO4_22	PIO4_22	PIO4_22				SD1_CAR D_DET_N		FC11_RX D_SDA_M OSI		FLEXIO_D 2	
T8	PIO4_23	PIO4_23	PIO4_23	DBI_RWD X	LCD_ENA BLE		SD1_RES ET_N		FC11_CTS _SDA_SS ELN0	TRACECL K	FLEXIO_D 3	
T10	PIO4_24	PIO4_24	PIO4_24	DBI_WRX	LCD_DTC LK		SD1_VOL T		FC11_RTS _SCL_SS ELN1	TRACEDA TA[0]	FLEXIO_D 4	
T11	PIO4_25	PIO4_25	PIO4_25	DBI_E	LCD_HSY NC				FC11_SSE LN2	TRACEDA TA[1]	FLEXIO_D 5	
T12	PIO4_26	PIO4_26	PIO4_26	LCD_VSY NC					FC11_SSE LN3	TRACEDA TA[2]	FLEXIO_D 6	
P9	PIO4_27	PIO4_27	PIO4_27	LCD_D0	DBI_D0					TRACEDA TA[3]	FLEXIO_D 7	
U8	PIO4_28	PIO4_28	PIO4_28	LCD_D1	DBI_D1						FLEXIO_D 8	
P8	PIO4_29	PIO4_29	PIO4_29	LCD_D2	DBI_D2						FLEXIO_D 9	
N8	PIO4_30	PIO4_30	PIO4_30	LCD_D3	DBI_D3				FC12_TXD _SCL_MIS O		FLEXIO_D 10	

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
N10	PIO4_31	PIO4_31	PIO4_31	LCD_D4	DBI_D4				FC12_RX D_SDA_M OSI		FLEXIO_D 11	
P12	PIO5_0	PIO5_0	PIO5_0	LCD_D5	DBI_D5				FC12_CTS _SDA_SS ELN0		FLEXIO_D 12	
M9	PIO5_1	PIO5_1	PIO5_1	LCD_D6	DBI_D6				FC12_RTS _SCL_SS ELN1		FLEXIO_D 13	
R9	PIO5_2	PIO5_2	PIO5_2	LCD_D7	DBI_D7				FC12_SSE LN2	LOW_FRE Q_CLKOU T	FLEXIO_D 14	
R10	PIO5_3	PIO5_3	PIO5_3	LCD_D8	DBI_D8				FC12_SSE LN3	LOW_FRE Q_CLKOU T_N	FLEXIO_D 15	
P2	PIO5_4	PIO5_4	PIO5_4	LCD_D9	DBI_D9		PDM_CLK 01					
P3	PIO5_8	PIO5_8	PIO5_8	LCD_D13	DBI_D13		PDM_DAT A01					
H5	PIO5_15	PIO5_15	PIO5_15	LCD_D20	FLEXSPI1 _DATA4		FC4_CTS_ SDA_SSE L0					
H4	PIO5_16	PIO5_16	PIO5_16	LCD_D21	FLEXSPI1 _DATA5		FC4_RTS_ SCL_SSE L1					
J3	PIO5_17	PIO5_17	PIO5_17	LCD_D22	FLEXSPI1 _DATA6		FC4_SSEL 2					
J4	PIO5_18	PIO5_18	PIO5_18	LCD_D23	FLEXSPI1 _DATA7		FC4_SSEL 3					
J12, J13,K12, M10,M12	VDDIO_0											

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
E9, F10,F11, F9,J5 J6	VDDIO_1											
N6, P7	VDDIO_2											
M8 N9	VDDIO_3											
F6, F7	VDDIO_4											
G9, H10,H8, H9,J10, J11,J9, K10,K8, K9, L9	VDDCORE											
D4, B2	VDD_AO1 V8											
H13	VDDA_AD C1V8											
E12	VDDA_BIA S											
D11, D7	VSSA											
A1, A17, C3, C7, C11, C15, E7, E11, G3, G4, G5, G7, G8, G10, G11, G13, G14, G15, H11, K7, K11, L3, L4, L5, L6, L7, L8, L10, L11, L12, L13, L14, L15,	VSS											

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
M7, M11, N7, N11, P11, R3, R7, R11, R15, U1, U17												
G6, M6, H7, J7, J14, H6, E6	VDD1V8											
E8	VDD1V8_1											

5.3 i.MX RT500 Pinouts: 141 CSP package

Part Num (141WLC SP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
J1	PIO0_0	PIO0_0	PIO0_0	FC0_SCK			CTIMER0_ MAT0	I2S_BRIDGE_CLK_IN	GPIO_INT_BMAT			
G3	PIO0_1	PIO0_1	PIO0_1	FC0_TXD_SCL_MISO_WS			CTIMER0_ MAT1	I2S_BRIDGE_WS_IN				
F1	PIO0_10 / TDI	PIO0_10	PIO0_10	FC1_CTS_SDA_SSEL0	SCT0_GPI7	SCT0_OUT7	CTIMER1_ MAT3	FC0_SSEL2				
E3	PIO0_11 / TDO	PIO0_11	PIO0_11	FC1_RTS_SCL_SSEL1	SCT0_GPI0	SCT0_OUT8	CTIMER1_ NP2	FC0_SSEL3				
G5	PIO0_12 / ADC0_1	PIO0_12	PIO0_12	FC1_SSEL2	SCT0_GPI2	SCT0_OUT2	CTIMER1_ NP3					
J2	PIO0_13 / ADC0_9	PIO0_13	PIO0_13	FC1_SSEL3	SCT0_GPI3	SCT0_OUT3	CTIMER0_ MAT1					
K6	PIO0_14	PIO0_14	PIO0_14	FC2_SCK	SCT0_GPI0	SCT0_OUT0	CTIMER2_ MAT0	I2S_BRIDGE_CLK_IN				
K4	PIO0_15	PIO0_15	PIO0_15	FC2_TXD_SCL_MISO_WS	SCT0_GPI1	SCT0_OUT1	CTIMER2_ MAT1	I2S_BRIDGE_WS_IN				
M3	PIO0_16	PIO0_16	PIO0_16	FC2_RXD_SDA_MOSI_DATA	SCT0_GPI2	SCT0_OUT2	CTIMER2_ MAT2	I2S_BRIDGE_DATA_IN				
M2	PIO0_17	PIO0_17	PIO0_17	FC2_CTS_SDA_SSEL0	SCT0_GPI3	SCT0_OUT3	CTIMER2_ MAT3	FC5_SSEL2				
J4	PIO0_18	PIO0_18	PIO0_18	FC2_RTS_SCL_SSEL1	SCT0_GPI6	SCT0_OUT6	CTIMER1_ NP4	FC5_SSEL3				
H4	PIO0_19 / ADC0_2	PIO0_19	PIO0_19	FC2_SSEL2	SCT0_GPI4	SCT0_OUT4	CTIMER1_ NP5	UTICK_CAP0				

Table continues on the next page...

Part Num (141WLC SP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
H2	PIO0_2	PIO0_2	PIO0_2	FC0_RXD_SDA_MOSI_DATA			CTIMER0_MAT2	I2S_BRIDGE_DATA_IN				
M4	PIO0_21	PIO0_21	PIO0_21	FC3_SCK	SCT0_GPI5	SCT0_OUT5	CTIMER3_MAT0	CTIMER_INP11	TRACECLK			
J5	PIO0_22	PIO0_22	PIO0_22	FC3_TXD_SCL_MISO_WS	SCT0_GPI6	SCT0_OUT6	CTIMER3_MAT1	CTIMER_INP7	TRACEDATA[0]			
L5	PIO0_23	PIO0_23	PIO0_23	FC3_RXD_SDA_MOSI_DATA	SCT0_GPI7	SCT0_OUT8	CTIMER3_MAT2	CTIMER0_MAT3	TRACEDATA[1]			
L4	PIO0_24	PIO0_24	PIO0_24	FC3_CTS_SDA_SSEL0	SCT0_GPI2	SCT0_OUT9	CTIMER3_MAT3	FC2_SSEL2	TRACEDATA[2]	CLKOUT		
H6	PIO0_25	PIO0_25	PIO0_25	FC3_RTS_SCL_SSEL1		FREQMGPIOP_CLK	CTIMER_INP6	FC2_SSEL3	TRACEDATA[3]	CLKIN		
M6	PIO0_28	PIO0_28	PIO0_28	FC4_SCK			CTIMER4_MAT0	I2S_BRIDGE_CLK_OUT				
J7	PIO0_29	PIO0_29	PIO0_29	FC4_TXD_SCL_MISO_WS			CTIMER4_MAT1	I2S_BRIDGE_WS_OUTPUT				
G2	PIO0_3	PIO0_3	PIO0_3	FC0_CTS_SDA_SSEL0			CTIMER0_MAT3	FC1_SSEL2				
L3	PIO0_30	PIO0_30	PIO0_30	FC4_RXD_SDA_MOSI_DATA			CTIMER4_MAT2	I2S_BRIDGE_DATA_OUT				
J6	PIO0_31	PIO0_31	PIO0_31	FC4_CTS_SDA_SSEL0	SCT0_GPI0	SCT0_OUT6	CTIMER4_MAT3	FC3_SSEL2				

Table continues on the next page...

Part Num (141WLC SP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
F4	PIO0_4	PIO0_4	PIO0_4	FC0_RTS_SCL_SSEL1			CTIMER1_NP0	FC1_SSEL3		CMP0_OUT		
H3	PIO0_5 / ADC0_0	PIO0_5	PIO0_5	FC0_SSEL2	SCT0_GPI0	SCT0_OUT0	CTIMER1_NP1					
K1	PIO0_6 / ADC0_8	PIO0_6	PIO0_6	FC0_SSEL3	SCT0_GPI1	SCT0_OUT1	CTIMER0_MAT0					
E4	PIO0_7 / TRST	PIO0_7	PIO0_7	FC1_SCK	SCT0_GPI4	SCT0_OUT4	CTIMER1_MAT0	I2S_BRIDGE_CLK_OUT				
G1	PIO0_8 / TCK	PIO0_8	PIO0_8	FC1_TXD_SCL_MISO_WS	SCT0_GPI5	SCT0_OUT5	CTIMER1_MAT1	I2S_BRIDGE_WS_OUT				
F3	PIO0_9 / TMS	PIO0_9	PIO0_9	FC1_RXD_SDA_MOSI_DATA	SCT0_GPI6	SCT0_OUT6	CTIMER1_MAT2	I2S_BRIDGE_DATA_OUT				
L7	PIO1_0	PIO1_0	PIO1_0	FC4_RTS_SCL_SSEL1	SCT0_GPI1	SCT0_OUT7	CTIMER1_NP8	FC3_SSEL3				
D3	PIO1_11	PIO1_11	PIO1_11	HS_SPI0_SCK			CTIMER2_MAT0					
E2	PIO1_12	PIO1_12	PIO1_12	HS_SPI0_MISO			CTIMER2_MAT1					
D2	PIO1_13	PIO1_13	PIO1_13	HS_SPI0_MOSI			CTIMER2_MAT2					
C2	PIO1_14	PIO1_14	PIO1_14	HS_SPI0_SSELN0			CTIMER2_MAT3					
D1	PIO1_15 / ISP0	PIO1_15	PIO1_15	HS_SPI0_SSELN1			CTIMER3_MAT0					
A5	PIO1_18	PIO1_18	PIO1_18	FLEXSPI0_SCLK	SCT0_GPI0		CTIMER3_MAT3					
D4	PIO1_19	PIO1_19	PIO1_19	FLEXSPI0_SS0_N	SCT0_OUT0		CTIMER4_MAT0			CLKOUT		

Table continues on the next page...

Part Num (141WLC SP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
B5	PIO1_20	PIO1_20	PIO1_20	FLEXSPI0_DATA0	SCT0_GPI1		CTIMER4_MAT1					
C5	PIO1_21	PIO1_21	PIO1_21	FLEXSPI0_DATA1	SCT0_OUT1		CTIMER4_MAT2					
D5	PIO1_22	PIO1_22	PIO1_22	FLEXSPI0_DATA2	SCT0_GPI2		CTIMER4_MAT3					
C6	PIO1_23	PIO1_23	PIO1_23	FLEXSPI0_DATA3	SCT0_OUT2		CTIMER1_NP8					
A6	PIO1_28	PIO1_28	PIO1_28	FLEXSPI0_DQS	SCT0_GPI5							
F11	PIO1_3	PIO1_3	PIO1_3	FC5_SCK					HS_SPI1_SCK			
F12	PIO1_4	PIO1_4	PIO1_4	FC5_TXD_SCL_MISO_WS					HS_SPI1_MISO			
E12	PIO1_5	PIO1_5	PIO1_5	FC5_RXD_SDA_MOSI_DATA					HS_SPI1_MOSI			
E9	PIO1_6	PIO1_6	PIO1_6	FC5_CTS_SDA_SSEL0	SCT0_GPI4	SCT0_OUT4		FC4_SSEL2	HS_SPI1_SSELN0			
F9	PIO1_7	PIO1_7	PIO1_7	FC5_RTS_SCL_SSEL1	SCT0_GPI5	SCT0_OUT5	CTIMER1_NP9	FC4_SSEL3	HS_SPI1_SSELN1			
L2	PIO1_9 / ADC0_12 / CMP1_B	PIO1_9	PIO1_9	FC5_SSEL3	SCT0_GPI7	UTICK_CAP1	CTIMER1_MAT3		HS_SPI1_SSELN3			
K2	PIO2_14 / CMP0_A	PIO2_14	PIO2_14		SCT0_OUT8		CTIMER1_NP1			32KHZ_CLKOUT		SmartDMA_PIO14
L1	PIO2_15 / CMP0_D	PIO2_15	PIO2_15		SCT0_OUT9					CLKIN		SmartDMA_PIO15
E8	PIO2_24	PIO2_24	PIO2_24	SWO					GPIO_INT_BMAT			SmartDMA_PIO24

Table continues on the next page...

Part Num (141WLC SP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
F10	PIO2_25	PIO2_25	PIO2_25	SWCLK								SmartDMA_PIO25
E11	PIO2_26	PIO2_26	PIO2_26	SWDIO								SmartDMA_PIO26
E10	PIO2_27	PIO2_27	PIO2_27	USB1_OV ERCURRE NTN								SmartDMA_PIO27
M7	PIO2_29	PIO2_29	PIO2_29	I3C0_SCL	SCT0_OU T0			CLKOUT				SmartDMA_PIO29
K7	PIO2_30	PIO2_30	PIO2_30	I3C0_SDA	SCT0_OU T3			CLKIN		CMP0_OU T		SmartDMA_PIO30
K5	PIO2_31 / CMP0_B	PIO2_31	PIO2_31	I3C0_PUR	SCT0_OU T7	UTICK_CA P3	CTIMER_I NP15	SWO				SmartDMA_PIO31
A4	PIO3_28 / ISP1	PIO3_28	PIO3_28	FC6_CTS_ SDA_SSE L0								
B4	PIO3_29 / ISP2	PIO3_29	PIO3_29	FC6_RTS_ SCL_SSE L1								
B8	PIO4_20	PIO4_20	PIO4_20	DBI_CSX			SD1_D[6]		FC11_SC K		FLEXIO_D 0	
B7	PIO4_21	PIO4_21	PIO4_21	DBI_DCX			SD1_D[7]		FC11_TXD _SCL_MIS O		FLEXIO_D 1	
A8	PIO4_22	PIO4_22	PIO4_22				SD1_CAR D_DET_N		FC11_RX D_SDA_M OSI		FLEXIO_D 2	
E7	PIO4_23	PIO4_23	PIO4_23	DBI_RWD X	LCD_ENA BLE		SD1_RES ET_N		FC11_CTS _SDA_SS ELN0	TRACECL K	FLEXIO_D 3	
C7	PIO4_24	PIO4_24	PIO4_24	DBI_WRX	LCD_DTC LK		SD1_VOL T		FC11_RTS _SCL_SS ELN1	TRACEDA TA[0]	FLEXIO_D 4	

Table continues on the next page...

Part Num (141WLC SP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
D7	PIO4_25	PIO4_25	PIO4_25	DBI_E	LCD_HSY NC				FC11_SSE LN2	TRACEDA TA[1]	FLEXIO_D 5	
D6	PIO4_26	PIO4_26	PIO4_26	LCD_VSY NC					FC11_SSE LN3	TRACEDA TA[2]	FLEXIO_D 6	
C8	PIO4_27	PIO4_27	PIO4_27	LCD_D0	DBI_D0					TRACEDA TA[3]	FLEXIO_D 7	
B10	PIO4_28	PIO4_28	PIO4_28	LCD_D1	DBI_D1						FLEXIO_D 8	
D8	PIO4_29	PIO4_29	PIO4_29	LCD_D2	DBI_D2						FLEXIO_D 9	
C9	PIO4_30	PIO4_30	PIO4_30	LCD_D3	DBI_D3				FC12_TXD _SCL_MIS O		FLEXIO_D 10	
B9	PIO4_31	PIO4_31	PIO4_31	LCD_D4	DBI_D4				FC12_RX D_SDA_M OSI		FLEXIO_D 11	
D9	PIO5_4	PIO5_4	PIO5_4	LCD_D9	DBI_D9		PDM_CLK 01					
C11	PIO5_8	PIO5_8	PIO5_8	LCD_D13	DBI_D13		PDM_DAT A01					
C4	PIO6_27	PIO6_27	PIO6_27	MCLK								
J12	MIPI_DSI_ CLKN	MIPI_DSI_ CLKN										
H11	MIPI_DSI_ CLKP	MIPI_DSI_ CLKP										
H9	MIPI_DSI_ D0N	MIPI_DSI_ D0N										
H8	MIPI_DSI_ D0P	MIPI_DSI_ D0P										
H12	MIPI_DSI_ VDD11											

Table continues on the next page...

Part Num (141WLC SP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
G10	MIPI_DSI_VDD18											
K12	MIPI_DSI_VDDA_CAP											
J11	MIPI_DSI_VSS											
K9	PMIC_IRQ_N	PMIC_IRQ_N										
K10	PMIC_MODE0	PMIC_MODE0										
J9	PMIC_MODE1	PMIC_MODE1										
L11	RESETN	RESETN										
J10	RTCXIN	RTCXIN										
K11	RTCXOUT	RTCXOUT										
B11	USB1_DM	USB1_DM										
B12	USB1_DP	USB1_DP										
D10	USB1_VD_D3V3	USB1_VD_D3V3										
K3	VREFN/VSSA	VREFN										
J3	VREFP/VDDA_AD_C1V8/VDDA_BIAS	VREFP										
L9	XTALIN	XTALIN										
K8	XTALOUT	XTALOUT										
A3, B1, B6, E1, F2, G4	VDDIO_0											

Table continues on the next page...

Part Num (141WLC SP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
D11, G6, H5, L6, M5	VDDIO_1											
NC	VDDIO_2											
E5	VDDIO_3											
NC	VDDIO_4											
A10, B2, C1, C3, C10, C12, E6, F6, G7, G12, M8	VDDCORE											
A11, L12, M11, F5, L8	VDD1V8											
L10	VDD_AO1 V8											
M10	VDD1V8_1											
J8	VSSA											
A1, A2, A12, B3, F7, F8, G8, G11, H1, H7, G9, H10, M1, M9, M12	VSS											

5.4 249-pin FOWLP and 141-pin WLCSP ballmaps

The following figure shows the 249 FOWLP ballmap for this device.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	RTCXIN		XTALOUT		PIO3_12		PIO3_8		PIO1_0		PIO0_28		PIO0_21		PIO0_16	VSS
B	MIPL_DSI_D0P	VDD_AO1V8	RTCXOUT	XTALIN		PIO3_18	PIO3_13	PIO3_9		PIO2_29	PIO0_29	PIO0_14		PIO0_22	PIO0_15	PIO0_18	PIO0_17
C		MIPL_DSI_D0N	VSS	RESETN	LDO_ENABLE	PIO3_19	VSS	PIO3_10	PIO3_16	PIO3_11	VSS	PIO0_25	PIO0_23	PIO2_31	VSS	PIO3_2	
D	MIPL_DSI_CLKN	MIPL_DSI_CLKP	PMIC_MODE0	VDD_AO1V8	PMIC_IRQ_N	PIO3_20	VSSA	PIO3_17	PIO3_14	PIO2_30	VSSA	PIO0_31	PIO0_24	PIO0_30	PIO0_3	PIO3_1	PIO2_15
E			MIPL_DSI_D1P	PMIC_MODE1	PIO3_21	VDD1V8	VSS	VDD1V8_1	VDDIO_1	PIO3_15	VSS	VDDA_BIAS	PIO4_18	PIO0_12	PIO2_14		
F	PIO4_14	PIO4_17	MIPL_DSI_D1N	MIPL_DSI_VSS	MIPL_DSI_VDDA_CAP	VDDIO_1	VDDIO_4	MIPL_DSI_VDDA18	VDDIO_1	VDDIO_1	VDDIO_1	VREFP	PIO0_19	PIO0_0	PIO0_13	PIO0_5	PIO0_6
G		PIO4_13	VSS	VSS	VSS	VDD1V8	VSS	VSS	VDDCORE	VSS	VSS	VREFN	VSS	VSS	VSS	PIO0_1	
H	PIO4_12	PIO4_11	PIO4_16	PIO0_16	PIO0_15	VDD1V8	VDD1V8	VDDCORE	VDDCORE	VDDCORE	VSS	PIO0_8	VDDA_ADC1V8	PIO0_4	PIO0_3	PIO0_2	PIO0_9
J			PIO0_17	PIO0_18	VDDIO_1	VDDIO_1	VDD1V8	MIPL_DSI_VDD11	VDDCORE	VDDCORE	VDDCORE	VDDCORE	VDDIO_0	VDDIO_0	VDD1V8	PIO0_7	
K	PIO1_4	PIO1_3	PIO4_15	PMIC_OC_SCL	USB1_VDD3V3	PMIC_OC_SDA	VSS	VDDCORE	VDDCORE	VDDCORE	VSS	VDDIO_0	PIO1_11	PIO1_12	PIO0_11	PIO0_10	PIO1_13
L		PIO1_5	VSS	VSS	VSS	VSS	VSS	VSS	VDDCORE	VDDCORE	VSS	VSS	VSS	VSS	VSS	PIO1_14	
M	PIO1_7	PIO2_25	PIO2_27	PIO2_26	PIO1_10	VDD1V8	VSS	VDDIO_1	PIO0_1	VDDIO_0	VSS	VDDIO_0	PIO3_29	PIO4_3	PIO4_1	PIO1_15	PIO4_2
N			PIO2_24	PIO1_6	PIO2_10	VDDIO_2	VSS	PIO4_30	VDDIO_2	PIO4_31	VSS	PIO1_24	PIO3_28	PIO3_27	PIO4_0		
P	PIO2_28	PIO0_4	PIO0_8	PIO2_7	PIO2_5	PIO2_4	VDDIO_2	PIO4_29	PIO2_27	PIO4_21	VSS	PIO0_0	PIO1_27	PIO1_26	PIO4_6	PIO4_5	PIO4_4
R		PIO2_11	VSS	PIO2_6	PIO1_30	PIO1_31	VSS	PIO4_20	PIO6_2	PIO0_3	VSS	PIO1_23	PIO1_22	PIO1_25	VSS	PIO3_25	
T	USB1_DM	USB1_VBUS	PIO2_9	PIO2_1		PIO2_8	PIO2_2	PIO4_23		PIO4_24	PIO4_25	PIO4_26		PIO1_21	PIO1_20	PIO3_26	PIO1_18
U	VSS	USB1_DP		PIO2_0		PIO2_3		PIO4_28				PIO4_29		PIO1_28		PIO1_19	VSS

Figure 43. i.MX RT500 249-pin FOWLP ballmap

The following figure shows the 141-pin WLCSP ballmap for this device.

	1	2	3	4	5	6	7	8	9	10	11	12
M	VSS	PIO0_17	PIO0_16	PIO0_21	VDDIO_1	PIO0_28	PIO2_29	VDDCORE	VSS	VDD1V8_1	VDD1V8	VSS
L	PIO2_15	PIO1_9	PIO0_30	PIO0_24	PIO0_23	VDDIO_1	PIO1_0	VDD1V8	XTALOUT	VDD_AO1V8	RESETN	VDD1V8
K	PIO0_6	PIO2_14	VSSA	PIO0_15	PIO2_31	PIO0_14	PIO2_30	XTALOUT	PMIC_IRQ	PMIC_MODE0	RTCXOUT	MIPL_DSI_VDDA_CAP
J	PIO0_0	PIO0_13	VDDA_ADC1V8	PIO0_18	PIO0_22	PIO0_31	PIO0_29	VSSA	PMIC_MODE1	RTCXIN	MIPL_DSI_VSS	MIPL_DSI_CLKN
H	VSS	PIO0_2	PIO0_5	PIO0_19	VDDIO_1	PIO0_25	VSS	MIPL_DSI_D0P	MIPL_DSI_D0N	VSS	MIPL_DSI_CLKP	MIPL_DSI_VDD11
G	PIO0_8	PIO0_3	PIO0_1	VDDIO_0	PIO0_12	VDDIO_1	VDDCORE	VSS	VSS	MIPL_DSI_VDD18	VSS	VDDCORE
F	PIO0_10	VDDIO_0	PIO0_9	PIO0_4	VDD1V8	VDDCORE	VSS	VSS	PIO1_7	PIO2_25	PIO1_3	PIO1_4
E	VDDIO_0	PIO1_12	PIO0_11	PIO0_7	VDDIO_3	VDDCORE	PIO4_23	PIO2_24	PIO1_6	PIO2_27	PIO2_26	PIO1_5
D	PIO1_15	PIO1_13	PIO1_11	PIO1_19	PIO1_22	PIO4_26	PIO4_25	PIO4_29	PIO0_4	USB1_VDD3V3	VDDIO_1	
C	VDDCORE	PIO1_14	VDDCORE	PIO6_27	PIO1_21	PIO1_23	PIO4_24	PIO4_27	PIO4_30	VDDCORE	PIO0_8	VDDCORE
B	VDDIO_0	VDDCORE	VSS	PIO3_29	PIO1_20	VDDIO_0	PIO4_21	PIO4_20	PIO4_31	PIO4_28	USB0_DM	USB0_DP
A	VSS	VSS	VDDIO_0	PIO3_28	PIO1_18	PIO1_28		PIO4_22		VDDCORE	VDD1V8	VSS

Figure 44. i.MX RT500 141-pin CSP ballmap

5.5 Termination of unused pins

The following table shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 50. Termination of unused pins

Pin	Default state ¹	Recommended termination of unused pins
All PION pins	Most are Z, a few are PU	Can be left unconnected if configured by software as an output with pull-up disabled and driven LOW.
PMIC_I2C_SCL/SDA	Z	Leave unconnected
PMIC_IRQ_N	Z	Tie to VDD_AO1V8 if not used in the system.
PMIC_MODEn	0	Leave unconnected.
RESETN	1	Tie high if not used in the system.
RTCXIN	-	Tie to ground.
RTCXOUT	-	Leave unconnected.
USB1_DM/DP	F	Can be left unconnected. If the USB interface is not used, these pins can be left unconnected except in deep power-down mode where they must be externally pulled low. When the USB PHY is disabled, the pins are floating.
USB1_VBUS	F	Leave unconnected.
VDD1V8	F	Leave unconnected.
VDD_1V8_1	F	Tie to 1.8V power during active. Can be powered off during deep sleep mode to reduce current consumption by approximately 22 uA.
USB1_VDD3V3	F	Leave unconnected.
VDD_AO1V8	F	Tie to 1.8V power.
VDDA_ADC1V8	F	Tie to 1.8V power.

Table continues on the next page...

Table 50. Termination of unused pins (continued)

Pin	Default state ¹	Recommended termination of unused pins
VDDA_BIAS	F	Tie to 1.8V power.
VREFN	F	Tie to VSS.
VREFP	F	Tie to VDDA_ADC1V8 analog supply
MIPI_DSI_VDD11	F	10 kΩ resistor to ground
MIPI_DSI_VDD18	F	10 kΩ resistor to ground
MIPI_DSI_VDDA_CAP	F	Leave unconnected
MIPI_DSI_VSS	F	Tie to VSS
VSSA	-	Tie to VSS.
XTALIN	-	Tie to ground.
XTALOUT	-	Leave unconnected.

1. Z = Input, pull-up, and pull-down disabled; PU = Pull-Up enabled; F = Floating, High-Z

5.6 Pin states in different power modes

Table 51. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep	Deep power-down
All PION pins	As configured in IOCON ¹ . Default is Z (input, pull-up, and pull-down disabled), except for a few pins where the pull-up and input are enabled.			Floating

1. Default and programmed pin states are retained in sleep and deep-sleep.

5.7 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
249-pin FOWLP	98ASA01357D
141-pin WLCSP	98ASA01653D

6 Power supply for pins

The following table shows the GPIOs belonging to the specific VDDIO groups and VDD_AO1V8 domain.

VDDIO_0, 1, 2, and 4 supply pins can ONLY be powered from 1.71V to 1.98V. The VDDIO_3 supply pin can be powered between 1.71V to 3.6V.

Table 52. Power supply for pins

Pin	GPIO pins
VDDIO_0	PIO0_0 to PIO0_13 (Fail Safe Pads) PIO1_11 to PIO1_15 (Fail Safe Pads) PIO1_18 to PIO1_29 (High Speed Pads) PIO2_14 to PIO2_15 (Fail Safe Pads) PIO3_25 to PIO3_29 (Fail Safe Pads) PIO4_0 to PIO4_6 (Fail Safe Pads)
VDDIO_1	PIO0_14 to PIO0_19 (Fail Safe Pads) PIO0_21 to PIO0_25 (Fail Safe Pads) PIO0_28 to PIO0_31 (Fail Safe Pads) PIO1_0 (Fail Safe Pads) PIO1_2 to PIO1_7 (Fail Safe Pads) PIO1_10 (Fail Safe Pad) PIO2_24 to PIO2_31 (High Speed Pads) PIO3_1 to PIO3_3 (Fail Safe Pads) PIO4_11 to PIO4_17 (High Speed Pads) PIO4_18 (Fail Safe Pad) PIO5_15 to PIO5_18 (High Speed) PMIC_I2C_SCL PMIC_I2C_SDA
VDDIO_2	PIO1_30 to PIO1_31 (High Speed Pads) PIO2_0 to PIO2_8 (High Speed Pads) PIO2_9 to PIO2_11 (Fail Safe Pads)
VDDIO_3	PIO4_20 to PIO4_31 (Fail Safe Pads) PIO5_0 to PIO5_4, PIO5_8 (Fail Safe Pads)
VDDIO_4	PIO3_8 to PIO3_18 (High Speed Pads) PIO3_19 to PIO3_21 (Fail Safe Pads)
VDD_AO1V8	RESETN LDO_ENABLE PMIC_IRQ_N PMIC_MODE0 and PMIC_MODE1

7 Revision history

Table 53. Revision history

Rev. No.	Date	Substantial changes
0	02/2021	Initial public release

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Table continues on the next page...

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Addendum to Rev. 0 of the i.MX RT500 Low-Power Crossover Processor Data Sheet

This addendum identifies changes to Rev. 0 of the i.MX RT500 Low-Power Crossover Processor Data Sheet. The changes described in this addendum have not been implemented in the specified pages.

1 Update the table “General operating conditions”

Location: [Section 1.1.6, Table 5, Page 14](#)

Add the following row to Table 5, “General operating conditions”

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{otp_clk} ($f_{clk}/OTP_CLK_DIV[DIV]$)	OTP clock frequency	For OTP programming only	-	-	120	MHz

2 Update the section “Termination of unused pins”

Location: [Section 5.5, Page 107](#)

Replace the paragraph text within the section “Termination of unused pins” with the text below.

The following table shows how to terminate pins on functions that are not used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

By default, unused pins with GPIO functions are tri-stated with the input buffer disabled and can remain floating.

All power pins in the domains listed below must be connected to the recommended voltage.

3 Update the table “Termination of unused pins”

Location: [Section 5.5, Table 50, Page 107](#)

Replace Table 50 “Termination of unused pins” with the following table.

Function	Pin Name	Default state ¹	Recommended termination of unused pins
GPIO	All PION pins	Z	Leave unconnected.
PMIC Control	PMIC_I2C_SCL/SDA	Z	Leave unconnected.
PMIC Control	PMIC_IRQ_N	I, Z	10 kΩ resistor to VDD_AO1V8.
PMIC Control	PMIC_MODEn	O	Leave unconnected.
Control	LDO_ENABLE	I	10 kΩ resistor to ground.
Control	RESETN	I	100 kΩ resistor to VDD_AO1V8.

Update the table “Termination of unused pins”

Oscillator	RTCXIN	I	Connect to ground.
Oscillator	RTCXOUT	-	Leave unconnected.
Oscillator	XTALIN	I	Connect to ground.
Oscillator	XTALOUT	-	Leave unconnected.
USB1	USB1_DM/DP	-	Leave unconnected.
USB1	USB1_VBUS	-	Leave unconnected.
USB1	USB1_VDD3V3	-	Leave unconnected.
MIPI_DSI	MIPI_DSI_VDD11	-	10 kΩ resistor to ground.
MIPI_DSI	MIPI_DSI_VDD18	-	10 kΩ resistor to ground.
MIPI_DSI	MIPI_DSI_VDDA_CAP	-	Leave unconnected.
MIPI_DSI	MIPI_DSI_VSS	-	Connect to ground.
MIPI_DSI	MIPI_DSI_D0N/D0P	-	Leave unconnected.
MIPI_DSI	MIPI_DSI_D1N/D1P	-	Leave unconnected.
MIPI_DSI	MIPI_DSI_CLKP	-	Leave unconnected.
MIPI_DSI	MIPI_DSI_CLKN	-	Leave unconnected.
Analog	VREFP	-	Connect to VDDA_ADC1V8.
Analog	VREFN	-	Connect to ground.
Power	VDDCORE	-	Connect to 1.0V power.
Power	VDD1V8	-	Connect to 1.8V power.
Power	VDD_1V8_1	-	Connect to 1.8V power during active. Can be powered off during deep sleep mode to reduce current consumption by approximately 22 uA.
Power	VDD_AO1V8	-	Connect to 1.8V power.
Power	VDDIO_n		Connect to 1.8V power.
Power	VDDA_ADC1V8	-	Connect to 1.8V power.
Power	VDDA_BIAS	-	Connect to 1.8V power.
Power	VSSA	-	Connect to ground.
Power	VSS	-	Connect to ground.

¹ Z = high impedance; I = Input; O = Output

4 Update the table “Power supply for pins”

Location: [Section 6, Table 52, Page 109](#)

Add the following rows to Table 52 “Power supply for pins”.

Pin	GPIO pins
VDDIO_0	PIO6_27 (Fail Safe Pad)
VDDIO_1	PIO5_4 and PIO5_8 (Fail Safe Pads)

Replace the following rows in Table 52 “Power supply for pins”, with the ones shown in the table.

VDDIO_1: PIO1_2 to PIO1_7 (Fail Safe Pads)

VDDIO_1: PIO1_10 (Fail Safe Pads)

VDDIO_3: PIO5_0 to PIO5_4, PIO5_8 (Fail Safe Pads)

Pin	GPIO pins
VDDIO_1	PIO1_3 to PIO1_7 (Fail Safe Pads) PIO1_9 to PIO1_10 (Fail Safe Pads)
VDDIO_3	PIO5_0 to PIO5_3 (Fail Safe Pads)

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Table continues on the next page...

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