SGM8604-1/SGM8604-2/SGM8604-3/SGM8604-5
15MHz, High Output Drive, High Precision, Low Noise Operational Amplifiers

GENERAL DESCRIPTION

The SGM8604-1 (single), SGM8604-3 (single with shutdown), SGM8604-2 (dual) and SGM8604-5 (dual with shutdown) are low noise, high precision CMOS operational amplifiers that provide a high output current of 232mA, rail-to-rail output operation from a range of 2.7V to 5.5V single supply. The SGM8604-3/5 are both available with shutdown pins that drive the output voltage low.

The SGM8604-1/2/3/5 offer low input offset voltage, low input offset voltage drift and high output current drive. These devices also can achieve a high 15MHz gain-bandwidth product and a high 7V/μs slew rate.

The SGM8604-1/2/3/5 are specifically designed to drive high current load, such as 32Ω headset, V_{BIAS} of RF power amplifier, etc.

The SGM8604-1/3 are available in a Green UTDFN-1.45×1-6L package. The SGM8604-2 is available in a Green TDFN-2×3-8AL package. The SGM8604-5 is available in a Green TDFN-3×3-10L package. They operate over an ambient temperature range of -40℃ to +125℃.

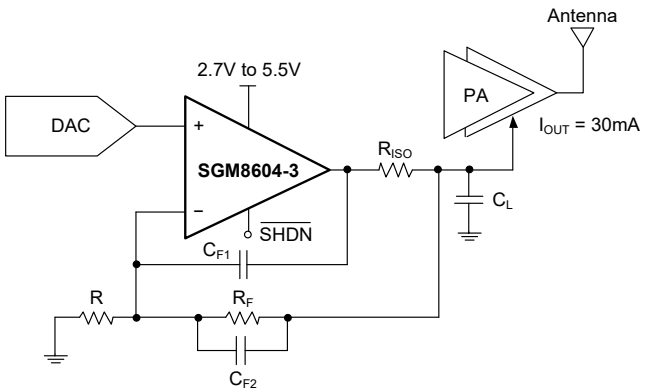
APPLICATIONS

V_{BIAS} of RF Power Amplifiers
Portable Stereo Headphone Drivers (32Ω)
Battery-Powered Equipment
Audio System
Optical Module
DAC Buffer
Industrial Equipment

FEATURES

- **Output Drive Capability: 232mA**
- **Low Input Offset Voltage: 10μV (MAX)**
- **Low Input Offset Voltage Drift: 17nV/℃ (TYP)**
- **Low Noise: 22nV/$\sqrt{Hz}$ at 1kHz**
- **Gain-Bandwidth Product: 15MHz**
- **High Slew Rate: 7V/μs**
- **High Open-Loop Gain (R_L = 2kΩ): 145dB**
- **Power Supply Rejection Ratio: 127dB**
- **Over-Temperature Protection**
- **No Phase Reversal for Overdriven Inputs**
- **Rail-to-Rail Input and Output**
- **Supply Voltage Range: 2.7V to 5.5V**
- **Quiescent Supply Current:**
  1.2mA/Amplifier (TYP)
  0.1μA/Amplifier (TYP) Shutdown Current for SGM8604-3/5
- **-40℃ to +125℃ Operating Temperature Range**
- **Small Packaging:**
  SGM8604-1 Available in a Green UTDFN-1.45×1-6L Package
  SGM8604-2 Available in a Green TDFN-2×3-8AL Package
  SGM8604-3 Available in a Green UTDFN-1.45×1-6L Package
  SGM8604-5 Available in a Green TDFN-3×3-10L Package

TYPICAL APPLICATION



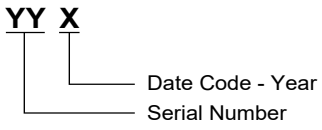
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8604-1	UTDFN-1.45×1-6L	-40℃ to +125℃	SGM8604-1XUDL6G/TR	D1X	Tape and Reel, 5000
SGM8604-2	TDFN-2×3-8AL	-40℃ to +125℃	SGM8604-2XTDC8G/TR	GD0 XXXX	Tape and Reel, 3000
SGM8604-3	UTDFN-1.45×1-6L	-40℃ to +125℃	SGM8604-3XUDL6G/TR	D2X	Tape and Reel, 5000
SGM8604-5	TDFN-3×3-10L	-40℃ to +125℃	SGM8604-5XTD10G/TR	SGM 86045D XXXXX	Tape and Reel, 4000

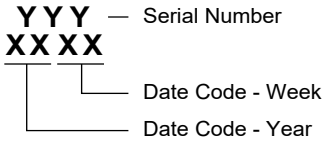
MARKING INFORMATION

NOTE: X = Date Code. XXXX = Date Code. XXXXX = Date Code and Vendor Code.

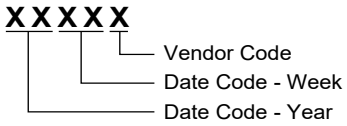
UTDFN-1.45×1-6L



TDFN-2×3-8AL



TDFN-3×3-10L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 6V
All Other Pins ..... ($-V_S$) - 0.3V to ($+V_S$) + 0.3V
Output Short-Circuit Duration to $+V_S$ or $-V_S$ 10s
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 7000V
MM 400V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃
Operating Supply Voltage Range ..... 2.7V to 5.5V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

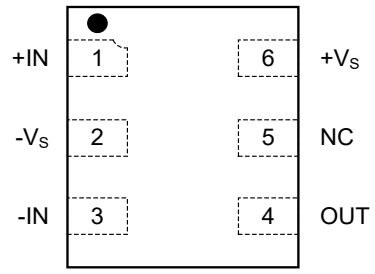
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

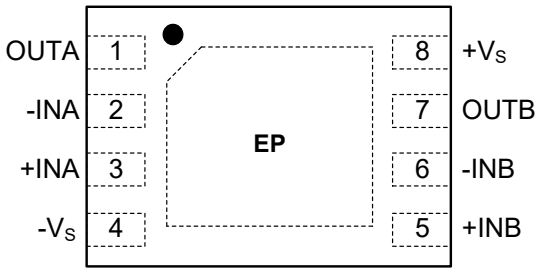
PIN CONFIGURATIONS

SGM8604-1 (TOP VIEW)



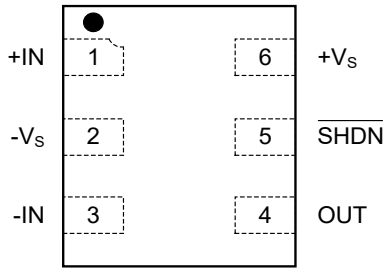
UTDFN-1.45×1-6L

SGM8604-2 (TOP VIEW)



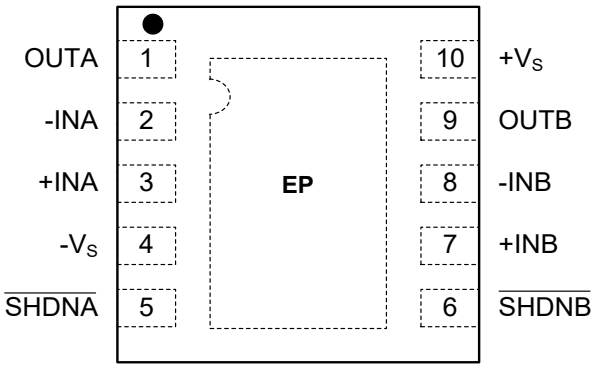
TDFN-2×3-8AL

SGM8604-3 (TOP VIEW)



UTDFN-1.45×1-6L

SGM8604-5 (TOP VIEW)



TDFN-3×3-10L

NOTE: For TDFN-2×3-8AL and TDFN-3×3-10L packages, the exposed pad must be connected to $-V_S$ or left floating. Connect it to $-V_S$ plane can maximize thermal performance.

ELECTRICAL CHARACTERISTICS

(At T_A = +25℃, Full = -40℃ to +125℃, V_S = 2.7V to 5V, $-V_S$ = 0V, V_{CM} = V_S/2, V_{OUT} = V_S/2, R_L = ∞ connected to V_S/2, $V_{\overline{SHDN}}$ = V_S, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Input Characteristics								
Input Offset Voltage	V_{OS}	V_S = 2.7V		+25℃		2.4	8	μV
		V_S = 5V		+25℃		2.4	10	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	V_S = 2.7V		Full		25	126	nV/℃
		V_S = 5V		Full		17	130	
Input Bias Current	I_B	V_S = 2.7V, V_{CM} = V_S/2		+25℃		50		pA
		V_S = 5V, V_{CM} = V_S/2		+25℃		200		
Input Offset Current	I_{OS}	V_S = 2.7V, V_{CM} = V_S/2		+25℃		50		pA
		V_S = 5V, V_{CM} = V_S/2		+25℃		200		
Input Common Mode Voltage Range	V_{CM}	Inferred from CMRR test		+25℃	$(-V_S)$ - 0.1		$(+V_S)$ + 0.1	V
Common Mode Rejection Ratio	CMRR	V_S = 2.7V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ + 0.1V		+25℃	104	120		dB
				Full	100			
		V_S = 5V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ + 0.1V		+25℃	108	120		
				Full	90			
Large Signal Voltage Gain	A_{VOL}	V_S = 2.7V, $(-V_S)$ + 0.2V < V_{OUT} < $(+V_S)$ - 0.2V	R_L = 2kΩ	+25℃	112	145		dB
				Full	110			
			R_L = 200Ω	+25℃	109	142		
				Full	106			
		V_S = 5V, $(-V_S)$ + 0.2V < V_{OUT} < $(+V_S)$ - 0.2V	R_L = 2kΩ	+25℃	115	145		
				Full	112			
			R_L = 200Ω	+25℃	110	145		
				Full	108			
Output Characteristics								
Output Voltage Swing from Rail	V_{OUT}	V_S = 2.7V	R_L = 32Ω	+25℃		245	300	mV
				Full			370	
			R_L = 200Ω	+25℃		45	60	
				Full			73	
			R_L = 2kΩ	+25℃		5	10	
				Full			12	
			I_{OUT} = 10mA	+25℃		62	100	
				Full			122	
		V_S = 5V	R_L = 32Ω	+25℃		400	485	mV
				Full			585	
			R_L = 200Ω	+25℃		72	95	
				Full			113	
			R_L = 2kΩ	+25℃		8	15	
				Full			18	
			I_{OUT} = 10mA	+25℃		62	85	
				Full			102	
Short Circuit Current Limit	I_{SC}	V_S = 2.7V		+25℃	85	120		mA
				Full	58			
		V_S = 5V		+25℃	185	240		
				Full	154			

ELECTRICAL CHARACTERISTICS (continued)

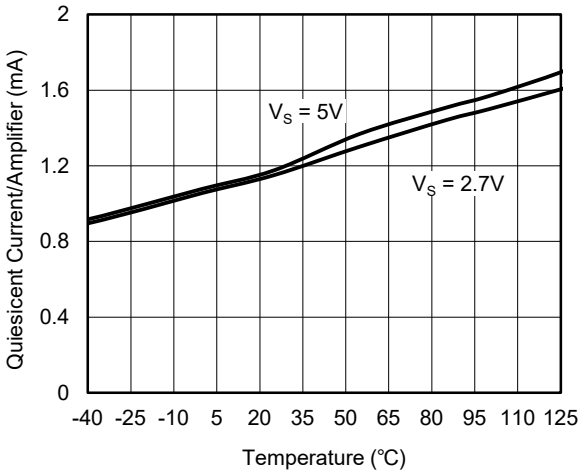
(At T_A = +25℃, Full = -40℃ to +125℃, V_S = 2.7V to 5V, $-V_S$ = 0V, V_{CM} = V_S/2, V_{OUT} = V_S/2, R_L = ∞ connected to V_S/2, $V_{\overline{SHDN}}$ = V_S, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Power-Down Disable (SGM8604-3/5 Only)							
Shutdown Supply Current/Amplifier	$I_{Q(\overline{SHDN})}$	$V_{\overline{SHDN}}$ = 0V, R_L = ∞	+25℃		0.1	2.5	μA
$\overline{SHDN}$ Logic Threshold	V_{IL}	Shutdown mode	+25℃			0.5	V
	V_{IH}	Normal mode	+25℃	1.6			
$\overline{SHDN}$ Input Bias Current		$-V_S < V_{\overline{SHDN}} < V_S$	+25℃		50		pA
Shutdown Output Impedance	R_{OUT}	$V_{\overline{SHDN}}$ = 0V	+25℃		10		Ω
Output Voltage in Shutdown	$V_{OUT(\overline{SHDN})}$	$V_{\overline{SHDN}}$ = 0V, R_L = 200Ω	+25℃		10		mV
Shutdown Time	$t_{\overline{SHDN}}$		+25℃		7		μs
Enable Delay Time	t_{ENABLE}		+25℃		10		μs
Power Supply							
Supply Voltage Range	V_S	Inferred from PSRR test	+25℃	2.7		5.5	V
Power Supply Rejection Ratio	PSRR		+25℃	102	127		dB
			Full	94			
Quiescent Supply Current/Amplifier	I_Q	V_S = 2.7V, V_{CM} = V_S/2	+25℃		1.1	1.55	mA
		V_S = 5V, V_{CM} = V_S/2	+25℃		1.2	1.6	
			Full			2.1	
Dynamic Performance							
Gain-Bandwidth Product	GBP	V_{CM} = V_S/2	+25℃		15		MHz
Slew Rate	SR		+25℃		7		V/μs
Total Harmonic Distortion + Noise	THD+N	V_S = 5V, R_L = 32Ω, f = 10kHz, V_{OUT} = $2V_{P-P}$, A_{VCL} = 1V/V	+25℃		0.008		%
Input Capacitance	C_{IN}		+25℃		20		pF
Channel-to-Channel Isolation		f = 1kHz, R_L = 100kΩ	+25℃		-125		dB
Capacitive-Load Stability		A_{VCL} = 1V/V, no sustained oscillations	+25℃		780		pF
Power-Up Time	t_{ON}		+25℃		50		μs
Noise Performance							
Input Voltage Noise Density	e_n	f = 1kHz	+25℃		22		$nV/\sqrt{Hz}$
		f = 10kHz	+25℃		20		
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		0.5		$μV_{P-P}$

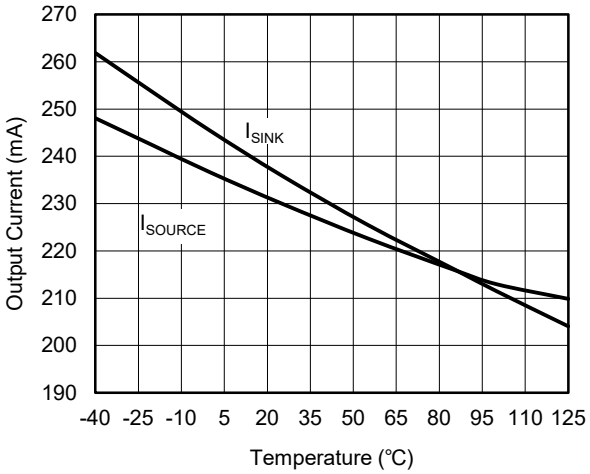
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = 5.0V, unless otherwise noted.

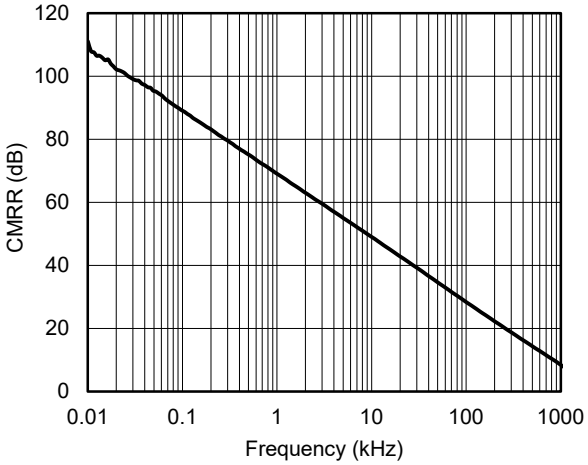
Quiescent Current vs. Temperature



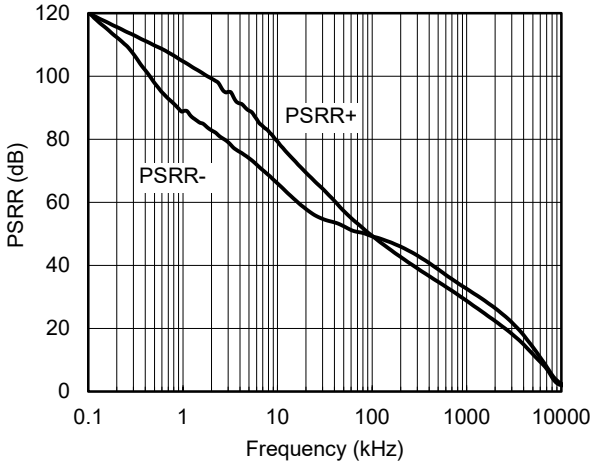
Output Current vs. Temperature



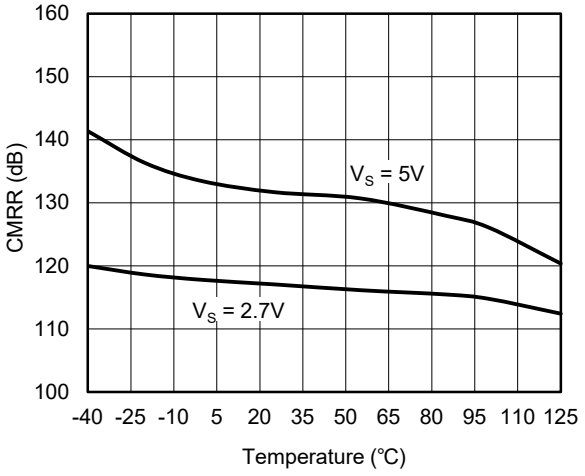
Common Mode Rejection Ratio vs. Frequency



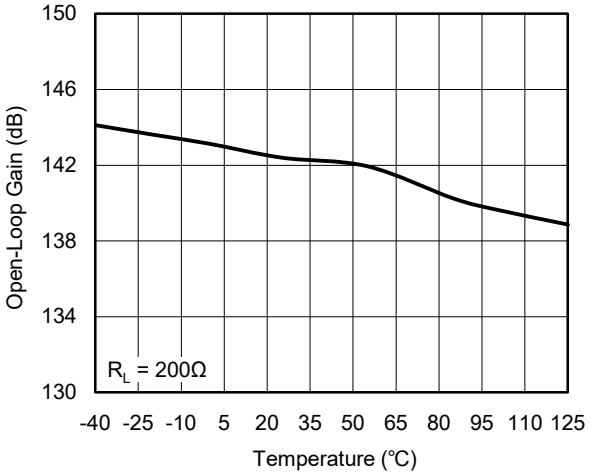
Power Supply Rejection Ratio vs. Frequency



Common Mode Rejection Ratio vs. Temperature



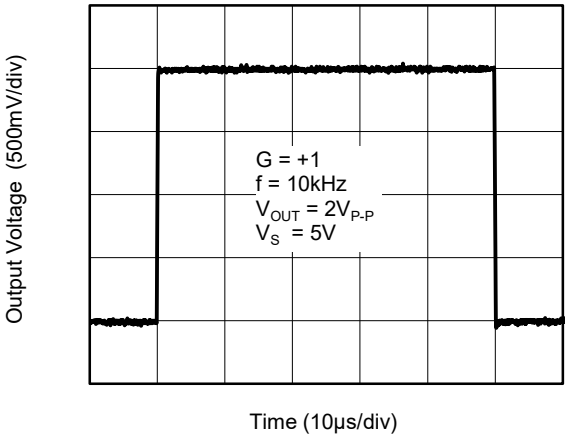
Open-Loop Gain vs. Temperature



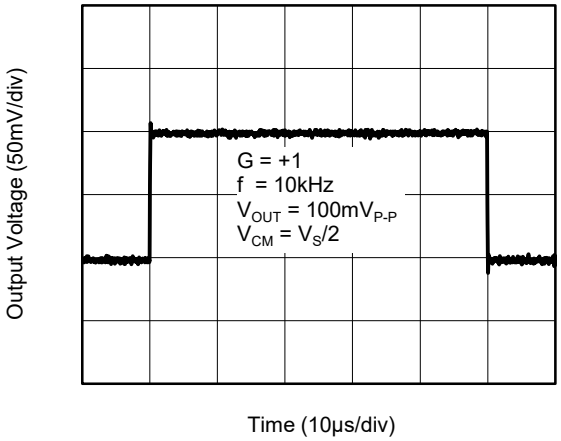
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 5.0V, unless otherwise noted.

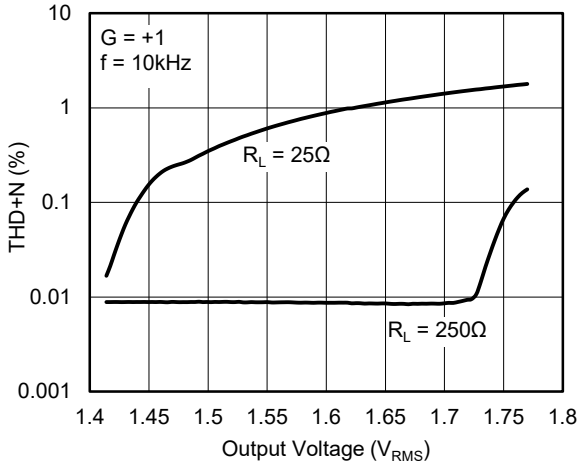
Large Signal Step Response



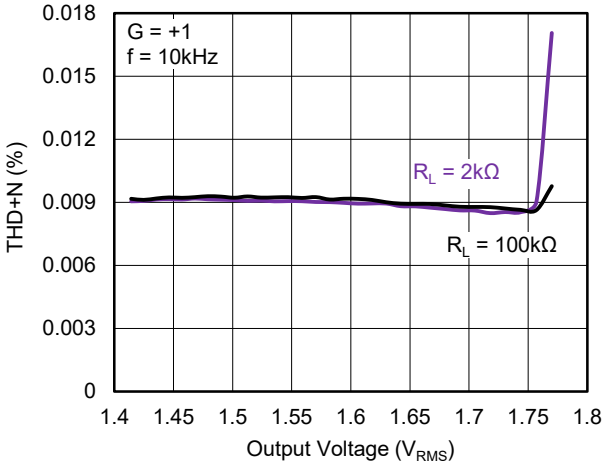
Small Signal Step Response



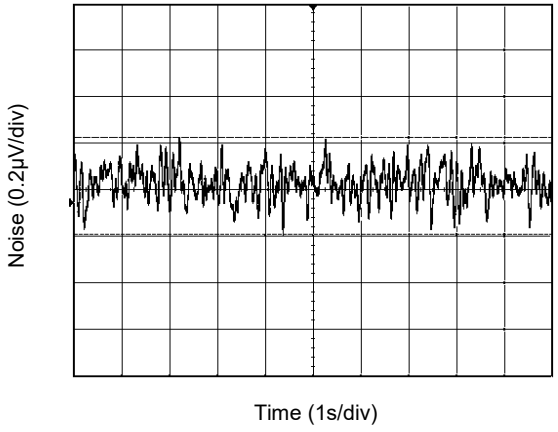
THD+N vs. Output Voltage



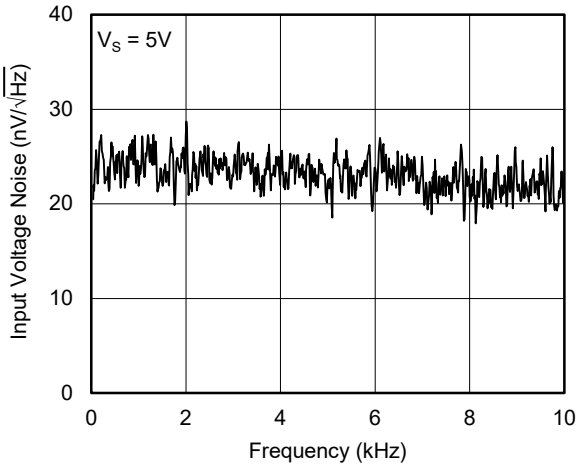
THD+N vs. Output Voltage



0.1Hz to 10Hz Noise



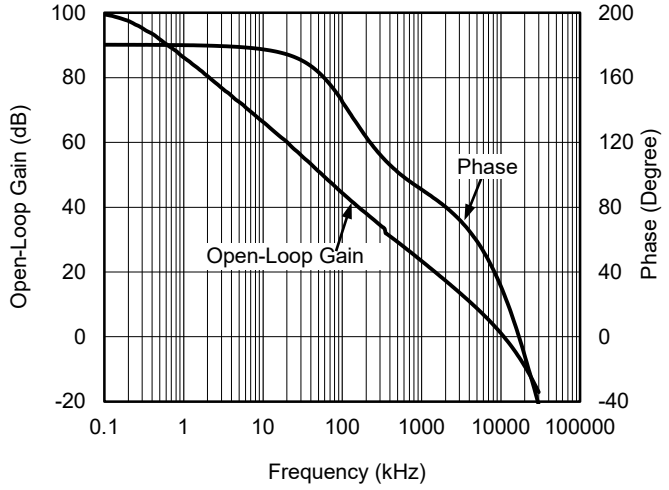
Input Voltage Noise Density



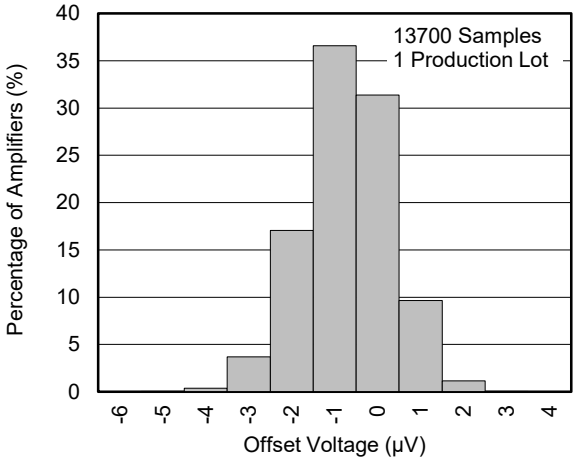
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 5.0V, unless otherwise noted.

Open-Loop Gain and Phase vs. Frequency



Offset Voltage Production Distribution



APPLICATION INFORMATION

Single-Supply Stereo Headphone Driver

A single-supply stereo headphone driver is shown in Figure 1 as an example to explain the simplified design procedure.

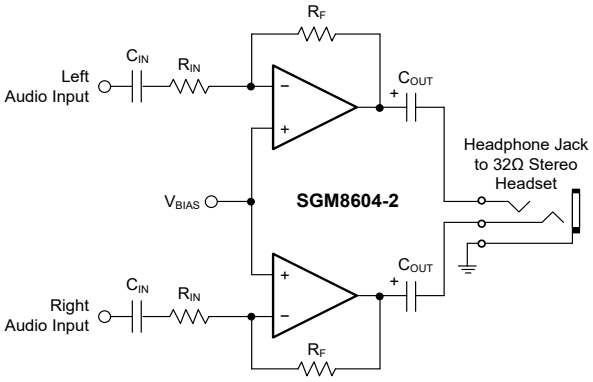


Figure 1. Stereo Headphone Driver

In this circuit, C_{IN} and R_{IN} form a high-pass filter, the DC bias is removed from the incoming signal. The -3dB point of the high-pass filter is using Equation 1:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}} \quad (1)$$

The gain of driver is $-R_F/R_{IN}$. The C_{OUT} and the load impedance form a high-pass filter with the -3dB point determined by Equation 2:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}} \quad (2)$$

Bridge Amplifier

A bridge amplifier circuit which can provide 200mW at 3V is shown in Figure 2. Due to differential output, this structure eliminates the large coupling capacitors in Figure 1. The voltage gain is 10V/V and the gain can be changed by changing R_2.

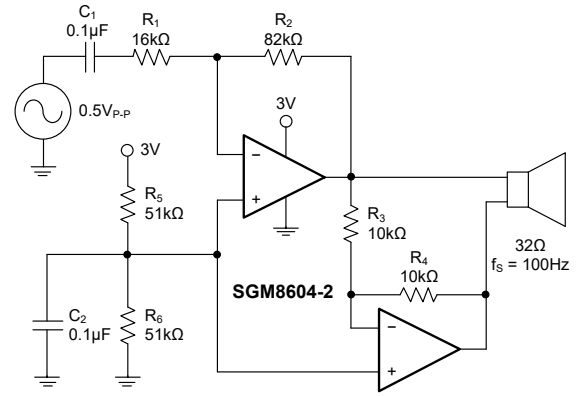


Figure 2. 200mW Bridge Amplifier at 3V

Cancel Input Capacitance

The C_{IN} (20pF TYP) at inverting input pin will generate a pole at frequency $(2\pi R'C_{IN})^{-1}$, where R′ is the parallel combination of the gain-setting resistor for the inverting or non-inverting amplifier in Figure 3. If the pole-frequency is less than or comparable to the unity-gain bandwidth (15MHz), the phase margin will be reduced, ringing in the step response or sustained oscillation will be generated. To cancel this pole, C_F is used to compensate C_{IN} in Figure 3. Equation 3 gives the C_F feedback capacitance.

$$C_F = 8\times(R/R_F)\ pF \quad (3)$$

where:

R_F is the feedback resistor.
R is the gain-setting resistor.

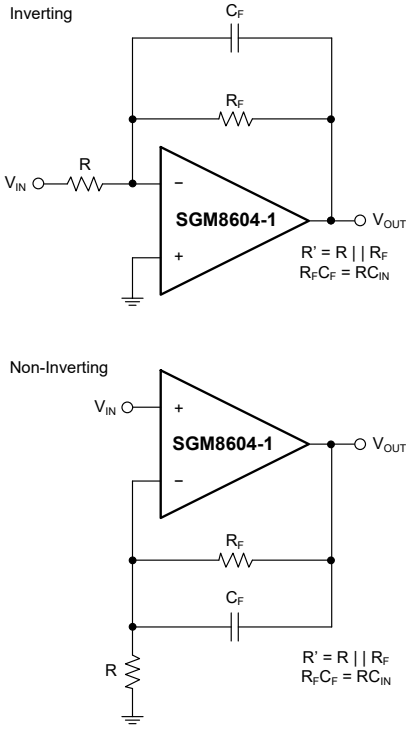


Figure 3. Inverting and Non-Inverting Amplifiers with C_F to Compensate C_{IN}

APPLICATIONS INFORMATION (continued)

Input Current-Limit Protection

For ESD diode clamping protection, when the current flowing through ESD diode exceeds the maximum rating value, the ESD diode and amplifier will be damaged, so current-limit protection will be added in some applications. One resistor is selected to limit the current not to exceed the maximum rating value. In Figure 4, a series input resistor is used to limit the input current to less than 10mA, but the drawback of this current-limit resistor is to contribute thermal noise at the amplifier input. If this resistor must be added, its value must be selected as small as possible.

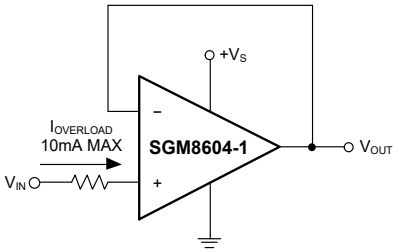


Figure 4. Input Current-Limit Protection

Rail-to-Rail Output

The SGM8604-1/2/3/5 support rail-to-rail output operation. In single power supply application, for example, when $+V_S$ = 5V, $-V_S$ = GND, 2kΩ load resistor is tied from OUT pin to V_S/2, the typical output swing range is from 0.008V to 4.992V.

Driving Capacitive Loads

The SGM8604-1/2/3/5 are designed for unity-gain stable for capacitive load up to 780pF. In Figure 5, it shows the transient response with capacitive load (C_L). If greater capacitive load must be driven in application, the circuit in Figure 6 can be used. In this circuit, the IR drop voltage generated by R_{ISO} is compensated by feedback loop.

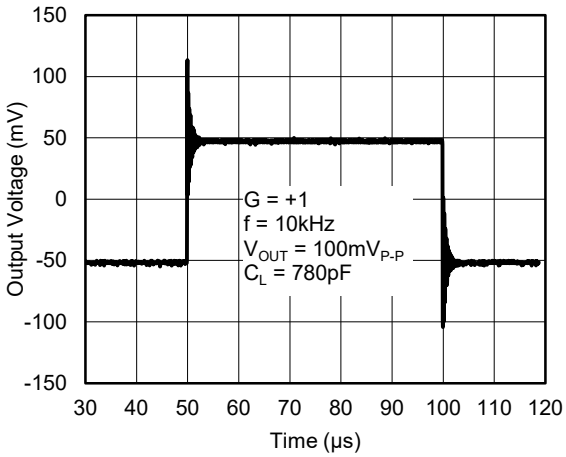


Figure 5. Small-Signal Transient Response (Capacitive Load)

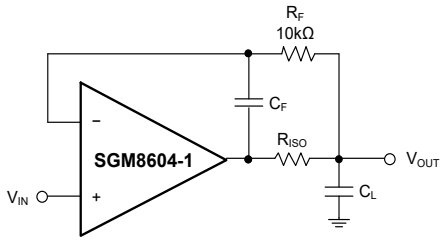


Figure 6. Circuit to Drive Capacitive Load

APPLICATIONS INFORMATION (continued)

Shutdown Mode and Power-Up

The SGM8604-3 and SGM8604-5 are disabled when the shutdown pin is pulled low. To disable the amplifier, the shutdown supply current drops to 0.1μA (TYP) per amplifier. When in shutdown mode the operational amplifier output is driven to $-V_S$. Pull the shutdown pin high to enable the amplifier. Figure 7 shows the output voltage to a shutdown pulse. The SGM8604-3/5 typically settle within 50μs after power-up.

When exiting shutdown mode, a 10μs delay-time can be added before the amplifier's output become active (Figure 7).

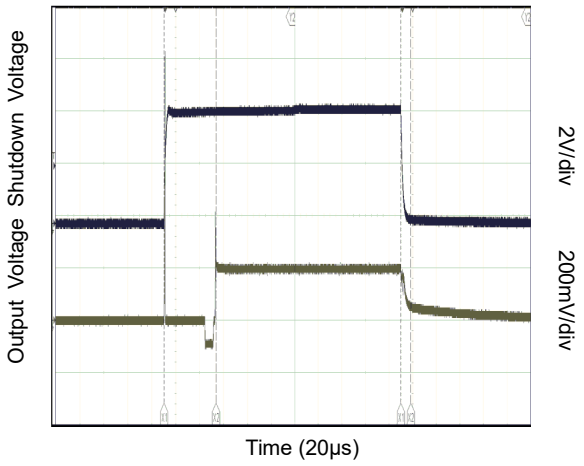


Figure 7. Enable or Disable the Output Voltage

Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design, besides of input signal noise, the power supply is one of important source of noise to the amplifiers through $+V_S$ and $-V_S$ pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, 10μF ceramic capacitor paralleled with 0.1μF or 0.01μF ceramic capacitor is used in Figure 8. The ceramic capacitors should be placed as close as possible to $+V_S$ and $-V_S$ power supply pins.

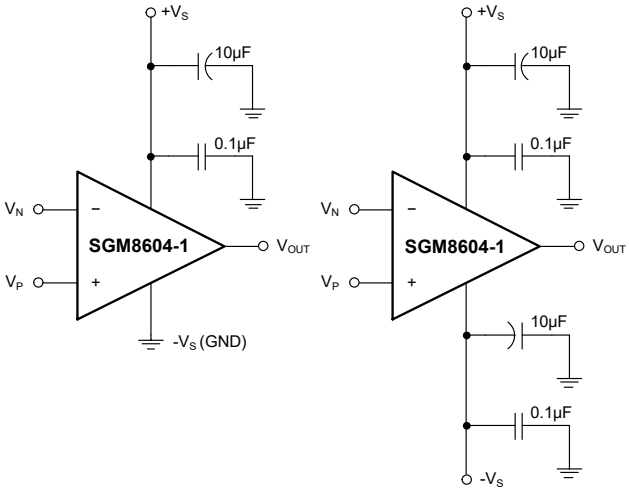


Figure 8. Amplifier Power Supply Bypassing

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2019 – REV.A.2 to REV.A.3	Page
Changed Figure 2	9

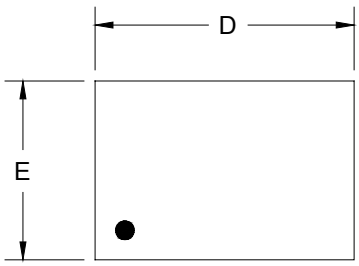
APRIL 2018 – REV.A.1 to REV.A.2	Page
Changed Package/Ordering Information section	2

NOVEMBER 2017 – REV.A to REV.A.1	Page
Changed Electrical Characteristics section	4
Changed Typical Performance Characteristics section	7, 8

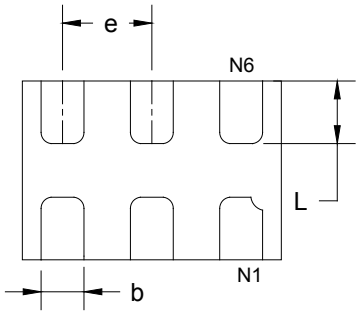
Changes from Original (DECEMBER 2016) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

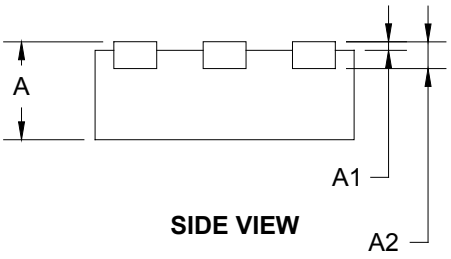
UTDFN-1.45×1-6L



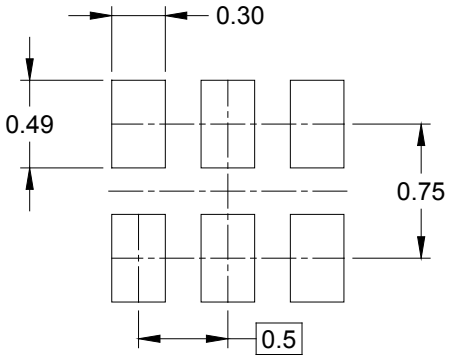
TOP VIEW



BOTTOM VIEW



SIDE VIEW

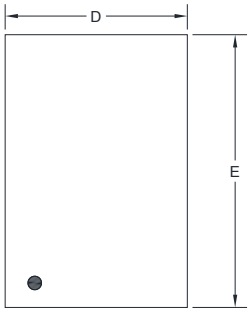


RECOMMENDED LAND PATTERN (Unit: mm)

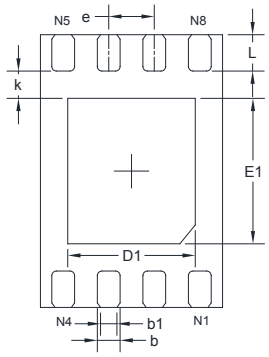
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A2	0.150 REF		0.006 REF	
D	1.374	1.526	0.054	0.060
E	0.924	1.076	0.036	0.042
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.274	0.426	0.011	0.017

PACKAGE OUTLINE DIMENSIONS

TDFN-2×3-8AL

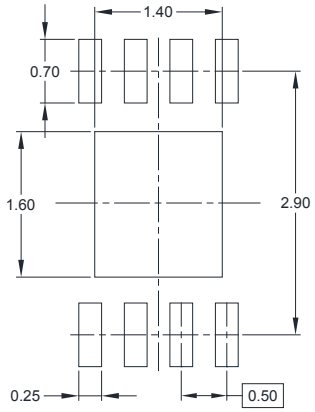


TOP VIEW



BOTTOM VIEW

SIDE VIEW

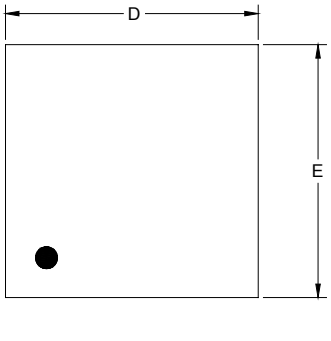


RECOMMENDED LAND PATTERN (Unit: mm)

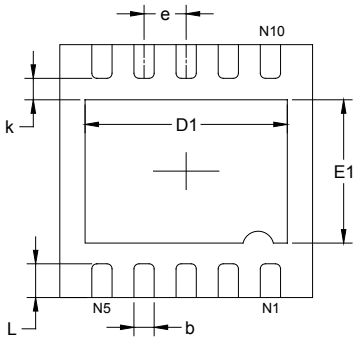
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.300	1.500	0.051	0.059
E	2.900	3.100	0.114	0.122
E1	1.500	1.700	0.059	0.067
k	0.300 REF		0.012 REF	
b	0.200	0.300	0.008	0.012
b1	0.180 REF		0.007 REF	
e	0.500 BSC		0.020 BSC	
L	0.300	0.500	0.012	0.020

PACKAGE OUTLINE DIMENSIONS

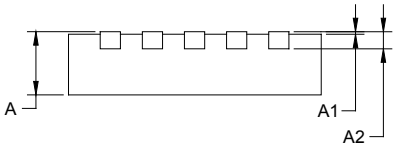
TDFN-3×3-10L



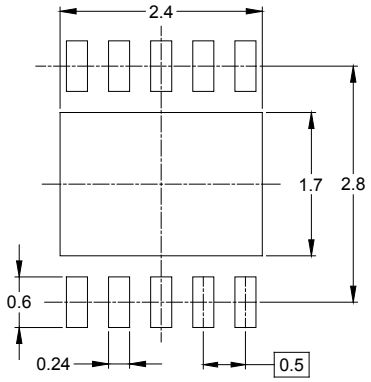
TOP VIEW



BOTTOM VIEW



SIDE VIEW

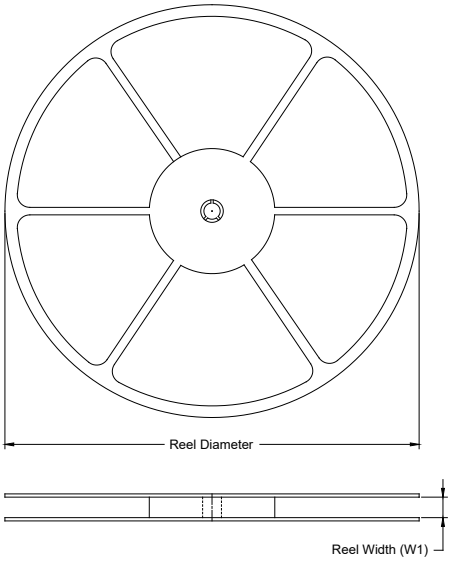


RECOMMENDED LAND PATTERN (Unit: mm)

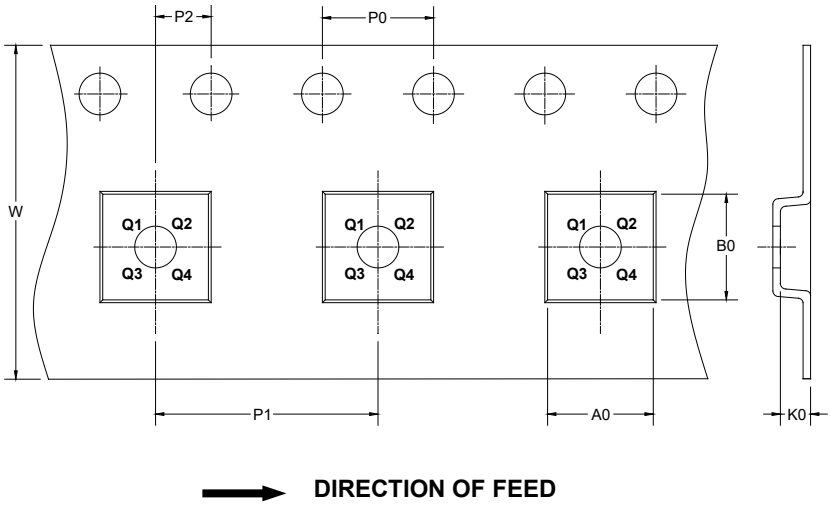
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



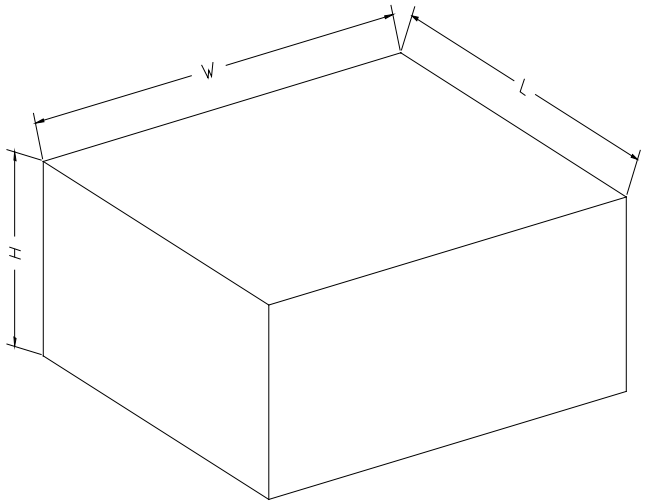
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.45×1-6L	7″	9.5	1.15	1.60	0.75	4.0	4.0	2.0	8.0	Q1
TDFN-2×3-8AL	7″	9.5	2.30	3.30	1.10	4.0	4.0	2.0	8.0	Q2
TDFN-3×3-10L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002