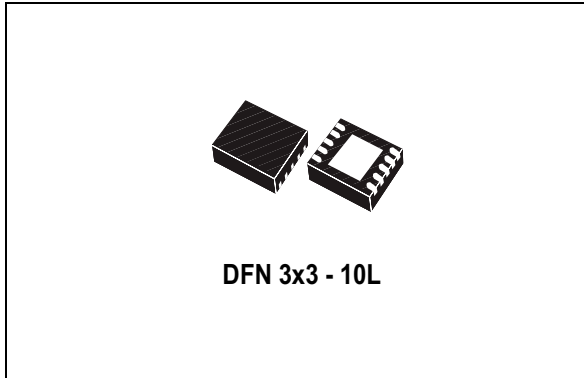


## Electronic fuse for 3.3 V and 5 V lines

Datasheet - production data



### Features

- Power MOSFET on-resistance (typ.): 40 mΩ
- Enable function
- Output clamp voltage (typ.): 5.7 V in 5 V mode, and 3.8 V in 3.3 V mode
- Undervoltage lockout
- Short-circuit limit
- Overload foldback current limit
- Controlled soft-start
- Thermal auto-retry
- Internal sensing FET
- Operative temp. range: - 40 °C to 85 °C
- Available in DFN 3x3 10L package

### Description

The STEF4S is an integrated electronic fuse optimized for monitoring the output current and the input voltage. It can be connected in series to 3.3 V or 5 V rails, protecting the electronic circuitry on its output from overcurrent and overvoltage. The operating mode (5 V or 3.3 V) can be selected by a dedicated pin. The STEF4S has a controlled turn-on time, adjustable by an external capacitor. When an overload condition occurs the device limits the output current to a

predefined safe value. If the anomalous overload condition persists it goes into an open state, disconnecting the load from the power supply. If a continuous short-circuit is present on the board, the E-fuse limits the output current to a safe value.

In case of overvoltage on the input, the device clamps the output voltage to a predefined value and protects the load.

If the anomalous fault condition persists, the internal thermal protection circuit shuts down the device and then automatically attempts to re-supply the load until the fault condition is removed.

Unlike mechanical fuses, which must be physically replaced after a single event, the E-fuse does not degrade in its performance after short-circuit/thermal protection interventions.

### Applications

- Hard disk drives
- Solid state drives (SSD)
- Hard disk and SSD arrays
- Set-top boxes
- DVD and blu-ray disc drivers

Table 1. Device summary

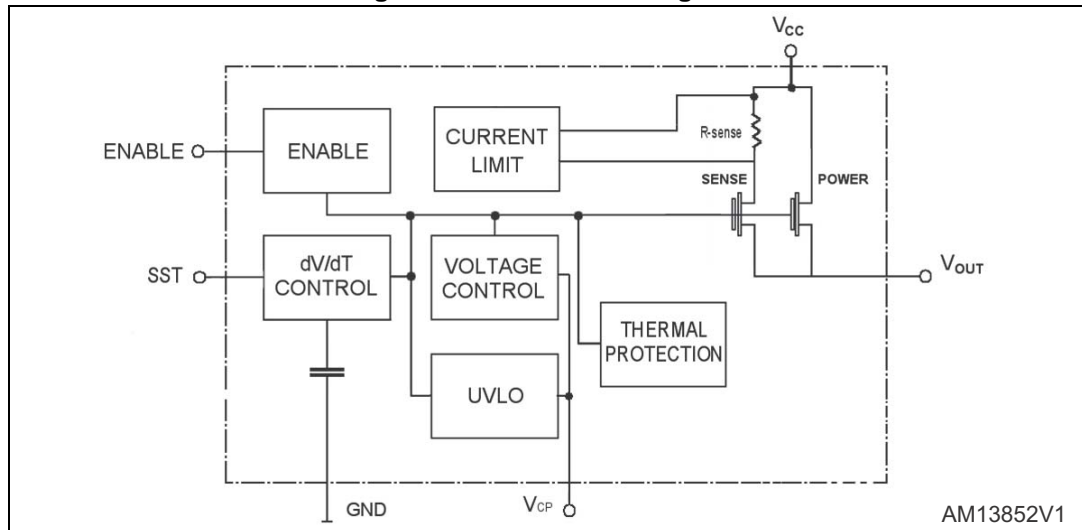
Order code	Package	Packing
STEF4SPUR	DFN 3x3 - 10L	Tape and reel

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# 1 Block diagram

Figure 1. Device block diagram



## 2 Pin configuration

Figure 2. Pin configuration (top view)

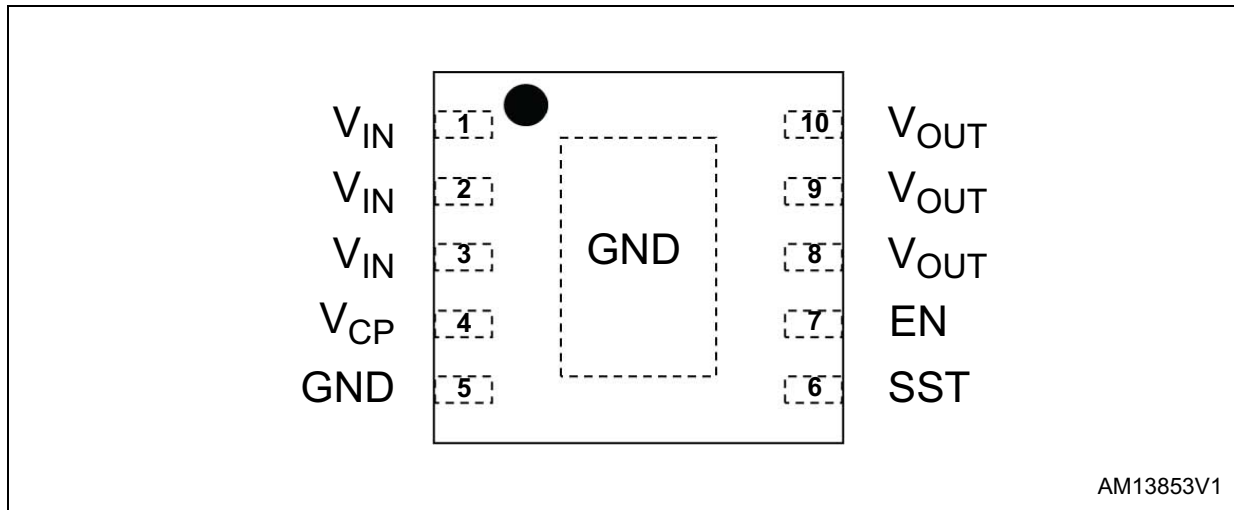


Table 2. Pin description

Pin n°	Symbol	Note
1, 2, 3	$V_{IN}$	Input supply voltage pin
4	$V_{CP}$	Voltage clamping and UVLO selection pin (high state 5 V, low state 3.3 V)
5	GND	Ground pin (can be left floating if TAB is connected to GND)
6	SST	Soft-start time selection pin. A capacitor can be connected between this pin and GND to increase the startup time
7	EN	Enable pin (active high)
8,9,10	$V_{OUT}$	Output voltage pin
EXP	GND	Exposed pad is internally connected to GND

### 3 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{IN}$	Positive power supply voltage	-0.3 to 15	V
$V_{OUT}$	Output voltage	-0.3 to 7	V
$V_{CP}$	UVLO and voltage clamp selection pin	-0.3 to $V_{IN}$	V
EN	Enable pin	-0.3 to $V_{IN}$	V
SST	Soft-start time selection pin	-0.3 to 4.6	V
$T_J$	Max. junction temperature <sup>(1)</sup>	-40 to 125	°C
$T_{STG}$	Storage temperature range	-65 to 150	°C
$T_{LEAD}$	Lead temperature (soldering) 10 s	260	°C

1. The thermal limit is set above the maximum thermal rating. It is not recommended the device to operate at temperatures greater than the maximum ratings for extended periods of time.

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}$	Thermal resistance junction-ambient	40	°C/W
$R_{thJC}$	Thermal resistance junction-case	2.5	°C/W

## 4 Electrical characteristics

Unless otherwise specified, typical values are referred to  $V_{IN} = 5\text{ V}$  for  $V_{CP} = V_{IN}$  and  $V_{IN} = 3.3\text{ V}$  for  $V_{CP} = \text{GND}$ ,  $C_{IN} = C_{OUT} = 22\text{ }\mu\text{F}$ ,  $T = 25\text{ }^\circ\text{C}$ , min. and max. values are referred to  $T = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ .

**Table 5. STEF4S electrical characteristic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operating input voltage				10	V
Under/overvoltage protection, 3.3 V mode						
$V_{Clamp}$	Output clamping voltage	$V_{IN} = 10\text{ V}$ , $V_{CP} = \text{GND}$	3.6	3.8	4.0	V
$V_{UVLO}$	Under voltage lockout	$V_{CP} = \text{GND}$ , Turn-on, voltage going up	2.2	2.3	2.4	V
$V_{Hyst}$	UVLO hysteresis	$V_{CP} = \text{GND}$	50	90	130	mV
Under/overvoltage protection, 5 V mode						
$V_{Clamp}$	Output clamping voltage	$V_{IN} = 10\text{ V}$ , $V_{CP} = V_{IN}$	5.4	5.7	6.0	V
$V_{UVLO}$	Under voltage lockout	$V_{CP} = V_{IN}$ , Turn-on, voltage going up	3.4	3.6	3.8	V
$V_{Hyst}$	UVLO hysteresis	$V_{CP} = V_{IN}$	60	105	150	mV
Power MOSFET						
$R_{DS(on)}$	ON-resistance $R_{DS(on)} = (V_{IN} - V_{OUT})/I_{OUT}$			40		m $\Omega$
		$T_j = 85\text{ }^\circ\text{C}^{(1)}$			70	
Current limit						
$I_{OL}$	Protection trip current			5		A
$I_{Lim}$	Overload current limit		5	7	9	A
$I_{Short}$	Short-circuit current limit	$V_{OUT} = 0\text{ V}$		3		A
Soft-start circuit						
$T_{SS}$	Output voltage ramp time	From $V_{IN} = V_{UVLO}$ to $V_{OUT} = 90\%$ , no $C_{SS}$		0.6		ms
		From $V_{IN} = V_{UVLO}$ to $V_{OUT} = 90\%$ , $C_{SS} = 100\text{ nF}$	16	23	30	
Enable pin thresholds						
$V_{EN-L}$	Enable pin switch-off voltage	Output disabled			0.4	V
$V_{EN-H}$	Enable pin switch-on voltage	Output enabled	2			V
$V_{CP}$ pin thresholds						
$V_{CP-L}$	3.3 V mode selection threshold	3.3 V mode enabled			0.4	V
$V_{CP-H}$	5 V mode selection threshold	5 V mode enabled	2			V
Total device						

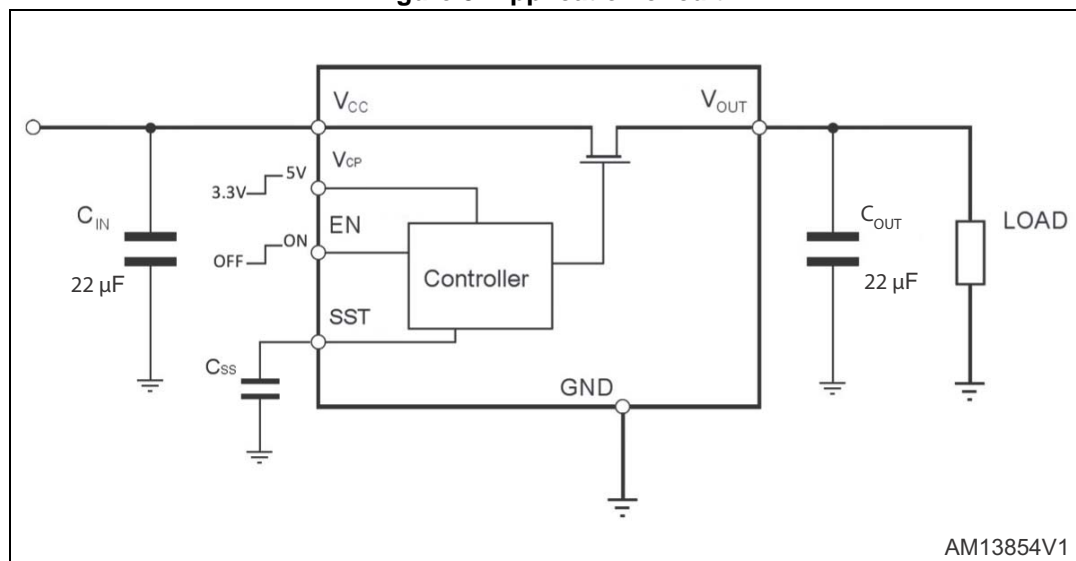
Table 5. STEF4S electrical characteristic (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{\text{Bias}}$	Bias current	ON state, $V_{\text{EN}} = V_{\text{IN}} = 5 \text{ V}$		50	65	$\mu\text{A}$
		OFF state, $V_{\text{EN}} = \text{GND}$ , $V_{\text{IN}} = 5 \text{ V}$		15		
$V_{\text{min}}$	Minimum operating voltage	Device is in OFF state ( $V_{\text{OUT}} = 0$ )	2			V
Thermal latch						
TSD	Shutdown temperature			140		$^{\circ}\text{C}$
	Hysteresis			20		

1. Guaranteed by design, not tested in production.

## 5 Typical characteristics

Figure 3. Application circuit





## 5.1 Operating modes

### 5.1.1 Turn-on

When the input voltage is applied and the EN pin is high, the output voltage is supplied with a slope defined by the internal dv/dt circuitry. If no additional capacitor is connected to C<sub>SS</sub> pin, the total time from the enable signal going high and the output voltage reaching the nominal value is around 0.6 ms.

### 5.1.2 Normal operating condition

The STEF4S E-fuse behaves like a mechanical fuse, buffering the circuitry on its output with the same voltage shown at its input, apart from a small voltage fall due to the MOSFET R<sub>DS(on)</sub>.

### 5.1.3 Output voltage clamp

The internal voltage clamp circuit clamps the output voltage to the V<sub>Clamp</sub> values reported in [Table 5](#) if the input voltage exceeds the typical thresholds of 3.8 V in the 3.3 V mode and 5.7 V in the 5 V mode.

### 5.1.4 Current limiting

When an overload event occurs, the current limiting circuit reduces the conductivity of the power MOSFET, in order to clamp the input current at the pre-programmed value. The current limit circuit has a foldback characteristic to reduce the power dissipation over the power MOSFET in short-circuit condition.

### 5.1.5 Thermal shutdown and auto-retry function

If the device temperature exceeds the thermal shutdown threshold, typically 140 °C, the thermal shutdown circuitry turns the power MOSFET off and disconnects the load. Once the die temperature has decreased about 20 °C the device automatically attempts to apply again the power to the load (auto-retry). This cycle persists until the fault condition is removed.

## 5.2 Startup time and C<sub>SS</sub> calculation

Connecting a capacitor between the C<sub>SS</sub> pin and GND allows the modification of the output voltage startup time. The startup time (T<sub>SS</sub>) is defined as the time interval between the device UVLO threshold, which has been overcome, and V<sub>OUT</sub>, which has reached 90% of the nominal value as shown in [Figure 4](#).

The below [Table 6](#) shows the typical startup time obtained with the industry-standard values of C<sub>SS</sub>.

**Table 6. Startup time vs. C<sub>SS</sub> capacitor value**

Parameter	Value			
C <sub>SS</sub> [nF]	None	10	47	100
T <sub>SS</sub> [ms]	0.6	2.3	10.8	23

The capacitance to be added to C<sub>SS</sub> pin can be also estimated by using the following theoretical formula:

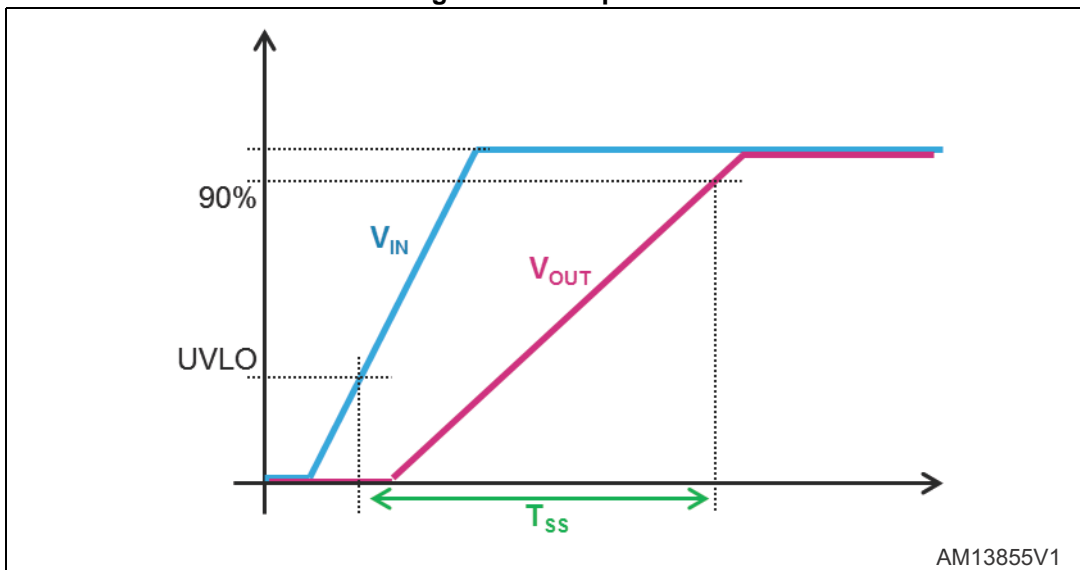
**Equation 1**

$$C_{SS} = 4.35 \times 10^{-6} \times T_{SS}$$

The above value is not valid if C<sub>SS</sub> is not connected. C<sub>SS</sub> is expressed in Farad and the time in seconds.

A ceramic low leakage capacitor is suggested for this purpose. The formula is meant as a theoretical support to choose the C<sub>SS</sub> capacitor and it does not take into account the capacitor tolerance, temperature and process variations.

**Figure 4. Startup time**



**5.3 UVLO and voltage clamp selection**

The device can be used either on the 3.3 V or on the 5 V lines. The operating mode can be selected through the V<sub>CP</sub> pin.

If this pin is set at high level (V<sub>CP</sub> > 2 V) the operating mode is 5 V. In this mode the UVLO threshold is 3.6 V typical, the clamping voltage is set to 5.7 V.

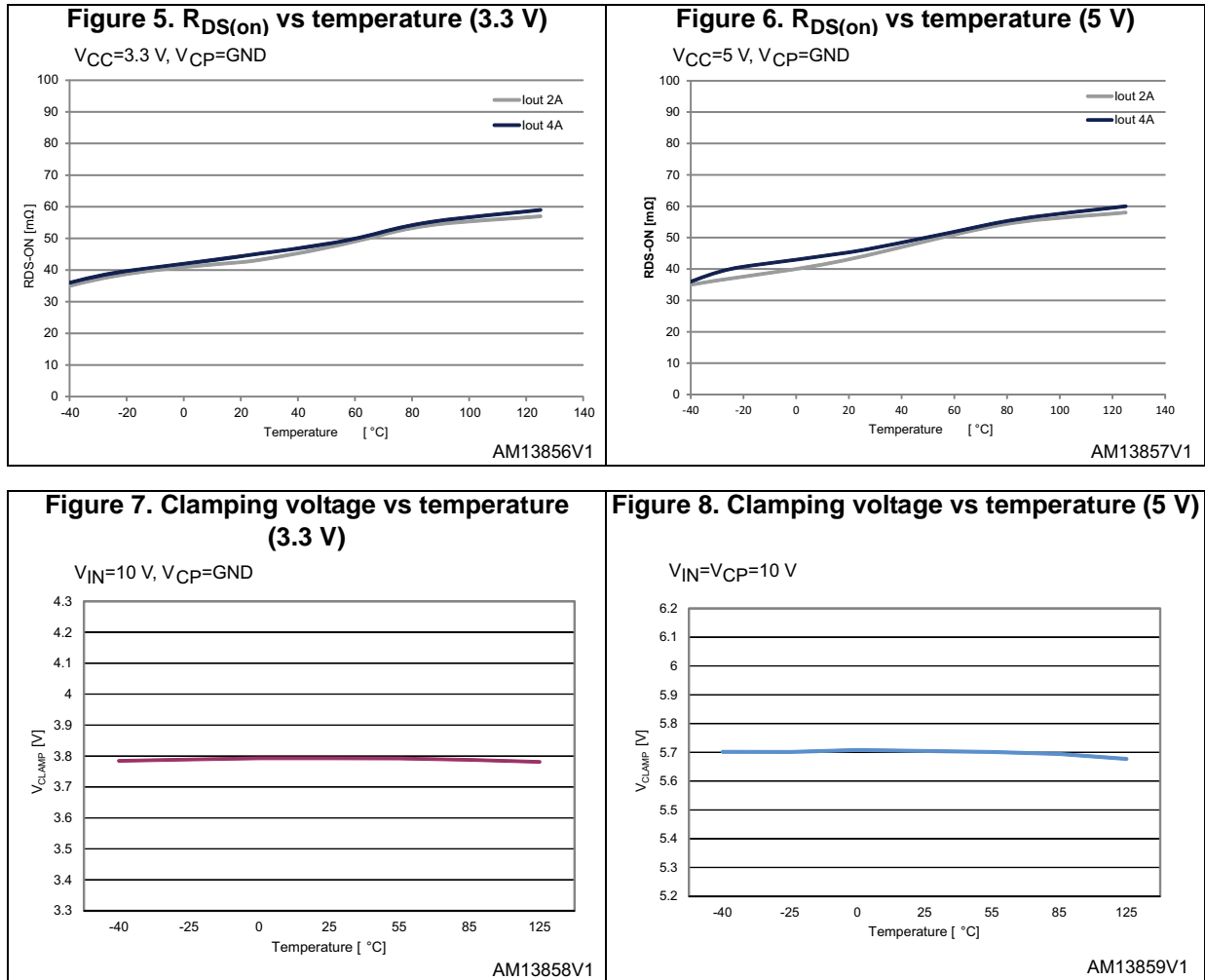
If the V<sub>CP</sub> pin is pulled to low level (V<sub>CP</sub> < 0.4 V), the operating mode is 3.3 V. In this mode the UVLO threshold is 2.3 V typical, the clamping voltage is set to 3.8 V.

**5.4 Enable pin**

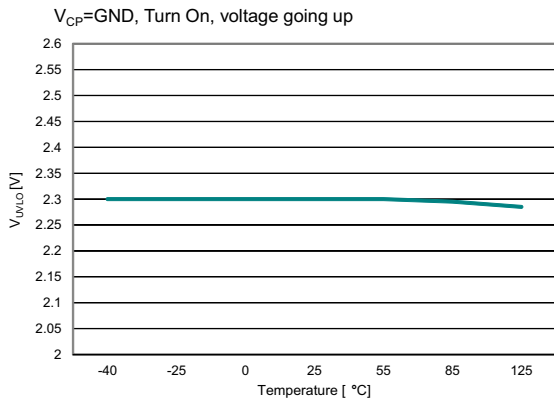
The EN pin is used to turn on/off the device. The device is disabled when the EN pin voltage is lower than 0.4 V, enabled if the EN pin voltage is higher than 2 V.

## 6 Typical performance characteristics

(The following plots are referred to the typical application circuit and, unless otherwise noted, at  $T_A = 25\text{ }^\circ\text{C}$ )

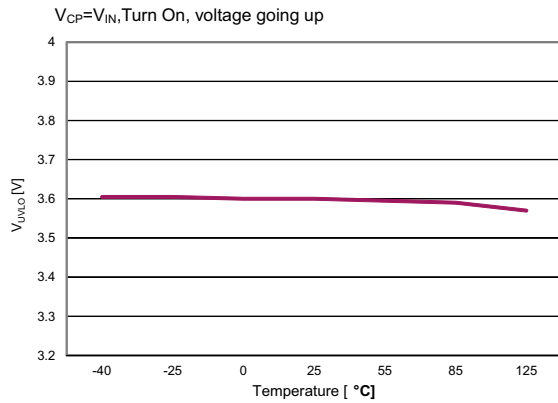


**Figure 9. UVLO threshold vs temperature (3.3 V)**



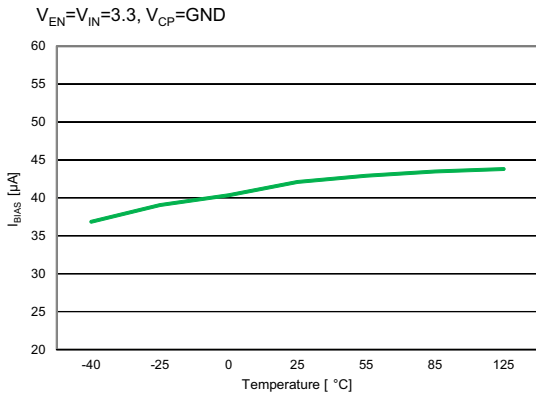
AM13861V1

**Figure 10. UVLO threshold vs temperature (5 V)**



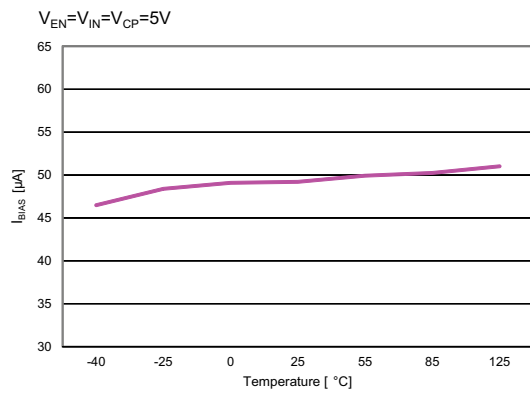
AM13860V1

**Figure 11. Bias current vs temperature (3.3 V)**



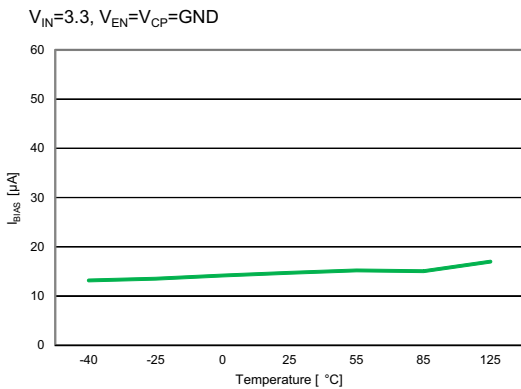
AM13862V1

**Figure 12. Bias current vs temperature (5 V)**



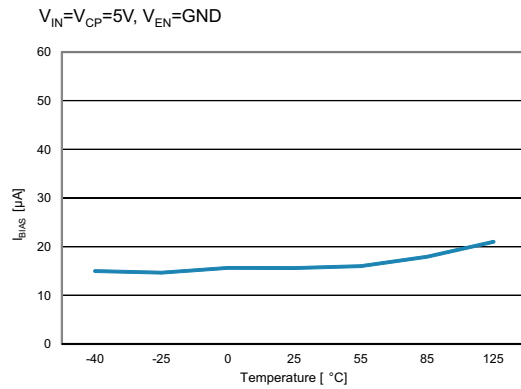
AM13863V1

**Figure 13. Shutdown current vs temperature (3.3 V)**



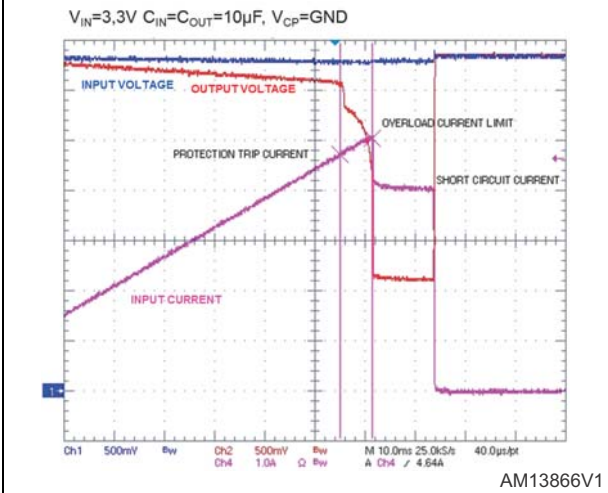
AM13864V1

**Figure 14. Shutdown current vs temperature (5 V)**

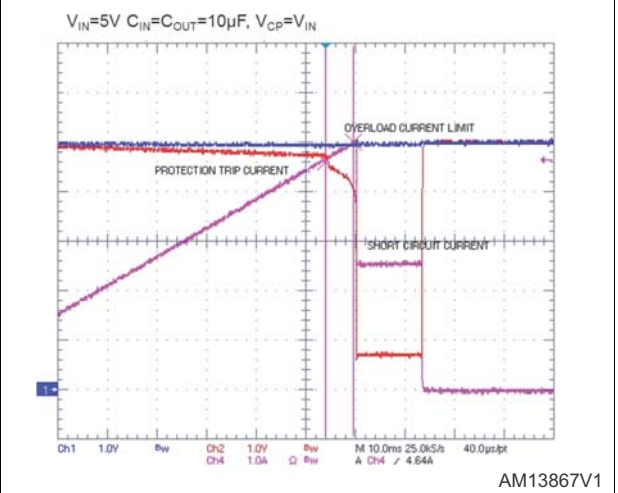


AM13865V1

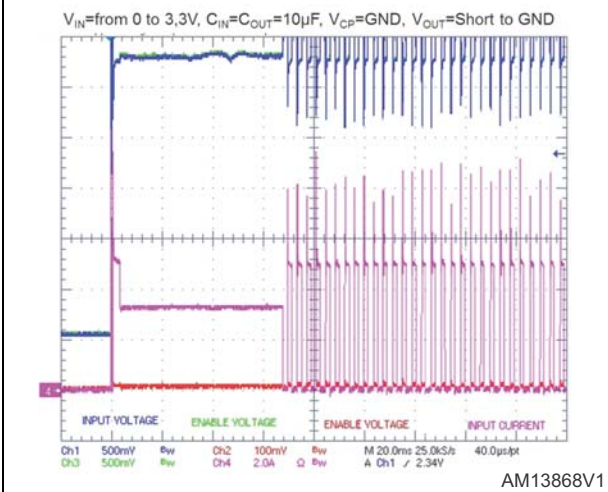
**Figure 15. Trip point, overload and short-circuit current (3.3 V)**



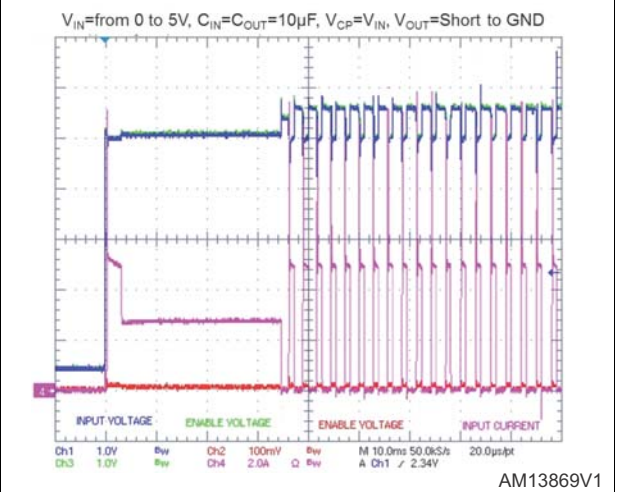
**Figure 16. Trip point, overload and short-circuit current (5 V)**



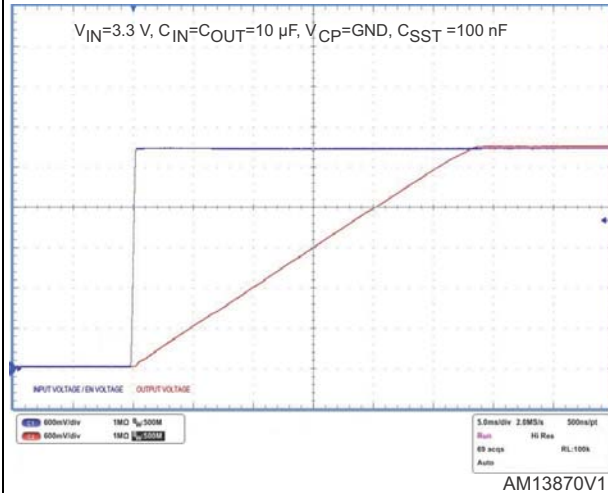
**Figure 17. Startup into short-circuit (3.3 V)**



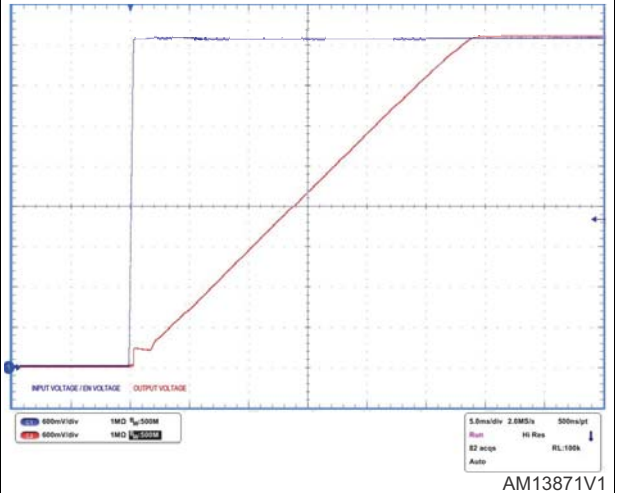
**Figure 18. Startup into short-circuit (5 V)**



**Figure 19. Soft-start behavior (3.3 V)**



**Figure 20. Soft-start behavior (5 V)**



## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 7.1 DFN6 3x3 - 10L package information

Figure 21. DFN6 3x3 - 10L package outline

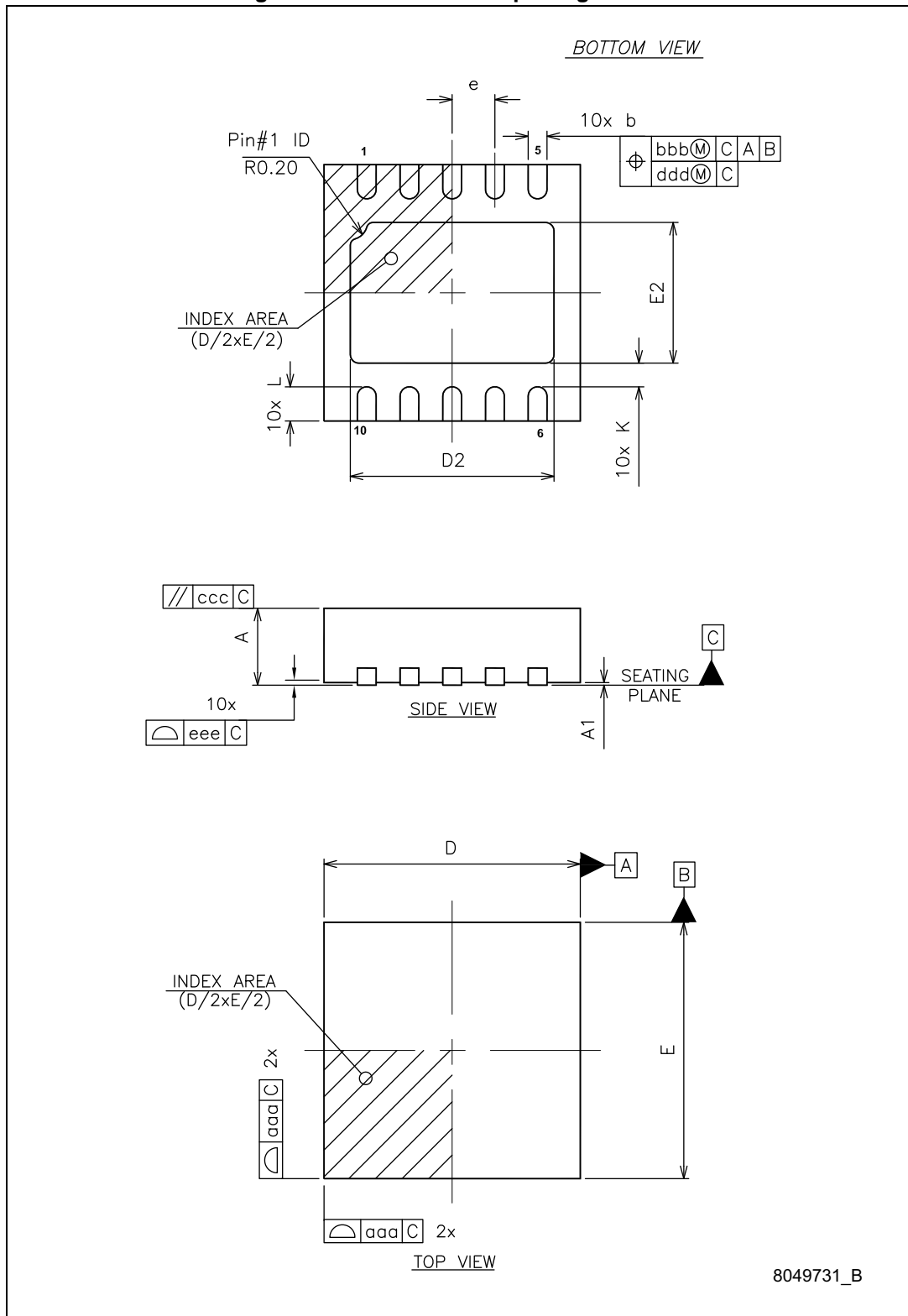
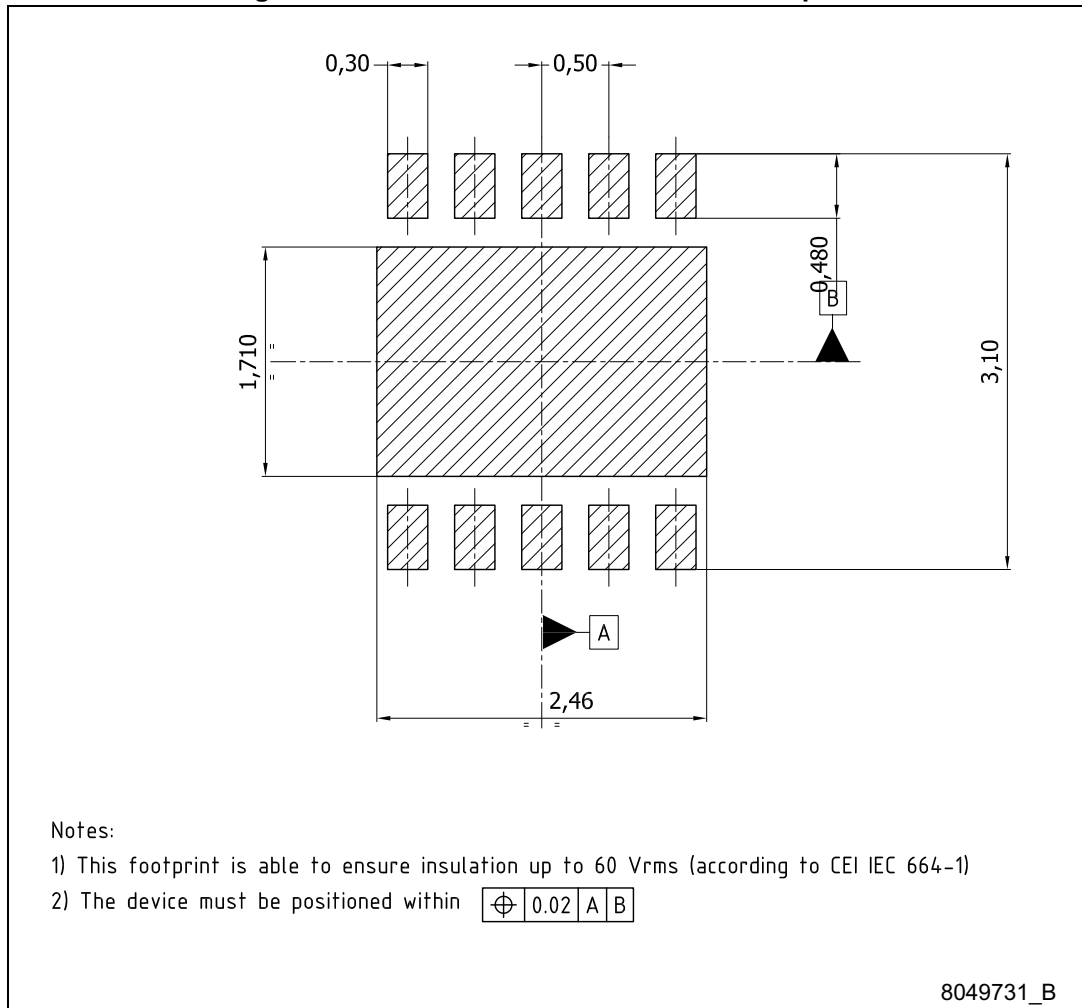


Table 7. DFN6 3x3 - 10L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		3.00	
E		3.00	
e		0.5	
D2	2.234	2.384	2.484
E2	1.496	1.646	1.746
K	0.20		
L	0.30	0.40	0.50
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	



Figure 22. DFN6 3x3 - 10L recommended footprint



## 7.2 DFN6 3x3 - 10L packing information

Figure 23. Tape for DFN6 3x3 - 10L

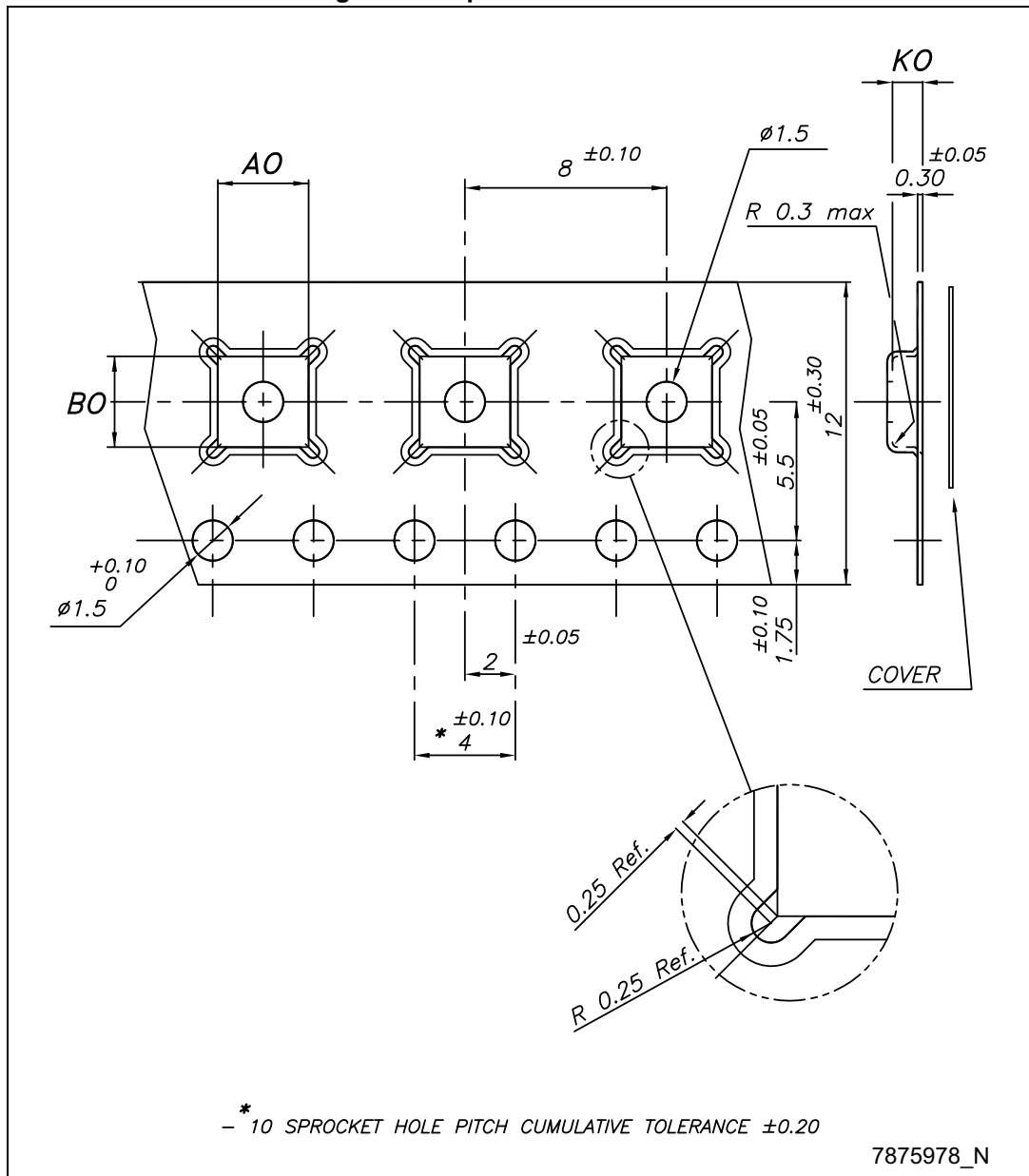


Figure 24. Reel for DFN6 3x3 - 10L

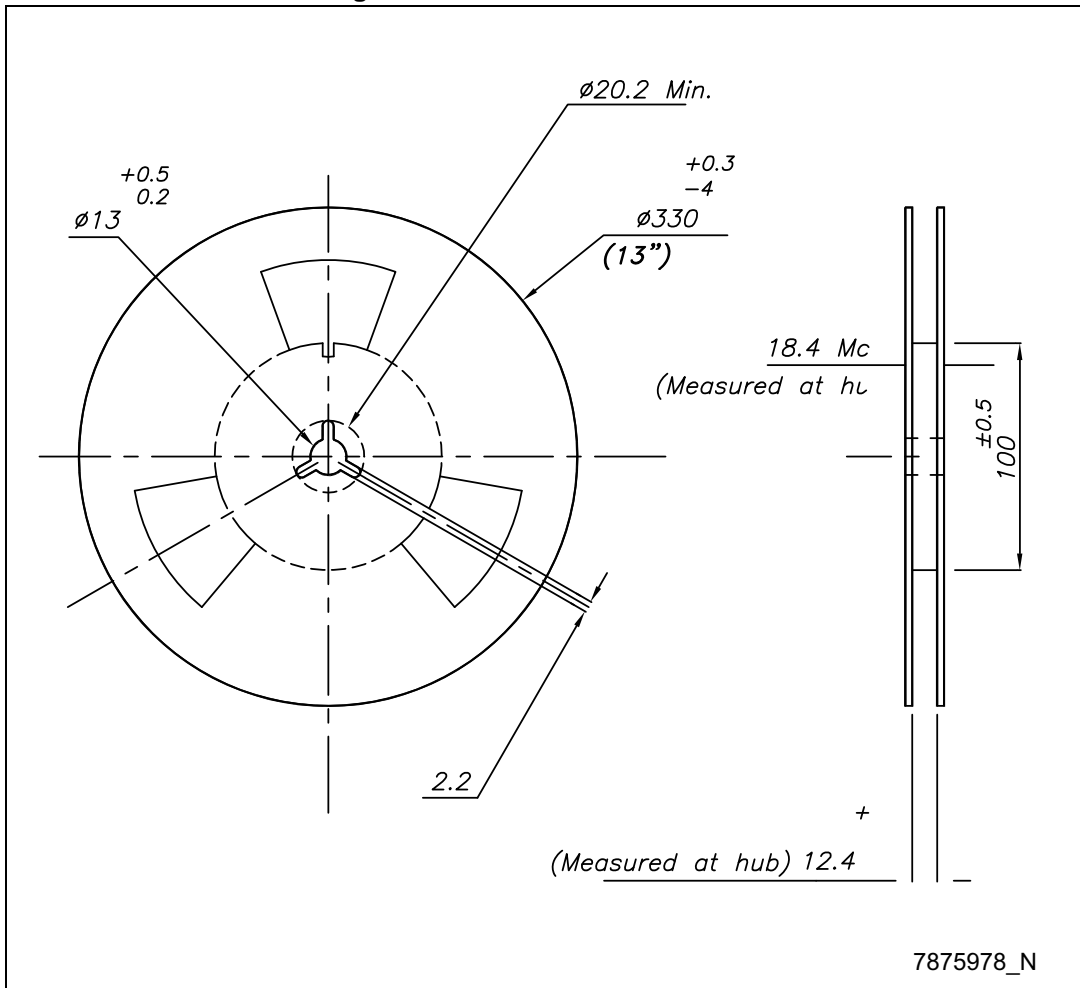


Figure 25. Schematic drawing orientation

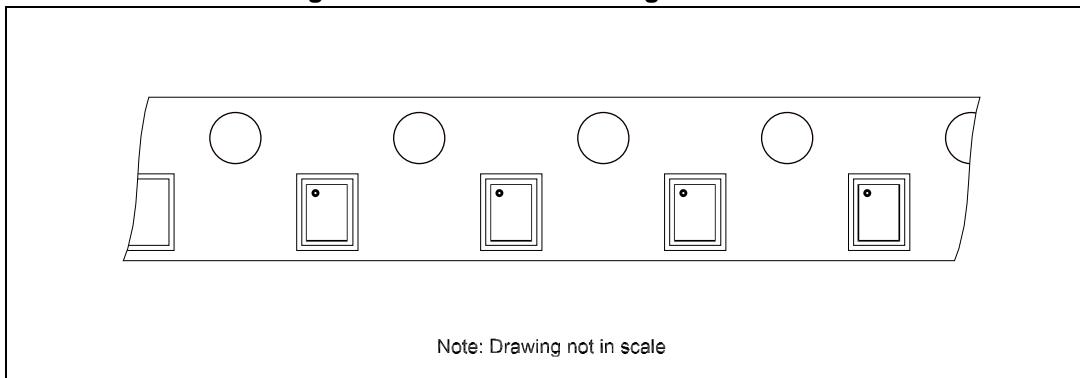


Table 8. DFN6 3x3 10L tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

## 8 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
23-Oct-2013	1	Initial release.
02-Dec-2014	2	Updated <i>Section 4: Electrical characteristics</i> , <i>Section 7: Package information</i> and <i>Figure 3: Application circuit</i> . Minor text changes.

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