SGM41528

I²C Controlled 2A, 2-Cell Battery Charger with Boost Mode for USB Input

FEATURES

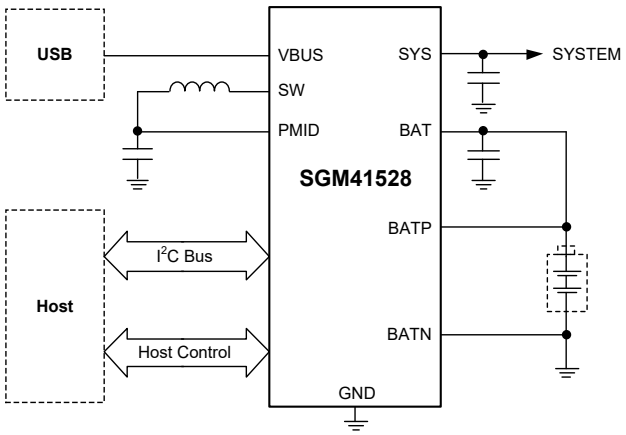
- 3.9V to 6.2V Operating Input Voltage Range
- Up to 20V Sustainable Voltage
- Fully Integrated All MOSFETs, Current Sense and Compensation
- High Efficiency, 2A, 1.5MHz Boost Charger:
  Up to 92.5% Charge Efficiency with 1A Charge Current for 7.6V Battery Voltage
- USB OTG with 4.5V to 5.5V Adjustable Output:
  Up to 2A Output, up to 94.5% Efficiency at 5.1V/1A Output
- Selectable PFM Mode and Out-of-Auto (OOA) Mode at Light Load Operations
- Narrow Voltage DC (NVDC) Power Path Management
- I²C Port for Flexible System Parameter Setting and Status Reporting
- Integrated ADC for Monitoring Input Voltage, Input Current, Battery Voltage, Charge Current, System Voltage, Battery Temperature and Die Temperature
- High Battery Discharge Efficiency with 13mΩ Switch
- USB BC1.2 and Non-Standard Input Source Adapters Auto Detection
- Input Current Optimizer (ICO) to Maximize Adapter Output Current without Overloading
- Programmable Input Current Limit (IINDPM) and Dynamic Power Management to Support USB Standard Adapters
- Maximum Power Tracking by Programmable Input Voltage Limit (VINDPM)
- Safety Features including Configurable JEITA for Battery Temperature Protection
- Battery Charging Safety Timer
- Thermal Regulation and Thermal Shutdown
- Watchdog Monitoring I²C Operation
- VBUS/System/Battery Over-Voltage Protection
- Output Over-Current Protection for Both Boost and OTG Buck Mode

APPLICATIONS

Smart Phones, EPOS

Portable Internet Devices and Accessory

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION

The SGM41528 is a battery charger and system power path management device for 2-cell Li-Ion or Li-polymer batteries. Its low-impedance power path optimizes efficiency, reduces battery charging time, and extends battery life. I²C programming makes it a flexible powering and charger design solution.

The SGM41528 can detect the input source types which include SDP/CDP/DCP and non-standard adapter through the D+/D- pins following USB BC1.2 Specification.

The SGM41528 features a dynamic power management (DPM) to avoid input adapter overloading or to meet the maximum current limit. It keeps the system voltage regulated to its minimum setting in DPM mode by reducing the charge current. The SGM41528 also provides supplement mode to further support system output in case that the charge current decreased to zero and input is still overload. The SGM41528 can provide the maximum power point with an algorithm called input current optimizer to avoid the input source from overloading.

The SGM41528 supports the default mode (standalone) without host control. It automatically detects the battery voltage and starts the charge. A charge cycle automatically terminates when a full charge is detected if the device is not in thermal regulation or DPM mode. The charger automatically initiates a new charging cycle if the battery voltage falls below the recharge threshold.

The SGM41528 supports USB On-The-Go (OTG) operation by supplying default 5.1V on the VBUS with an output current limit up to 2A.

The SGM41528 provides full protections for safety of battery charging and system operation, including battery temperature monitoring, charging safety timer, over-current and over-voltage protections. When any fault occurs, the SGM41528 asserts a nINT pulse to notify the host.

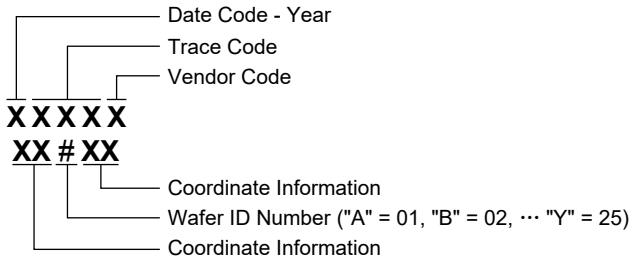
The SGM41528 is available in a Green WLCSP-2.1×2.1-25B package.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41528	WLCSP-2.1×2.1-25B	-40℃ to +85℃	SGM41528YG/TR	41528 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- VBUS (Converter Not Switching) ..... -0.3V to 20V
- PMID (Converter Not Switching) ..... -0.3V to 8.5V
- BAT, SYS (Converter Not Switching) ..... -0.3V to 12V
- SW ..... -0.6V (1) to 13V
- BTST ..... -0.3V to 19V
- BATP ..... -0.3V to 12V
- BATN, REGN, D+, D-, SDA, SCL, nINT, nCE, TS, nPG ..... -0.3V to 6V
- ILIM ..... -0.3V to 5V
- SYS to BAT ..... -0.3V to 8.5V
- BTST to SW ..... -0.3V to 6V

Output Sink Current, nINT, nPG 6mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{VBUS} ..... 3.9V to 6.2V
Average Input Current (VBUS), I_{VBUS} ..... 3.3A (MAX)
Average Charge Current (BAT), I_{BAT} ..... 2.2A (MAX)
Battery Voltage (BATP - BATN), V_{BAT} ..... 9.2V (2) (MAX)
RMS Discharging Current with Internal MOSFET, I_{BAT_RMS} ..... 4A (MAX)
Peak Discharging Current with Internal MOSFET, I_{BAT_PK} ..... 8A (MAX)
Operating Ambient Temperature Range ..... -40℃ to +85℃

NOTES:
1. -2V for 50ns.
2. The voltage spikes on SW pins should be less than the absolute maximum rating. Following the layout guidelines is helpful to minimize the switching noise.

OVERSTRESS CAUTION

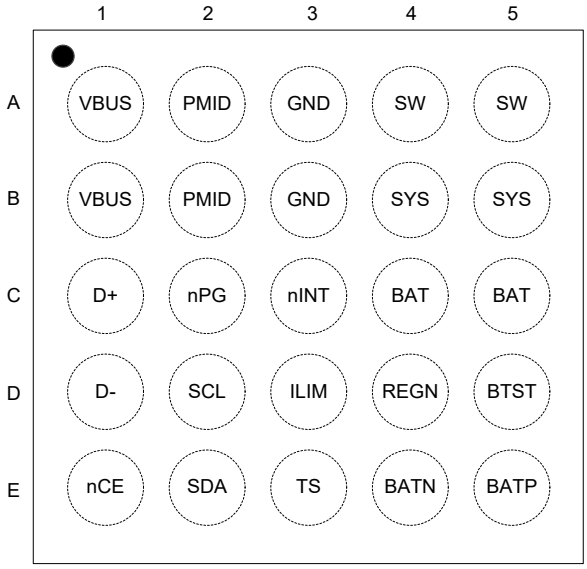
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.1×2.1-25B

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
A1, B1	VBUS	P	Charger Input (V_{IN}). Connect VBUS to the external DC power supply. Place a 1μF ceramic capacitor from VBUS pin to GND close to the device.
A2, B2	PMID	P	PMID Pin. Connect to the source of blocking MOSFET (QBLK). Given the total IC internal input supply. Connect a 10μF ceramic capacitor from PMID pin to GND.
A3, B3	GND	-	Ground Pin of the Device.
A4, A5	SW	P	Switching Node Output. Connect SW pin to the output inductor.
B4, B5	SYS	P	System Connection. The SYS pin is connected to BAT pin with an internal BATFET. It is recommended to connect more than 44μF ceramic capacitor between SYS and GND pins as close to the device as possible.
C1	D+	AIO	Positive Line of the USB Data Line Pair. D+/D- based USB device protocol detection.
C2	nPG	DO	Open-Drain Input Power Good Indicator Pin. Use a 10kΩ pull-up to the logic high rail. If the input voltage is below V_{VBUS_OV}, and passes the poor source detection, this pin outputs a low state to indicate a good input.
C3	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. The nINT pin sends out a negative 256μs pulse to the host when a fault occurs or a new charge status updates.
C4, C5	BAT	P	Battery Positive Terminal Pin. Use a 10μF capacitor between BAT and GND pins close to the device. SYS and BAT pins are internally connected by BATFET with current sensing capability.
D1	D-	AIO	Negative Line of the USB Data Line Pair. D+/D- based USB device protocol detection.
D2	SCL	DI	I²C Clock Signal. Use a 10kΩ pull-up to the logic high rail.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE (1)	FUNCTION
D3	ILIM	AI	Input Current Limit. A resistor between ILIM and GND pins can clamp the input current limit as I_{INMAX} = K_{ILIM}/R_{ILIM}. When EN_ILIM = 1, the lower limit between IINDPM[4:0] registers and ILIM pin resistor setting set the actual input current limit. The ILIM pin can supply higher than 500mA current limit only. If the current limit is not triggered, the ILIM pin voltage indicates the actual input current limit by I_{IN} = K_{ILIM} × $V_{ILIM}/(R_{ILIM}$ × 0.8V). Change EN_ILIM = 0 can disable both input current limit clamping and input current monitor function from ILIM pin.
D4	REGN	P	Gate Drive Power Supply. Power supply for internal MOSFET drivers and IC. Connect a 4.7μF ceramic capacitor from REGN pin to GND. It is recommended to place the capacitor close to REGN pin.
D5	BTST	P	PWM High-side Driver Supply. It is internally connected to the bootstrap diode cathode. A 47nF bootstrap capacitor between SW pin and BTST pin is recommended.
E1	nCE	DI	Charge Enable Input Pin (Active Low). When nCE pin is low and EN_CHG = 1, the charge is enabled. Do not leave nCE pin floating.
E2	SDA	DIO	I^2C Data Signal. Use a 10kΩ pull-up to the logic high rail.
E3	TS	AI	Temperature Sense Input Pin. Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor divider between REGN and GND. When TS pin voltage goes to hot or cold range, the charge suspends. It is recommended to use a 103AT-2 type thermistor.
E4	BATN	AI	Battery Sense Negative Terminal. Kelvin connects as close to the negative terminal of the battery as possible.
E5	BATP	AI	Battery Sense Positive Terminal. Kelvin connects as close to the positive terminal of the battery as possible.

NOTE:

1. AI = Analog Input, AO = Analog Output, AIO = Analog Input and Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input and Output, P = Power.

ELECTRICAL CHARACTERISTICS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Currents							
Battery Discharge Current (BATP, BAT, SYS)	I_{BAT}	V_{BAT} = 9V, no VBUS, SCL, SDA = 0V or 1.8V, ADC disabled	T_J = +25℃		14	22	μA
			T_J < +85℃		14	26	
Input Supply Current (VBUS) in HIZ	I_{VBUS_HIZ}	V_{VBUS} = 5V, HIZ mode, no battery, ADC disabled	T_J = +25℃		14.5	19	μA
			T_J < +85℃		14.5	23	
Input Supply Current (VBUS)	I_{VBUS}	V_{VBUS} = 5V, V_{BAT} = 7.6V, converter not switching			1.4	2	mA
		V_{VBUS} = 5V, V_{BAT} = 7.6V, I_{SYS} = 0A, converter switching, OOA disabled			5.6		
Battery Discharge Current in OTG Mode	I_{BAT_OTG}	V_{BAT} = 8.4V, OTG Buck mode, I_{VBUS} = 0A, converter switching, OOA disabled			3.5		mA
BAT Pin and VBUS Pin Power-Up							
VBUS Operating Range	V_{VBUS_OP}			3.9		6.2	V
VBUS UVLO to Have Active I²C (with No Battery)	V_{VBUS_UVLOZ}	V_{VBUS} rising			3.25	3.7	V
V_{VBUS} Minimum (as One of the Conditions) to Turn on REGN	$V_{VBUS\_PRESENT}$	V_{VBUS} rising			3.6	3.9	V
VBUS Over-Voltage Rising Threshold	V_{VBUS_OV}	V_{VBUS} rising		6.1		6.6	V
VBUS Over-Voltage Falling Threshold		V_{VBUS} falling		5.9		6.5	V
BAT Voltage to Have Active I²C (No Source on VBUS)	V_{BAT_UVLOZ}	V_{BAT} rising		3	3.55	4.1	V
Bad Adapter Detection Threshold	V_{BAD_SRC}				3.6		V
Bad Adapter Detection Current Source	I_{BAD_SRC}				7.6		mA
Power Path Management							
System Regulation Voltage	V_{SYS}	I_{SYS} = 0A, V_{BAT} = 8.8V, V_{BAT} > SYS_MIN[3:0], charge disabled (EN_CHG = 0), offset above V_{BAT}, PFM disabled			100		mV
		I_{SYS} = 0A, V_{BAT} < SYS_MIN[3:0], charge disabled (EN_CHG = 0), offset above V_{SYS_MIN}, PFM disabled			300		
Minimum DC System Voltage Output	V_{SYS_MIN}	V_{BAT} < SYS_MIN[3:0] = 1010, charge disabled (EN_CHG = 0)		7.2	7.3		V
Blocking MOSFET (Q1) On-Resistance between VBUS and PMID	R_{ON_QBLK}	T_J = +25℃			20	25	mΩ
		T_J = -40℃ to +85℃			20	31	
High-side Switching MOSFET (Q2) On-Resistance between SW and SYS	R_{ON_HSFET}	T_J = +25℃			27	33	mΩ
		T_J = -40℃ to +85℃			27	41	
Low-side Switching MOSFET (Q3) On-Resistance between SW and GND	R_{ON_LSFET}	T_J = +25℃			39	48	mΩ
		T_J = -40℃ to +85℃			39	58	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
Charge Voltage Program Range	$V_{BAT\_REG\_RANGE}$			6.8		9.2	V
Charge Voltage Step	$V_{BAT\_REG\_STEP}$				10		mV
Charge Voltage Setting Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 8.4V	T_J = +25℃	8.358	8.4	8.442	V
			T_J = -40℃ to +85℃	8.338	8.4	8.462	
		V_{BAT_REG} = 8.7V	T_J = +25℃	8.652	8.696	8.740	
			T_J = -40℃ to +85℃	8.633	8.696	8.760	
		V_{BAT_REG} = 8.8V	T_J = +25℃	8.754	8.798	8.842	
			T_J = -40℃ to +85℃	8.734	8.798	8.862	
Charge Current Regulation Range	$I_{CHG\_REG\_RANGE}$			0		2200	mA
Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$				50		mA
Fast Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$	V_{BAT} = 7.6V, T_J = +25℃	I_{CHG} = 250mA	210		290	mA
			I_{CHG} = 500mA	435		540	
			I_{CHG} = 1000mA	940		1060	
Pre-Charge Current Range	I_{PRECHG_RANGE}			50		800	mA
Typical Pre-Charge Current Step	I_{PRECHG_STEP}				50		mA
Pre-Charge Current Accuracy	I_{PRECHG_ACC}	V_{BAT} = 5V, I_{PRECHG} = 200mA, T_J = -20℃ to +85℃		145		270	mA
Termination Current Range	I_{TERM_RANGE}			50		800	mA
Typical Termination Current Step	I_{TERM_STEP}				50		mA
Termination Current Accuracy	I_{TERM_ACC}	I_{CHG} = 1.5A, T_J = -40℃ to +85℃	I_{TERM} = 50mA	30		70	mA
			I_{TERM} = 150mA	110		175	
Battery Short Voltage Rising Threshold to Start Pre-Charging	V_{BAT_SHORT}	V_{BAT} rising		4.2	4.4	4.6	V
Battery Short Voltage Falling Threshold to Stop Pre-Charging	$V_{BAT\_SHORT\_HYS}$	V_{BAT} falling		3.7	4	4.3	V
Battery Short Voltage Trickle Charging Current	I_{SHORT}	V_{BAT} < 4.4V			70		mA
Battery LOW Rising Threshold to Start Fast-Charging	V_{BAT_LOW}	V_{BAT} rising, V_{BATLOW} = 6V		5.8	6	6.2	V
Battery LOW Falling Threshold to Stop Fast-Charging		V_{BAT} falling, V_{BATLOW} = 6V		5.3	5.6	5.9	V
Recharge Threshold below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling	VRECHG[1:0] = 01		230		mV
			VRECHG[1:0] = 10		330		
MOSFET (Q4) On-Resistance between SYS and BAT	R_{ON_BATFET}	T_J = +25℃			13	19	mΩ
		T_J = -40℃ to +85℃			13	24	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage and Current Regulation (DPM: Dynamic Power Management)						
Input Voltage Regulation Range	V_{INDPM_RANGE}		3.9		5.5	V
Input Voltage Regulation Step	V_{INDPM_STEP}			100		mV
Input Voltage Regulation Limit	V_{INDPM}	V_{INDPM} = 3.9V	3.738	3.9	4.053	V
		V_{INDPM} = 4.4V	4.237	4.4	4.547	
Input Current Regulation Range	I_{INDPM_RANGE}		500		3300	mA
Input Current Regulation Step	I_{INDPM_STEP}			100		mA
Input Current Regulation Limit	I_{INDPM_ACC}	I_{INDPM} = 500mA	380	460	540	mA
		I_{INDPM} = 900mA	770	835	900	
		I_{INDPM} = 2500mA	2220	2335	2455	
		I_{INDPM} = 3000mA	2650	2805	2965	
Charge Current Setting Ratio	K_{ILIM}	I_{INMAX} = K_{ILIM}/R_{ILIM}, input current regulation by ILIM pin = 1.5A	935	1035	1135	A × Ω
D+/D- Detection						
D+/D- Voltage Source (600mV)	$V_{D+D-\_600MVSRC}$		560	600	640	mV
D+ Current Source (10μA)	$I_{D+\_10UASRC}$		7	12.5	18	μA
D+/D- Current Sink (100μA)	$I_{D+D-\_100UASNK}$		76	125	172	μA
D+/D- Comparator Threshold for Secondary Detection	V_{D+D-_0P325}		315		375	mV
D+ Comparator Threshold for Data Contact Detection	V_{D+_0P8}				840	mV
D- Resistor to Ground (19kΩ)	R_{D-_19K}			19		kΩ
D+/D- Threshold for Non-Standard Adapter	V_{D+D-_1P2}		1.07		1.42	V
	V_{D+D-_2P0}		1.90		2.09	
	V_{D+D-_2P8}		2.62		2.86	
D+/D- Leakage Current	I_{D+D-_LKG}	HIZ mode	-1		1	μA
Battery Over-Voltage Protection						
Battery Over-Voltage Rising Threshold	V_{BAT_OVP}	V_{BAT} rising, as percentage of V_{BAT_REG}	102.9	104	105.1	%
Battery Over-Voltage Falling Threshold		V_{BAT} falling, as percentage of V_{BAT_REG}	100.7	101.8	102.9	%
Thermal Regulation and Thermal Shutdown						
Junction Temperature Regulation Threshold	$T_{JUNCTION\_REG}$	TREG[1:0] = 11 (120℃)		120		℃
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature increasing		150		℃
Thermal Shutdown Falling Temperature		Temperature decreasing		120		℃
JEITA Thermistor Comparator (Boost Mode)						
T1 (0℃) Threshold	V_{T1}	As percentage of V_{REGN}, charge suspended below T1	72.9	73.3	73.7	%
	V_{T1_HYS}	As percentage of V_{REGN}, charge resume to I_{CHG}/2 and V_{REG} above T1_HYS		1.3		%
T2 (10℃) Threshold	V_{T2}	As percentage of V_{REGN}, charge back to I_{CHG}/2 and V_{REG} below T2	68	68.35	68.7	%
	V_{T2_HYS}	As percentage of V_{REGN}, charge back to I_{CHG} and V_{REG} above T2_HYS		1.3		%
T3 (45℃) Threshold	V_{T3}	As percentage of V_{REGN}, charge back to I_{CHG} and 8.1V above T3	44.4	44.85	45.3	%
	V_{T3_HYS}	As percentage of V_{REGN}, charge back to I_{CHG} and V_{REG} below T3_HYS		1		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
T4 (60℃) Threshold	V_{T4}	As percentage of V_{REGN}, charge suspended above T4	34	34.45	34.9	%
	V_{T4_HYS}	As percentage of V_{REGN}, charge back to I_{CHG} and 8.1V below T4_HYS		1.15		%
Cold/Hot Thermistor Comparator (OTG Buck Mode)						
Cold Temperature Threshold 0 (TS Pin Voltage Rising Threshold)	V_{BCOLD0}	As percentage of V_{REGN}, BCOLD = 0 (approx. -10℃ w/103AT)	76.6	77	77.4	%
Cold Temperature Threshold 0 (TS Pin Voltage Falling Threshold)	V_{BCOLD0_HYS}	As percentage of V_{REGN}		1		%
Cold Temperature Threshold 1 (TS Pin Voltage Rising Threshold)	V_{BCOLD1}	As percentage of V_{REGN}, BCOLD = 1 (approx. -20℃ w/103AT)	79.6	80	80.4	%
Cold Temperature Threshold 1 (TS Pin Voltage Falling Threshold)	V_{BCOLD1_HYS}	As percentage of V_{REGN}		1		%
Hot Temperature Threshold 0 (TS Pin Voltage Falling Threshold)	V_{BHOT0}	As percentage of V_{REGN}, BHOT[1:0] = 01 (approx. 55℃ w/103AT)	37.3	37.8	38.3	%
Hot Temperature Threshold 0 (TS Pin Voltage Rising Threshold)	V_{BHOT0_HYS}	As percentage of V_{REGN}		3		%
Hot Temperature Threshold 1 (TS Pin Voltage Falling Threshold)	V_{BHOT1}	As percentage of V_{REGN}, BHOT[1:0] = 00 (approx. 60℃ w/103AT)	34	34.45	34.9	%
Hot Temperature Threshold 1 (TS Pin Voltage Rising Threshold)	V_{BHOT1_HYS}	As percentage of V_{REGN}		3		%
Hot Temperature Threshold 2 (TS Pin Voltage Falling Threshold)	V_{BHOT2}	As percentage of V_{REGN}, BHOT[1:0] = 10 (approx. 65℃ w/103AT)	30.9	31.35	31.8	%
Hot Temperature Threshold 2 (TS Pin Voltage Rising Threshold)	V_{BHOT1_HY2}	As percentage of V_{REGN}		3		%
PWM						
PWM Switching Frequency	f_{SW}	Oscillator frequency, Boost mode	1.35	1.5	1.65	MHz
OTG Buck Mode Operation						
Battery Voltage Exiting OTG Mode	V_{OTG_BAT}	V_{BAT} falling	5.88	6.02	6.17	V
Typical OTG Buck Mode Voltage Regulation Range	V_{OTG_RANGE}		4.5		5.5	V
Typical OTG Buck Mode Voltage Regulation Step	V_{OTG_STEP}			100		mV
OTG Buck Mode Voltage Regulation Accuracy	V_{OTG_ACC}	I_{VBUS} = 0A, OTG_VLIM[3:0] = 5V	4.89		5.17	V
Typical OTG Buck Mode Current Regulation Range	I_{OTG_RANGE}		0.5		2	A
Typical OTG Buck Mode Current Regulation Step	I_{OTG_STEP}			100		mA
OTG Buck Mode Current Regulation Accuracy	I_{OTG_ACC}	OTG_ILIM[3:0] = 1A, T_J = +25℃	-17	-5	8	%
OTG Buck Mode Over-Voltage Threshold	V_{OTG_OVP}		5.88	6.03		V
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 5V, I_{REGN} = 20mA	4.8	4.95		V
REGN LDO Current Limit	I_{REGN}	V_{VBUS} = 5V, V_{REGN} = 3.8V	23			mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog-to-Digital Converter (ADC) (1)						
Conversion Time, Each Measurement	t_{ADC_CONV}	ADC_SAMPLE[1:0] = 00		24		ms
		ADC_SAMPLE[1:0] = 01		12		
		ADC_SAMPLE[1:0] = 10		6		
		ADC_SAMPLE[1:0] = 11		3		
Effective Resolution	ADCRES	ADC_SAMPLE[1:0] = 00		15		bits
		ADC_SAMPLE[1:0] = 01		14		
		ADC_SAMPLE[1:0] = 10		13		
		ADC_SAMPLE[1:0] = 11		11		
ADC Measurement Ranges and LSB						
ADC BUS Current Range	$I_{BUS\_ADC\_RANGE}$		0		4	A
ADC BUS Current LSB	$I_{BUS\_ADC\_LSB}$			1		mA
ADC BAT Current Range	$I_{BAT\_ADC\_RANGE}$		0		4	A
ADC BAT Current LSB	$I_{BAT\_ADC\_LSB}$			1		mA
ADC BUS Voltage Range	$V_{BUS\_ADC\_RANGE}$		0		6.5	V
ADC BUS Voltage LSB	$V_{BUS\_ADC\_LSB}$			1		mV
ADC SYS Voltage Range	$V_{SYS\_ADC\_RANGE}$		0		10	V
ADC SYS Voltage LSB	$V_{SYS\_ADC\_LSB}$			1		mV
ADC BAT Voltage Range	$V_{BAT\_ADC\_RANGE}$		0		10	V
ADC BAT Voltage LSB	$V_{BAT\_ADC\_LSB}$			1		mV
ADC TS Voltage Range	$V_{TS\_ADC\_RANGE}$		10		90	%
ADC TS Voltage LSB	$V_{TS\_ADC\_LSB}$			0.098		%
ADC Die Temperature Range	$V_{TDIE\_ADC\_RANGE}$		0		128	℃
ADC Die Temperature LSB	$V_{TDIE\_ADC\_LSB}$			0.5		℃
I²C Interface Characteristics (SCL, SDA)						
Input High Threshold (SDA and SCL)	V_{IH}	Pull up rail 1.8V	1.3			V
Input Low Threshold	V_{IL}	Pull up rail 1.8V			0.4	V
Output Low Threshold	V_{OL}	Sink current = 5mA			0.4	V
High-Level Leakage Current	I_{BIAS}	Pull up rail 1.8V			1	μA
Logic I/O Pin Characteristics (nCE)						
Input High Threshold	V_{IH}		1.3			V
Input Low Threshold	V_{IL}				0.4	V
High-Level Leakage Current	I_{IN_BIAS}	Pull up rail 1.8V			1	μA
Logic Output Pin Characteristics (nINT, nPG)						
Output Low Threshold	V_{OL}	Sink current = 5mA			0.4	V
High-Level Leakage Current	I_{OUT_BIAS}	Pull up rail 1.8V			1	μA

NOTE:
1. Guaranteed by design.

TIMING REQUIREMENTS

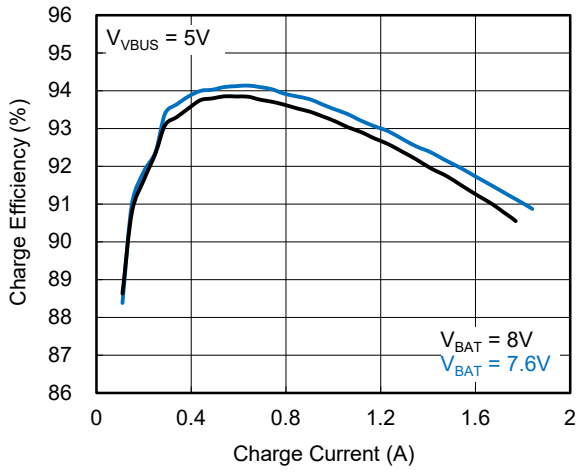
(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{VBUS}/V_{BAT} Power-Up							
VBUS OVP Reaction Time	t_{VBUS_OV}	V_{VBUS} rising above V_{VBUS_OV} threshold to turn off the converter			200		ns
Wait Window for Bad Adapter Detection	t_{BAD_SRC}				30		ms
Battery Charger							
Deglitch Time for Charge Termination	t_{TERM_DGL}	Charge current falling below I_{TERM}			250		ms
Deglitch Time for Recharge Threshold	t_{RECGH_DGL}	BAT voltage falling below V_{RECHG} = 100mV			250		ms
Deglitch Time for Battery Over-Voltage to Disable Charge	$t_{BAT\_OVP\_DGL}$				1		μs
Typical Charge Safety Timer Range	t_{SAFETY}	CHG_TIMER[1:0] = 10 (16.5h)		12.9	16.5	20.2	h
Typical Top-Off Timer Range	t_{TOP_OFF}	TOPOFF_TIMER[1:0] = 10 (30min)		27	34	44	min
Digital Clock and Watchdog Timer							
Watchdog Reset Time	t_{WDT}	WATCHDOG[1:0] = 11 (160s)	REGN LDO disabled		164		s
			REGN LDO enabled	132	164	202	
Digital Clock Frequency in Low Power	f_{LPDIG}	REGN LDO disabled			30		kHz
Digital Clock Frequency	f_{DIG}	REGN LDO enabled			1.5		MHz
I²C Interface							
SCL Clock Frequency	f_{SCL}					1	MHz

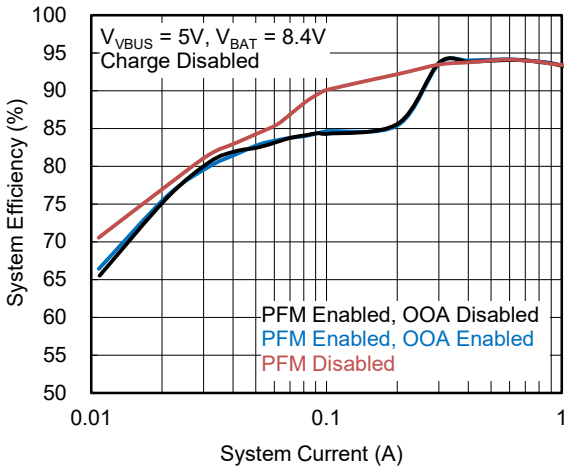
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, C_{VBUS} = 1μF, C_{PMID} = 10μF, C_{BAT} = 10μF, C_{SYS} = 2 × 22μF, L = 1μH, unless otherwise noted.

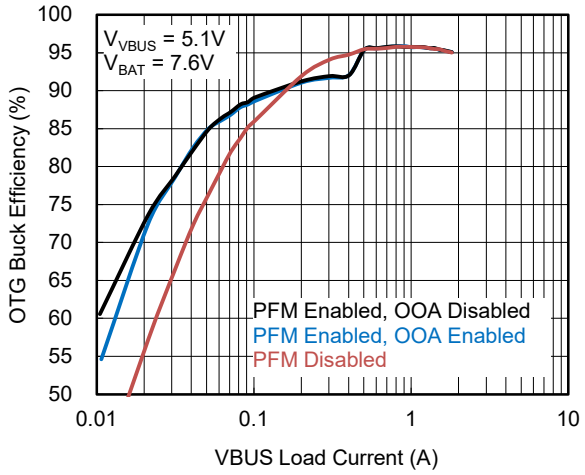
Charge Efficiency vs. Charge Current



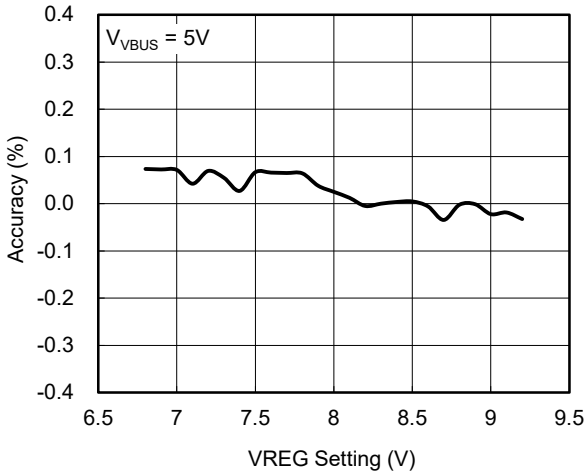
System Efficiency vs. System Current



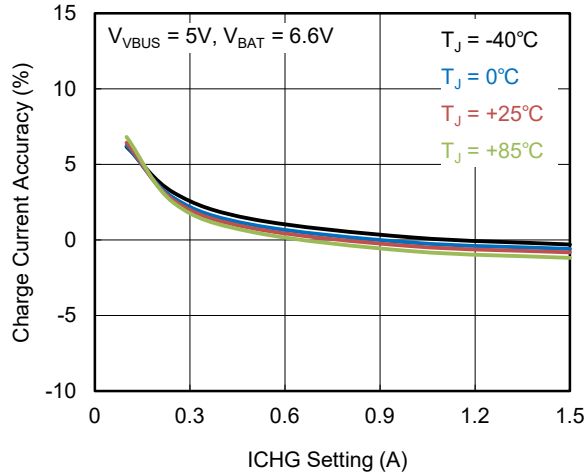
OTG Buck Efficiency vs. VBUS Load Current



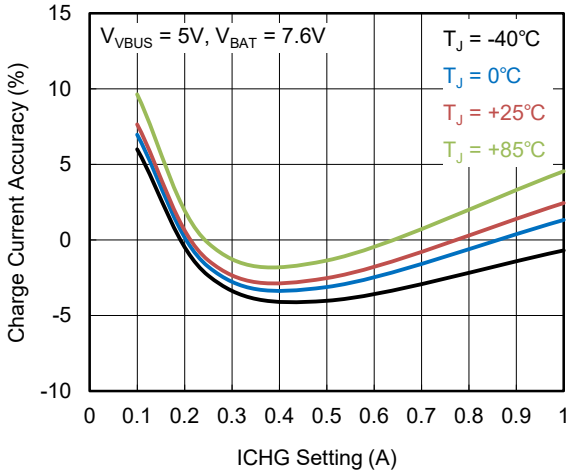
Battery Voltage Accuracy vs. VREG Setting



Charge Current Accuracy vs. ICHG Setting



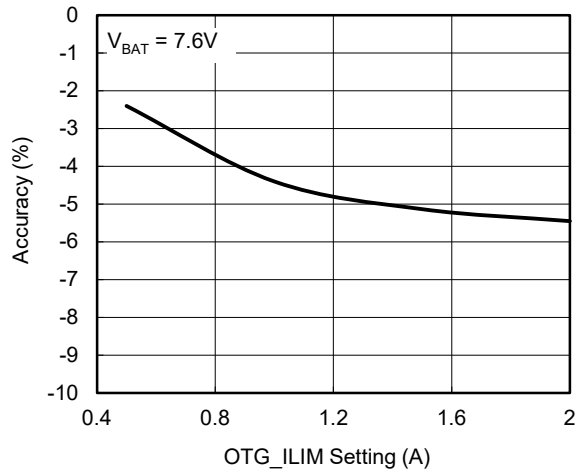
Charge Current Accuracy vs. ICHG Setting



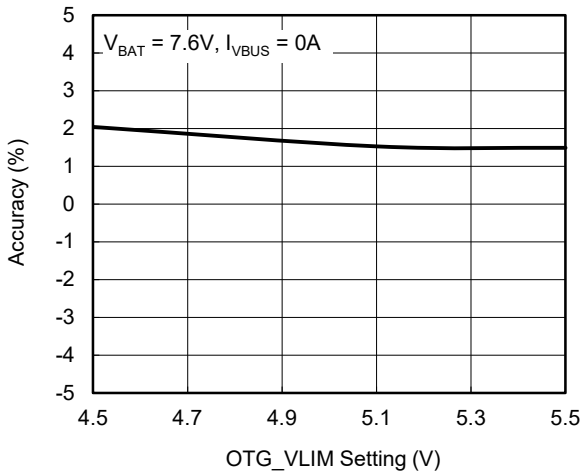
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, C_{VBUS} = 1μF, C_{PMID} = 10μF, C_{BAT} = 10μF, C_{SYS} = 2 × 22μF, L = 1μH, unless otherwise noted.

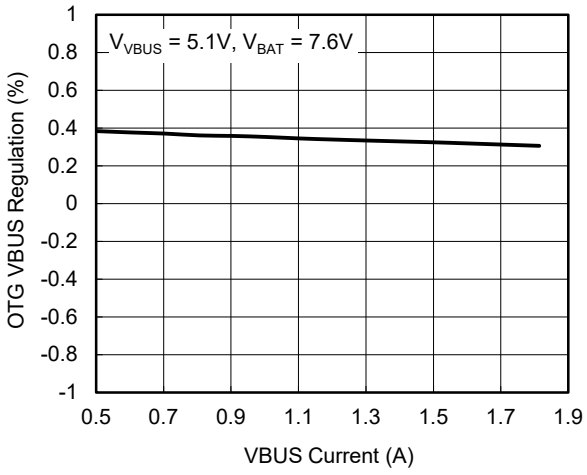
OTG_ILIM Accuracy



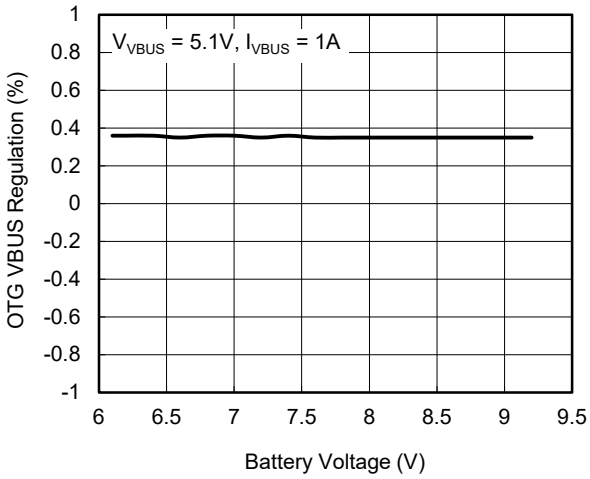
OTG_VLIM Accuracy



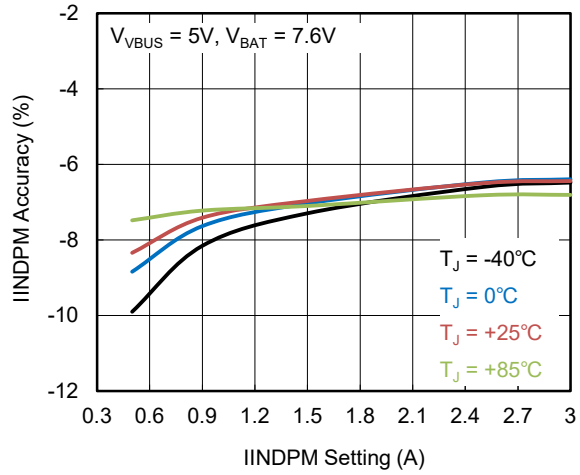
OTG VBUS Regulation vs. VBUS Current



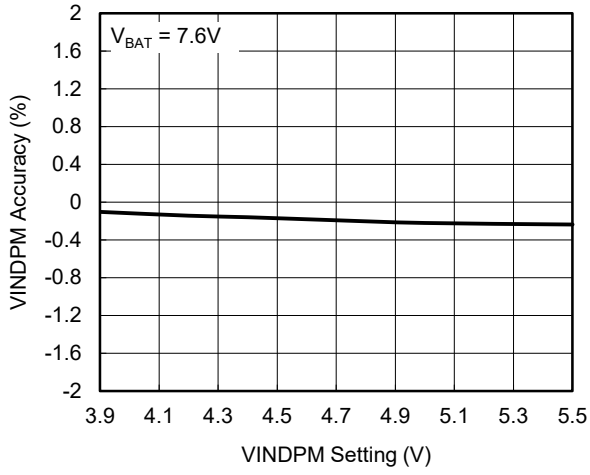
OTG VBUS Regulation vs. Battery Voltage



IINDPM Accuracy



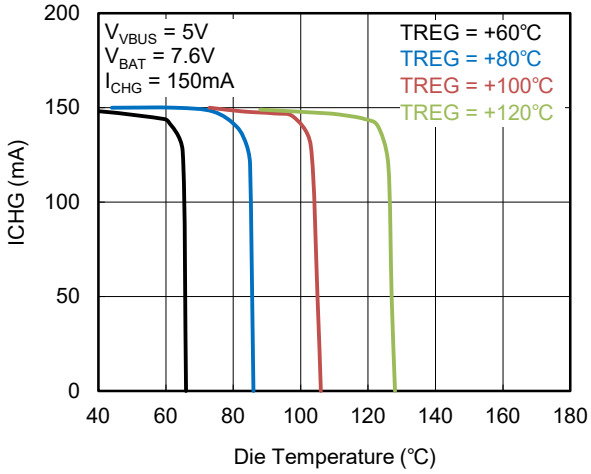
VINDPM Accuracy



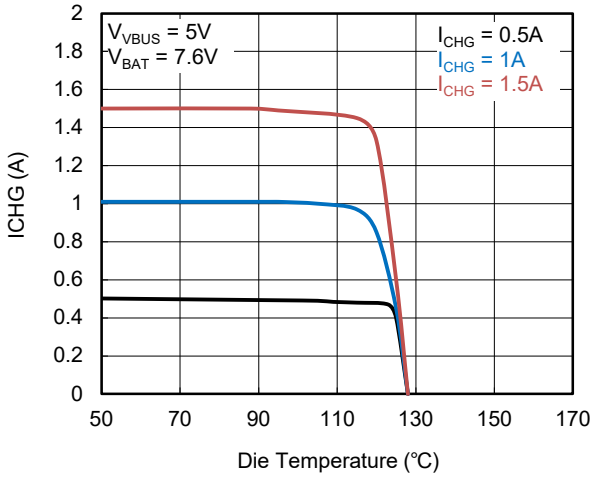
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, C_{VBUS} = 1μF, C_{PMID} = 10μF, C_{BAT} = 10μF, C_{SYS} = 2 × 22μF, L = 1μH, unless otherwise noted.

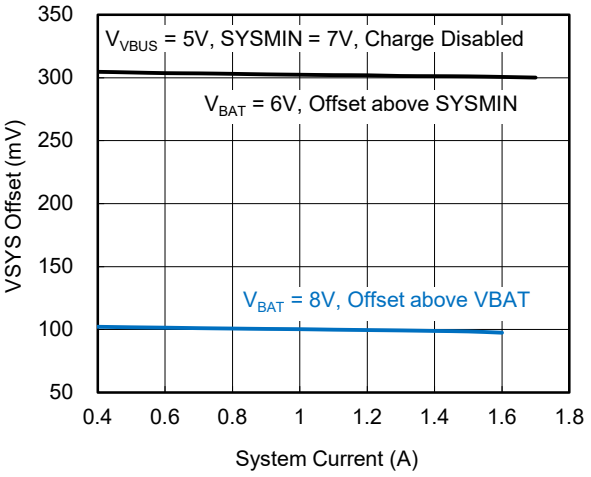
TREG Profiles



ICHG vs. Die Temperature



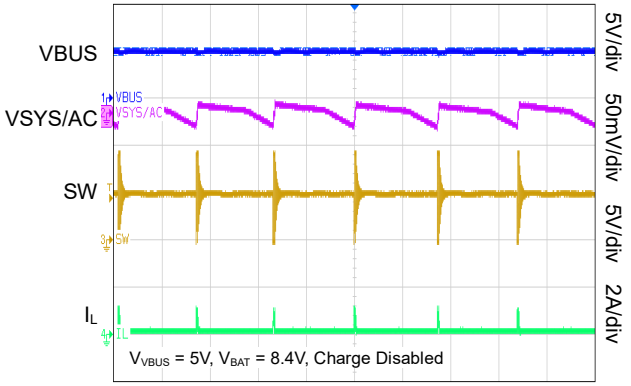
System Load Regulation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

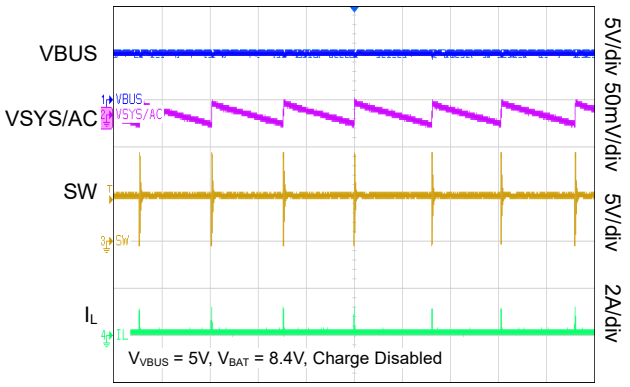
T_J = +25℃, C_{VBUS} = 1μF, C_{PMID} = 10μF, C_{BAT} = 10μF, C_{SYS} = 2 × 22μF, L = 1μH, unless otherwise noted.

Boost Mode PFM Switching, OOA Enabled



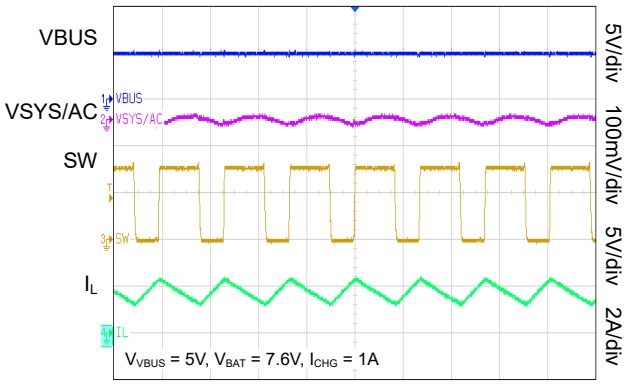
Time (20μs/div)

Boost Mode PFM Switching, OOA Disabled



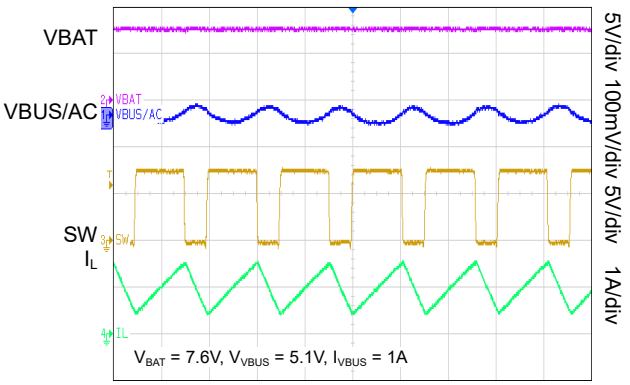
Time (50μs/div)

Boost Mode CCM Switching



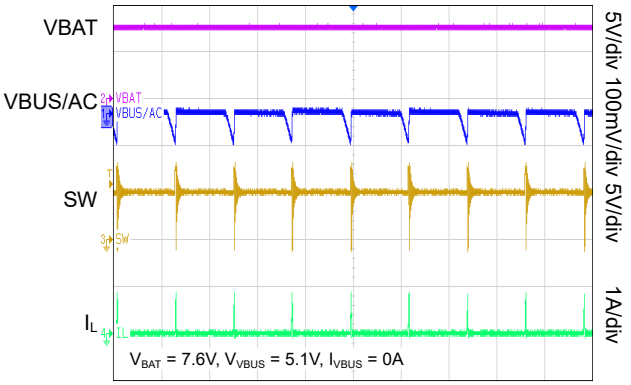
Time (500ns/div)

OTG Buck Mode CCM Switching



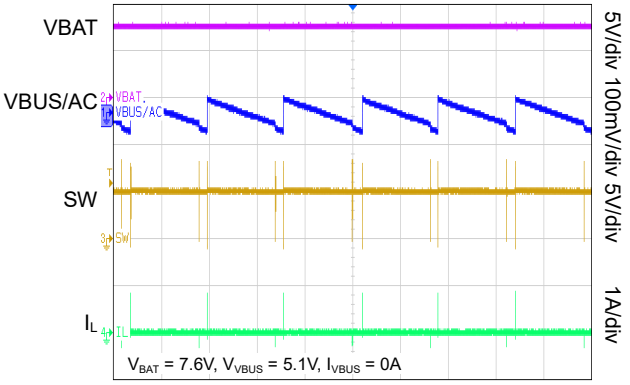
Time (500ns/div)

OTG Buck Mode PFM Switching, OOA Enabled



Time (20μs/div)

OTG Buck Mode PFM Switching, OOA Disabled

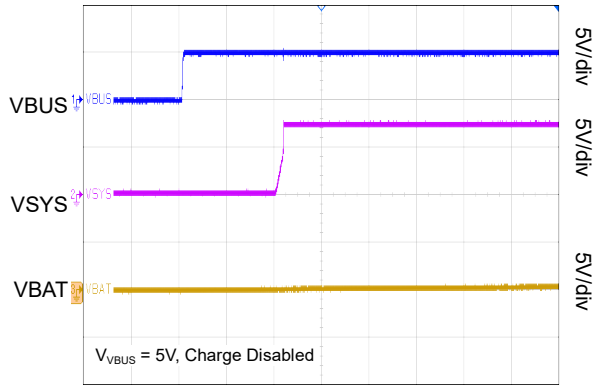


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

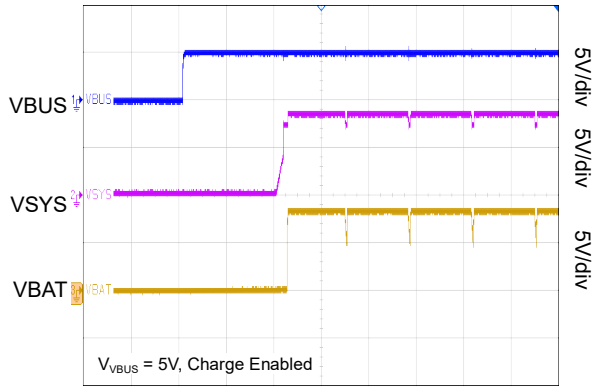
T_J = +25℃, C_{VBUS} = 1μF, C_{PMID} = 10μF, C_{BAT} = 10μF, C_{SYS} = 2 × 22μF, L = 1μH, unless otherwise noted.

Adapter Plug-In with No Battery



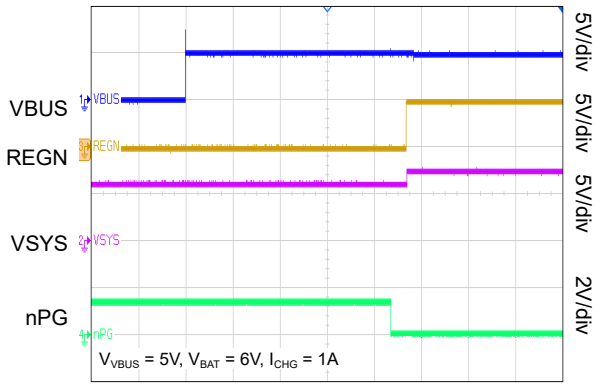
Time (200ms/div)

Adapter Plug-In with No Battery



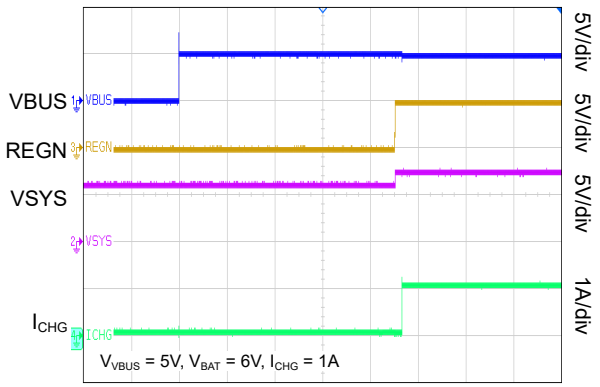
Time (200ms/div)

Adapter Plug-In with Charge Enabled



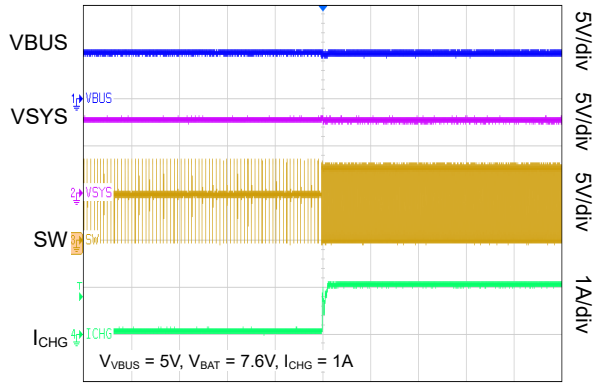
Time (100ms/div)

Adapter Plug-In with Charge Enabled



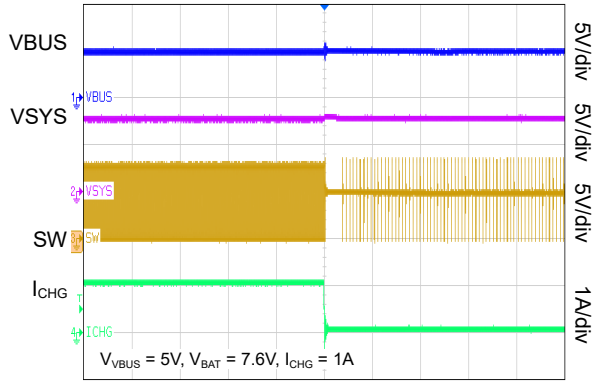
Time (100ms/div)

Charge Enabled



Time (500μs/div)

Charge Disabled

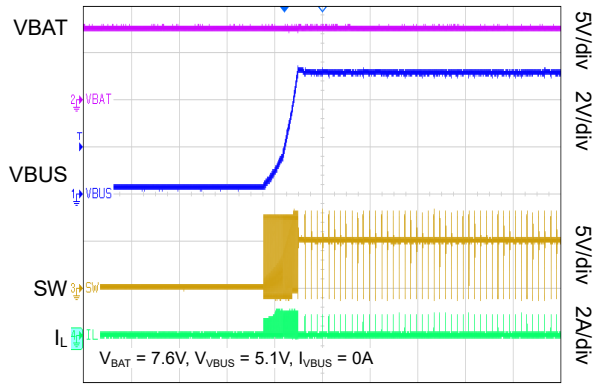


Time (500μs/div)

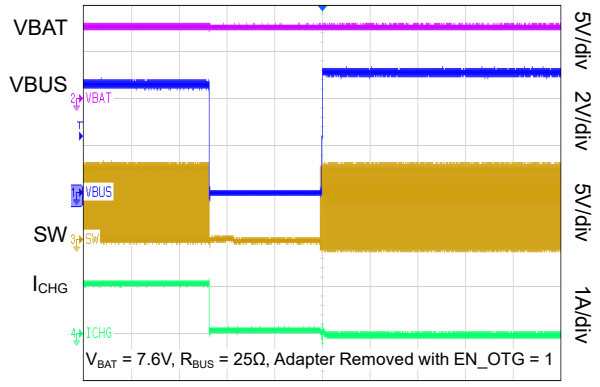
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, C_{VBUS} = 1μF, C_{PMID} = 10μF, C_{BAT} = 10μF, C_{SYS} = 2 × 22μF, L = 1μH, unless otherwise noted.

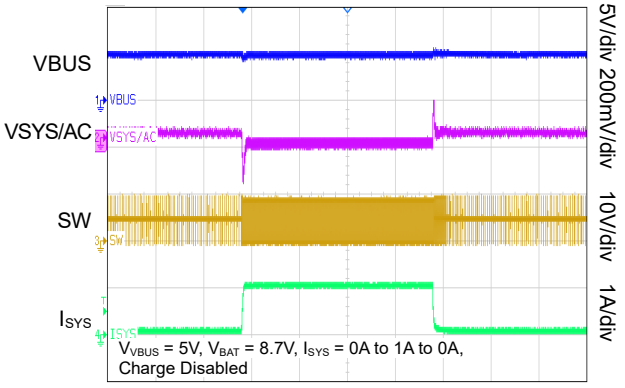
OTG Buck Mode Startup



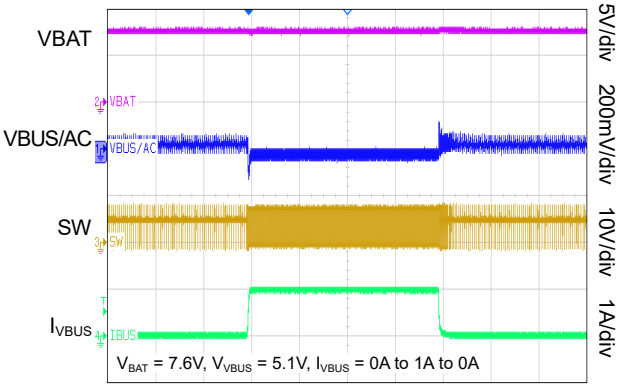
OTG Buck Mode Startup after Adapter Removal



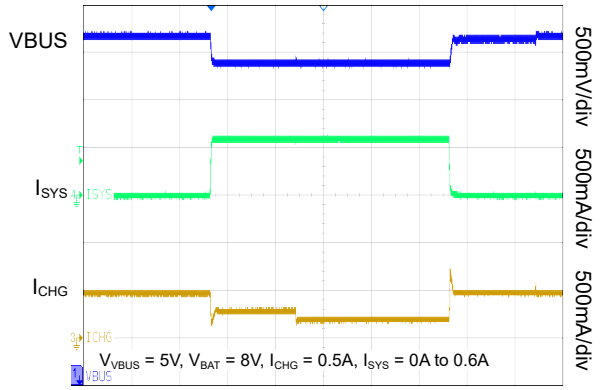
System Load Transient Response



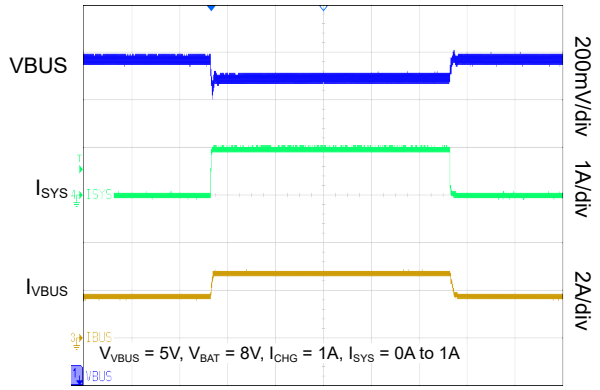
OTG Buck Mode Load Transient Response



VINDPM Transient Response



IINDPM Transient Response



TYPICAL APPLICATION CIRCUIT

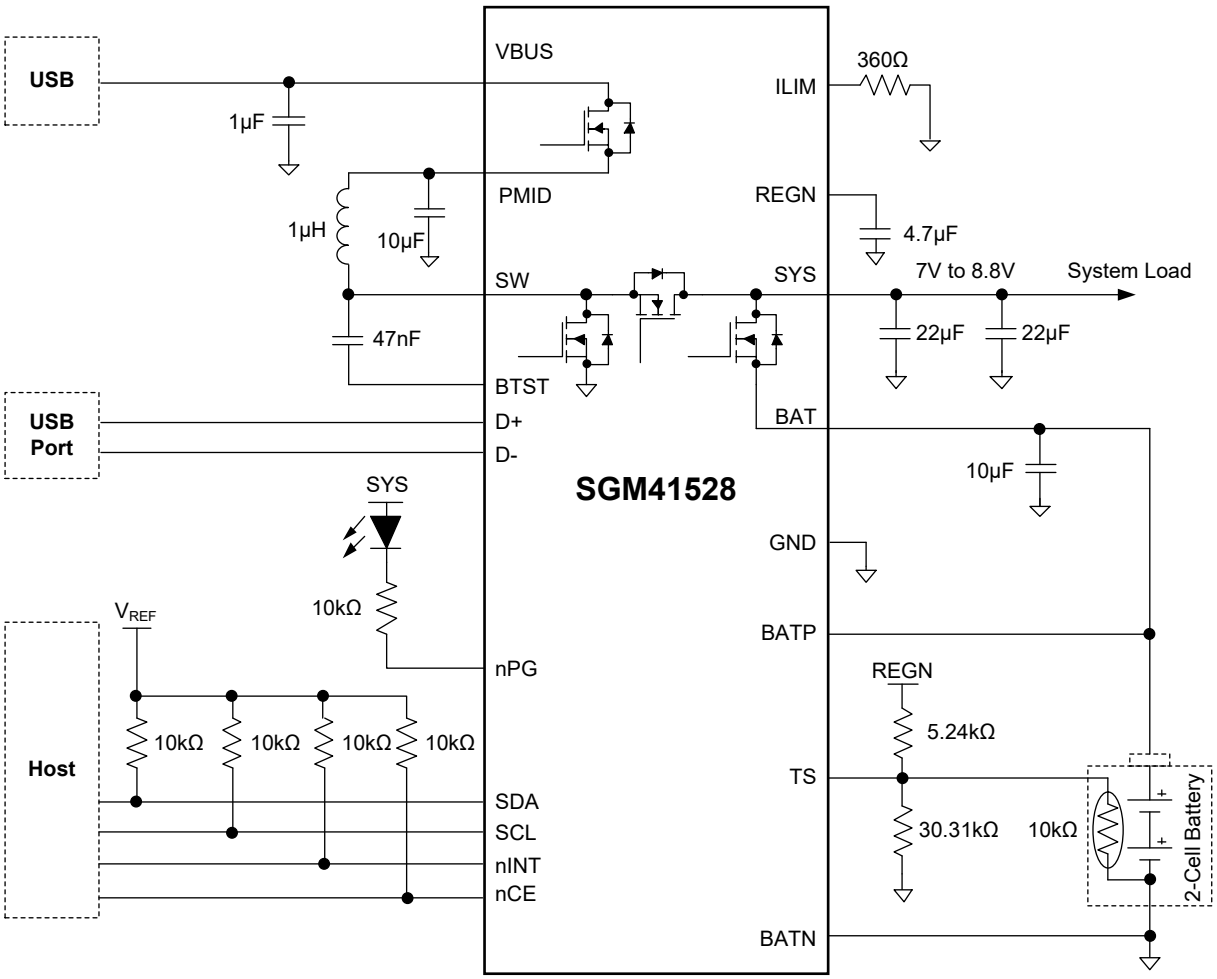


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

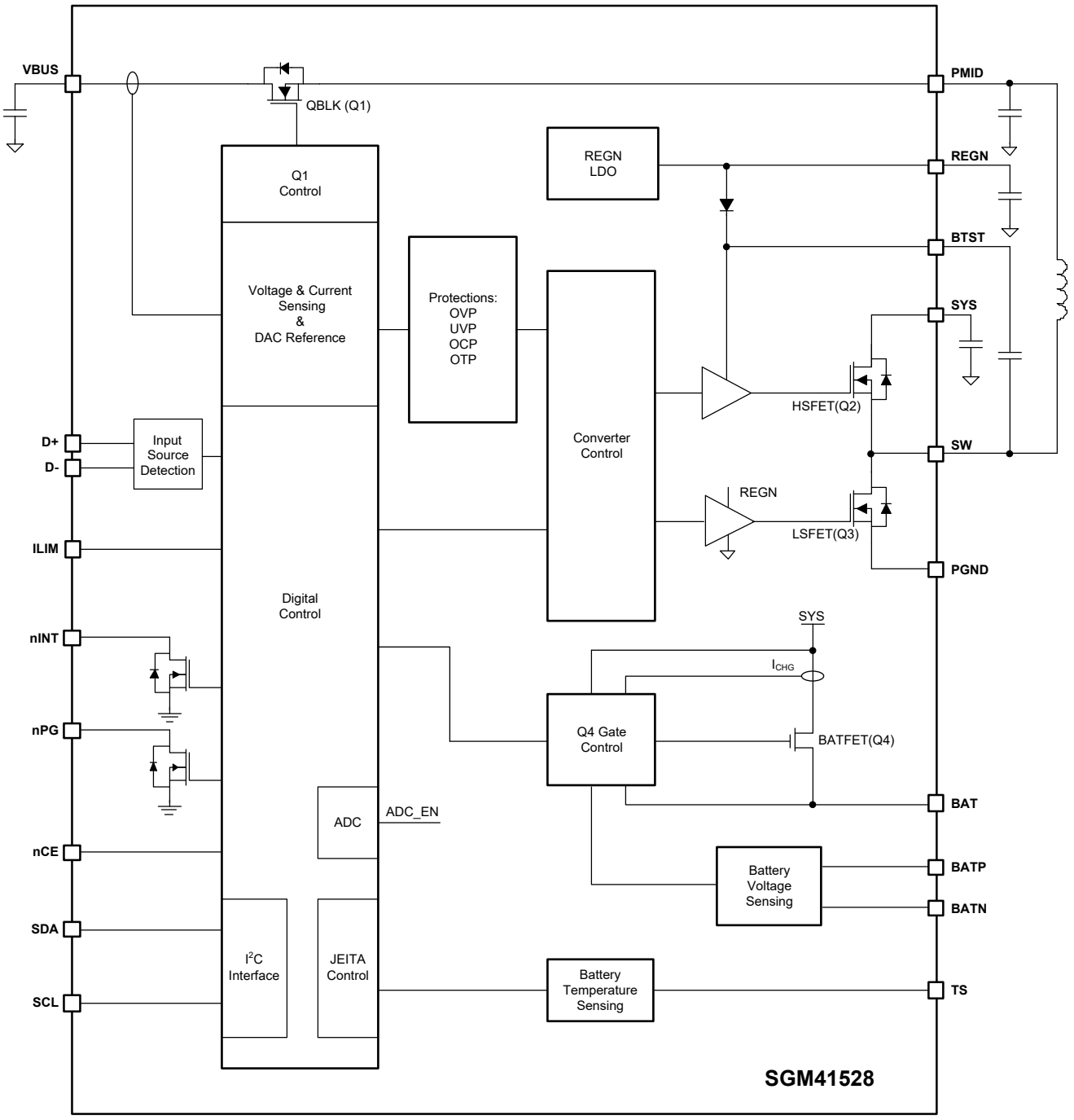


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM41528 is a battery charger and system power path management device with integrated Boost converter and power switches for use with 2-cell Li-Ion or Li-polymer batteries. The device includes four main power switches: input blocking MOSFET (Q1, QBLK), high-side switching MOSFET (Q2, HSFET), low-side switching MOSFET (Q3, LSFET), and battery MOSFET (Q4, BATFET).

Power-On Reset (POR)

The internal circuit of the device is powered from the greater voltage between V_{VBUS} and V_{BAT}. When the voltage of the selected source goes above its UVLO level (V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > V_{BAT_UVLOZ}), a POR happens and activates the BATFET driver. Upon activation, the I^2C interface will also be ready for communication, and all the registers reset to their default values.

Power-Up from Battery Only (No Input Source)

When there have no other input source but only the battery, that the voltage is higher than the UVLO threshold (V_{BAT_UVLOZ}), is presented, the BATFET turns on to connect the system to the battery. The quiescent current is minimum because the REGN LDO remains off. Conduction losses are also low due to small R_{DSON} of BATFET. Low losses help to extend the battery run time. The discharge current through BATFET is continuously monitored.

Power-Up Process from the Input Power Source

Upon connection of an input source (VBUS), the input source from VBUS pin is checked to turn on the internal REGN LDO regulator and the bias circuits (no matter whether the battery is present or not). Before the Boost converter starts, the device is detected and set the input current limit threshold. The sequences of actions when VBUS as input source is powered up are:

1. Poor power source detection (qualification).
2. Input power source type detection. (Based on D+/D- inputs. It is used to set the default input current limit (IINDPM[4:0]).)
3. REGN LDO power-up.
4. DC/DC converter power-up.

Details of the power-up steps are explained in the following sections.

Poor Power Source Detection (Qualification)

When valid VBUS is plugged in, the input power source (adapter or other source) is checked for its type and current capacity. To start the Boost converter, the input (VBUS) must meet the following conditions:

1. V_{VBUS} < V_{VBUS_OV}.
2. V_{VBUS} > V_{BAD_SRC} + $V_{BAD\_SRC\_HYS}$ (100mV TYP) during t_{BAD_SRC} test period (30ms TYP) in which the I_{BAD_SRC} (7.6mA TYP) current is pulled from VBUS.

Once the VBUS over-voltage protection is detected, the SGM41528 will automatically retry the detection when the over-voltage fault condition disappears. If above condition 2 is detected (bad source adapter), the SGM41528 retries the detection and enters HIZ mode (EN_HIZ bit is reset to 0) after 7 consecutive failures. In HIZ mode, the system is supplied by the battery only. Resume the converter operation requires re-plugging the adapter and/or toggling the EN_HIZ bit. When the adapter is plugged in, the EN_HIZ bit is automatically reset to 0.

Input Power Source Type Detection

The input power source detection will run through the D+/D- lines after the adapter passes the poor source qualification when the AUTO_INDET_EN bit is set to 1. The SGM41528 follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input adapter power source type via D+/D- lines. All the types of SDP/CDP/DCP and non-standard adapter can be automatically detected and indicated. When the input power source type detection is completed, the statuses of some related registers and pins are updated as detailed below:

1. Input current limit register (IINDPM[4:0]) is changed to set the right current limit.
2. Change the input voltage limit register (VINDPM[4:0]) to default setting if EN_VINDPM_RST = 1. Keep VINDPM[4:0] register value unchanged if EN_VINDPM_RST = 0.
3. Change the VBUS_STAT[2:0] bits according to the input source type detection result.
4. The PG_STAT bit is set to 1 and the nPG pin is pulled to logic low.
5. The nINT pin is pulsed to notify the host.

The input current or the input voltage is always limited by the IINDPM[4:0] or VINDPM[4:0] register and the limit can be updated by the host if needed. Regardless of the input current optimizer (ICO) setting, the charger input current is always limited by the lower value of the IINDPM[4:0] register or the current limit set by ILIM pin.

DETAILED DESCRIPTION (continued)

The input power source type detection is ignored if AUTO_INDET_EN = 0. In this case, the IINDPM[4:0] register remains unchanged and the VBUS_STAT[2:0] bits keep 000 (no input). If EN_VINDPM_RST bit is set to 0 by the host before the input power source type detection, the VINDPM[4:0] register remains unchanged.

Input Current Limit by D+/D- Detection

The input current limit of SGM41528 is determined and set by the integrated D+/D- based input power source detection. Four major steps are included in the D+/D- detection: VBUS detection, data contact detection (DCD, detect non-standard adapter), primary detection (detect SDP), and secondary detection (detect CDP and DCP). Please refer to Figure 3. Table 1 shows the non-standard adapter type detection.

After the input power source type detection is completed, the nINT pin sends out a low pulse to notify the host. In addition, the VBUS_STAT[2:0] bits and the IINDPM[4:0] register are updated as below, refer to Table 2.

Input Current Limit Force Detection

In host mode, the host can set FORCE_INDET = 1 to force the charger to run the input current limit detection. The FORCE_INDET bit automatically reset to 0 once the detection is done. Due to the force detection result, the VBUS_STAT[2:0] bits and IINDPM[4:0] register may be changed.

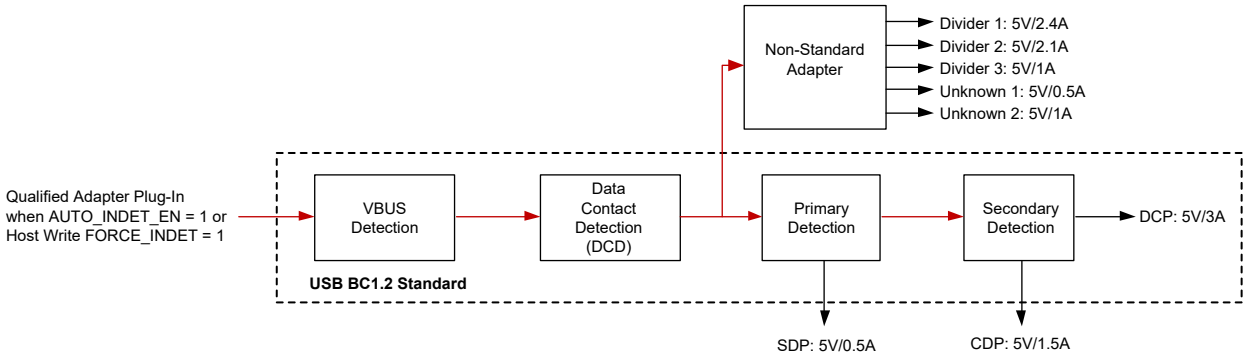


Figure 3. D+/D- Based USB BC1.2 Detection Flow

Table 1. Non-Standard Adapter Type Detection

Non-Standard Adapter	D+ Threshold	D- Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P8_VTH}	2.4
Divider 2	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P0_VTH}	2.1
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P8_VTH}	1
Unknown 2	V_{D+} = 1MΩ to 0V	V_{D-} = 3.3V	1
Unknown 1	Unknown	Unknown	0.5

Table 2. Input Current Limit Setting and Status

D+/D- Detection	Input Current Limit (I_{INDPM})	VBUS_STAT[2:0]
USB SDP (USB500)	500mA	001
USB CDP	1.5A	010
USB DCP	3.0A	011
Divider 3	1A	110
Divider 2	2.1A	110
Divider 1	2.4A	110
Unknown 5V Adapter 1	500mA	101
Unknown 5V Adapter 2	1000mA	101

DETAILED DESCRIPTION (continued)

REGN LDO Power-Up

The REGN low dropout regulator powers the internal bias circuits, HSFET and LSFET gate drivers and TS rail (thermistor pin). The nPG pin can also be pulled up to REGN. The REGN LDO enables when the following 3 conditions are satisfied and remain valid for 220ms delay time, otherwise the device stays in HIZ mode, and the REGN LDO keeps off.

1. V_{VBUS} > V_{VBUS_UVLOZ} (in forward direction Boost mode) or V_{VBUS} < V_{VBUS_UVLOZ} (in reverse direction OTG Buck mode).
2. A valid input source is detected by the poor power source detection.
3. Input power source type detection is done.

In HIZ state, the quiescent current drawn from VBUS is very small (less than I_{VBUS_HIZ}). System is only powered by the battery in HIZ mode.

DC/DC Converter Power-Up

The input current limit is set when input source detection is completed, then the VBUS_STAT[2:0] bits update to indicate the input source type, the nPG changes to logic low to indicate the power good and the PG_STAT and PG_FLAG bits also give the corresponding indication. The 1.5MHz switching converter composed of LSFET and HSFET is enabled and can start switching. Converter is initiated with a soft-start when the system voltage is ramped up.

The BATFET remains on to charge the battery if the battery charging function is enabled, otherwise BATFET turns off.

The SGM41528 provides an auto-run battery discharge source (I_{BAT_DISCHG}, 11mA (TYP)) for 13ms to detect the battery presence prior to the charge starts. During normal operation (include HIZ mode or battery only operation), this discharge current also can be enabled by setting EN_BAT_DISCHG bit to 1.

At light load condition, if charging is disabled or the battery voltage is lower than V_{SYS_MIN}, the SGM41528 changes from PWM mode to PFM mode. The SYS and BUS voltage relationship decides the switching duty cycle during the PFM operation. Host can disable the PFM operation via writing PFM_DIS = 1. If the PFM mode is selected, the out-of-audio (OOA) feature can be chosen under PFM_OOA_DIS = 0 condition. In OOA operation mode, the converter switching frequency is larger than 20kHz even at extremely light load to prevent the audible range operation.

Input Current Optimizer (ICO)

The SGM41528 provides input current optimizer (ICO) to identify the input adapter source maximum power point. To avoid the input adapter source overload and staying in VINDPM, the ICO algorithm identifies maximum input current limit of the adapter automatically and updates this input current limit to ICO_ILIM[4:0] register.

The ICO function is default enabled, and it can be disabled by the host through setting EN_ICO bit to 0. After a DCP type power source is detected, the ICO algorithm runs automatically when EN_ICO bit is valid. The host can set FORCE_ICO bit to force the ICO algorithm under EN_ICO bit to 1 condition. Refer to Table 3.

The actual input current limit is reported by ICO_ILIM[4:0] register in ICO mode, while it is decided by the IINDPM[4:0] register when out of ICO mode. In addition, the actual input current is also limited by an external resistor at ILIM pin when EN_ILIM = 1.

Table 3. Automatic ICO Operation

Input Source	Input Current Limit (I_{INDPM})	Automatic ICO Mode when EN_ICO = 1
USB SDP (USB500)	500mA	Disable
USB CDP	1.5A	Disable
USB DCP	3.0A	Enable
Divider 3	1A	Disable
Divider 2	2.1A	Disable
Divider 1	2.4A	Disable
Unknown 5V Adapter 1	500mA	Disable
Unknown 5V Adapter 2	1000mA	Disable

DETAILED DESCRIPTION (continued)

When the ICO algorithm is activated, it runs to dynamically and continuously adjust the input current limit using ICO_ILIM[4:0] register. During the adjustment, the ICO_STAT[1:0] and ICO_FLAG bits change until they are finally set. The operation of ICO algorithm depends on the battery voltage as following:

Case 1: When V_{BAT} < V_{SYS_MIN}, the device starts ICO algorithm by ICO_ILIM[4:0] register with an initial value that equals the I_{INDPM}. Where the I_{INDPM} is the maximum input current limit that determined by the system.

Case 2: When V_{BAT} > V_{SYS_MIN}, the device starts ICO algorithm by ICO_ILIM[4:0] register with an initial value of 500mA. The 500mA is the minimum input current limit which minimizes the input power source overload.

During the optimization, if VINDPM is triggered, the ICO algorithm decreases the input current limit (the dynamic ICO_ILIM[4:0] register) to avoid input source overloading. When the maximum input current limit is detected, the ICO_ILIM[4:0] register reflects the optimal maximum input current limit which is not trigger VINDPM. The ICO_FLAG bit is set and the ICO_STAT[1:0] bits are updated to 10 to indicate the maximum input current detected.

In above case 1, if both VINDPM and IINDPM are not triggered at ICO_ILIM[4:0] initial value, the ICO_ILIM[4:0] register keeps the initial value and the ICO_STAT[1:0] = 01 to indicate the ICO optimization is in process. If the load becomes heavy, the VINDPM still not be triggered but IINDPM is triggered, the ICO algorithm is also completed, the ICO_ILIM[4:0] register keeps the initial value still, the ICO_FLAG bit is set and ICO_STAT[1:0] bits are updated to 10 to indicate the maximum input current detected.

In above case 2, if the VINDPM is not triggered and the converter is under light load condition, the ICO_ILIM[4:0] gives the input current limit a little higher than the actual input current (500mA minimum input current limit). The ICO_STAT[1:0] bits remain 01 to indicate the ICO optimization is in process. If the load becomes heavy, the ICO algorithm automatically runs to set new ICO_ILIM[4:0] register value.

Once the ICO algorithm is completed (ICO_STAT[1:0] = 10), the ICO_ILIM[4:0] register will keep un-change unless one of the following events occurs. Each of the following events can force the ICO algorithm to run again and reset the ICO_STAT[1:0] bits to 01:

1. EN_HIZ bit is toggled or re-plugin the input source.
2. Host changes the IINDPM[4:0] register.
3. Host changes the VINDPM[4:0] register.
4. Host sets the FORCE_ICO bit to 1.
5. Resume from VBUS_OVP.

OTG Buck Mode

The SGM41528 supports USB On-The-Go (OTG). When a load device is connected to the USB port, the converter can operate as a Buck synchronous converter (Buck mode) with 1.5MHz switching frequency to supply power from the battery to that load. The USB OTG output current limit is programmable from 500mA to 2A (default). Converter will be set to Buck mode if at least 30ms is passed from enabling this mode (EN_OTG bit = 1) and the following conditions are satisfied:

1. V_{BAT} > V_{OTG_BAT}.
2. V_{VBUS} < $V_{VBUS\_PRESENT}$.
3. TS pin voltage is out of V_{BHOTx} and V_{BCOLDx} range.

The default output Voltage is set to V_{VBUS} = 5.1V (via OTG_VLIM[3:0] register) and is maintained as long as V_{BAT} is above V_{OTG_BAT}, and the V_{VBUS} is above $V_{VBUS\_PRESENT}$. The output current can reach up to the programmed value by OTG_ILIM[3:0] register (2A). The VBUS_STAT[2:0] status bits are set to 111 in Buck mode (OTG).

In OTG Buck mode, the SGM41528 default works in PFM mode at light load to improve the efficiency. The SYS and BUS voltage relationship decides the switching duty cycle. Host can disable the OTG PFM operation via writing PFM_DIS bit. If the PFM mode is selected, the out-of-audio (OOA) feature can be chosen under PFM_OOA_DIS = 0 condition. In OOA operation mode, the converter switching frequency is larger than 20kHz even at extremely light load to prevent the audible range operation.

DETAILED DESCRIPTION (continued)

Host Mode and Default Mode Operation with Watchdog Timer

After power-on reset (POR), the SGM41528 starts in default mode (standalone) with all registers reset to default values as if the watchdog timer is expired. When the host is in sleep mode or there is no host, the device stays in the default mode in which the SGM41528 operates like an autonomous charger. After 16.5 hours (default fast charging safety timer), the device stops charging the battery by turning off the BATFET, while the Boost converter continuously supplies the system load without shutdown.

Most of the flexibility features of the SGM41528 become available in the host mode when the device is controlled by a host with I²C. By setting the WD_RST bit to 1, the device changes to host mode. In this mode, the WD_STAT bit is low and all device parameters can be programmed in order to prevent the device watchdog reset from going back to the default mode, the host must disable the watchdog timer by writing 00 to WATCHDOG[1:0], or consistently reset the watchdog timer before expiry by writing 1 to WD_RST bit to prevent WD_STAT bit from being set. Every time a 1 is written to WD_RST bit, the watchdog timer will restart counting. Therefore, it should be reset again before overflow (expiry) to keep the device in the host mode. The SGM41528 goes back to default mode and resets all related registers when the watchdog timer expires.

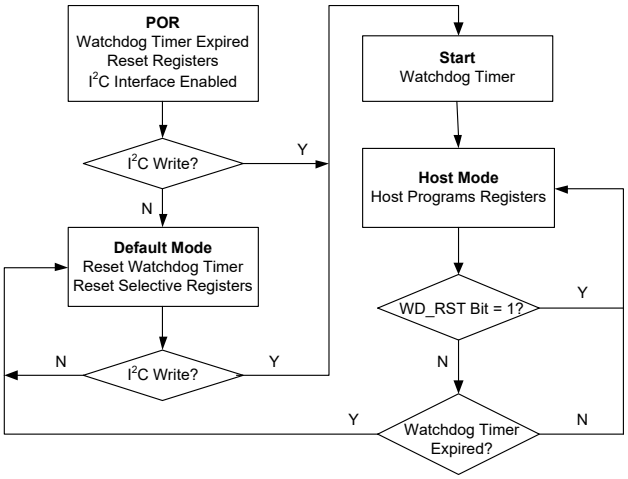


Figure 4. Watchdog Timer Flow Chart

Battery Charging Management

The SGM41528 is designed for charging 2-cell Li-Ion or Li-polymer batteries with a charge current up to 2.2A (MAX). The battery connection switch (BATFET) is in the charge or discharge current path and features low on-resistance to allow high efficiency and low voltage drop.

Charging Cycle in Autonomous Mode

Charging is enabled if EN_CHG = 1 and nCE pin is pulled low. In default mode, the SGM41528 runs a charge cycle with the default parameters itemized in Table 4. At any moment, the host can be controlled by changing to the host mode.

Table 4. Default Charging Parameter Settings

Default Mode	SGM41528
Charging Voltage (V_{REG})	8.4V
Charging Current (I_{CHG_REG})	1A
Pre-Charge Current (I_{PRECHG})	150mA
Termination Current (I_{TERM})	150mA
Temperature Profile	JEITA Enable
Charging Safety Timer	16.5h

Start a New Charging Cycle

If the converter can start switching and all the following conditions are satisfied, a new charge cycle starts:

• NTC temperature fault is not asserted (TS pin).
• Safety timer fault is not asserted.
• Charging enabled (2 conditions: EN_CHG bit = 1, nCE pin is low).
• Battery voltage is below the programmed full charge level (V_{REG}).

A new charge cycle starts automatically if battery voltage falls below the recharge threshold level (V_{REG} - 100mV or V_{REG} - 200mV configured by VRECHG[1:0] bits). Also, if the charge cycle is finished, a new charging cycle can be initiated by toggling of the nCE pin or EN_CHG bit.

Normally a charge cycle terminates when the charge voltage is above the recharge threshold level and the charging current falls below the termination threshold if the device is not in thermal regulation or dynamic power management (DPM) mode.

DETAILED DESCRIPTION (continued)

Charge Status Report

The charge status bits (CHRG_STAT[2:0]) indicate the charging phases of the device as below:

- 000 = Not Charging
- 001 = Trickle Charge
- 010 = Pre-Charge
- 011 = Fast Charge (CC Mode)
- 100 = Taper Charge (CV Mode)
- 101 = Top-Off Timer Active
- 110 = Charge Termination

When the device changes to any of the above statuses, or the charge cycle is completed, the nINT pin is pulsed to notify the host.

Battery Charging Profile

The SGM41528 features a full battery charging profile with five phases. When a charging cycle starts, the battery voltage (V_{BAT}) is tested and appropriate current and voltage regulation levels are selected as shown in Table 5. Depending on the detected status of the battery, the proper phase is selected to start or for continuation of the charging cycle. The five phases are: trickle charge (battery voltage too low), pre-charge, constant current, constant voltage and an optional top-off trickle charging phase.

Note that in the DPM or thermal regulation modes, normal charging functions are temporarily modified: the charge current is less than the value in the register; termination is disabled, and the charging safety timer is slowed down by counting at half clock rate.

Table 5. Charging Current Setting Based on V_{BAT}

V_{BAT} Voltage	Selected Charging Current	Default Value in the Register	CHRG_STAT[2:0]
$V_{BAT} < V_{BAT\_SHORT}$	I_{SHORT}	70mA	001
$V_{BAT\_SHORT} < V_{BAT} < V_{BAT\_LOW}$	I_{PRECHG}	150mA	010
$V_{BAT} > V_{BAT\_LOW}$	I_{CHG}	1000mA	011

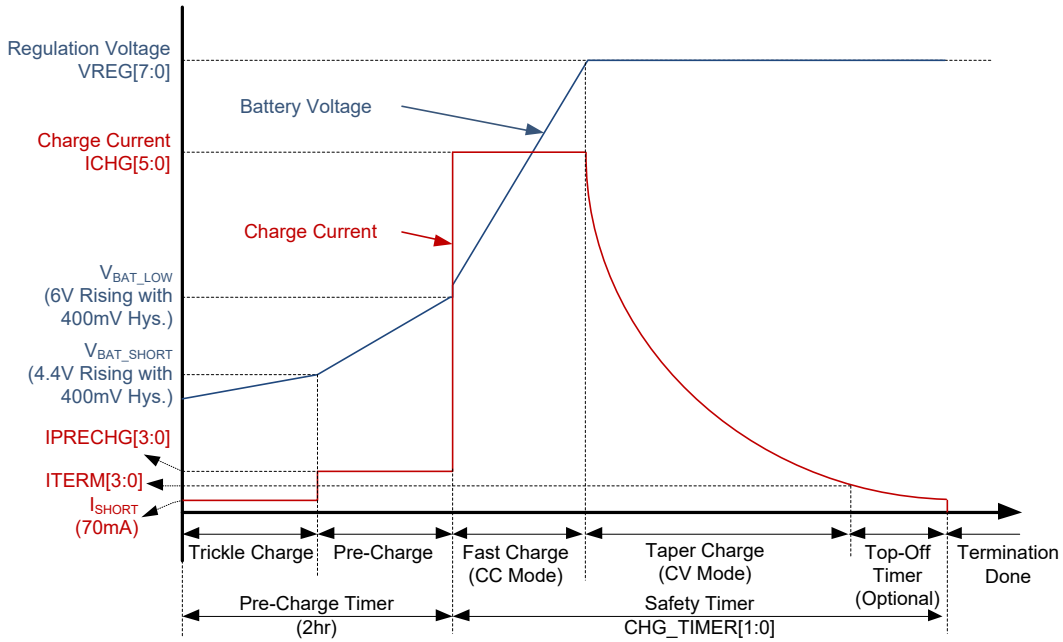


Figure 5. Battery Charging Profile

DETAILED DESCRIPTION (continued)

Charge Termination

A charge cycle is terminated when the battery voltage is higher than the recharge threshold and the charge current falls below the programmed termination current. Unless there is a high power demand for system and it needs to operate in supplement mode, the BATFET turns off at the end of the charge cycle. Even after termination, the Boost converter operates continuously to supply the system.

CHRG_STAT[2:0] bits are set to 110 and a negative pulse is sent to nINT pin after termination.

If the charger is regulating input current, input voltage or junction temperature instead of charge current, termination will be temporarily prevented. EN_TERM bit is a termination control bit and can be set to 0 to permanently disable termination before it happens.

Due to offset of the internal current comparator, the termination charge current may be much higher (40% TYP) than the set value when it is set too low (50mA TYP). A delay in termination can be added (optional) as a compensation for comparator offset using a programmable top-off timer. During the delay, constant voltage charge phase continues and gives the falling charge current the chance to drop closer to the programmed value. The top-off delay timer has the same restrictions of the safety timer. In other words, if the safety timer is suspended under certain conditions, the top-off timer will also be suspended or if the safety timer is slowed down, the top-off timer will also be slowed down. Code 101 in CHRG_STAT[2:0] indicates that the top-off timer is valid. The CHRG_STAT[2:0] bits change to 110 after the top-off timer expires. And the nINT pin reports a negative pulse to notify the host.

Any of the following events resets the top-off timer:

1. Disable to enable transition of nCE (charge enable).
2. A low to high change in the status of termination.
3. Set REG_RST bit to 1.

The setting of the top-off timer is applied at the time of termination detection and unless a new charge cycle is started, modifying the top-off timer parameters after termination has no effect. A negative pulse is sent to nINT when top-off timer is started or ended. If set CHRG_MASK bit to 1, the CHRG_STAT[2:0] bits change will not produce nINT pulse.

Temperature Qualification

The charging current and voltage of the battery must be limited when battery is cold or hot. A thermistor input for battery temperature monitoring is included in the device that can protect the battery based on JEITA guidelines. There is no battery temperature protection when Boost or Buck converter stops switching.

Compliance with JEITA Guideline

JEITA guideline (April 20, 2007 release) is implemented in the device for safe charging of the Li-Ion battery. JEITA highlights the considerations and limits that should to be considered for charging at cold or hot battery temperatures. High charge current and voltage must be avoided outside normal operating temperatures (typically 0℃ and 60℃). Four temperatures levels are defined by JEITA from T1 (minimum) to T4 (maximum). Outside this range, charging should be stopped. The corresponding voltages sensed by NTC are named V_{T1} to V_{T4}. Due to the sensor negative resistance, a higher temperature results in a lower voltage on TS pin. The battery cool range is between T1 and T2, the warm range is between T3 and T4. Charge must be limited in the cool and warm ranges.

One of the conditions for starting a charge cycle is having the TS voltage within V_{T1} to V_{T4} window limits. If during the charge, battery gets too cold or too hot and TS voltage exceeds the T1 - T4 limits, charging is suspended (zero charge current) and the controller waits for the battery temperature to come back within the T1 to T4 window.

JEITA recommends reducing charge current to 1/2 of fast charging current or lower at cool temperatures (T1 - T2). For warmer temperature (within T3 - T4 range), charge voltage is recommended to be kept below 4.1V/cell.

The SGM41528 follows the JEITA requirement by its flexible charge parameter settings. At warm temperature range (T3 - T4), the charge voltage can be set to 8.0V (default), 8.3V, V_{REG}, or charge suspend through JEITA_VSET[1:0] register. At cool temperatures (T1 - T2), the fast charge current can be set to 100%, 40%, or 20% (default) of I_{CHG} or charge suspend through JEITA_ISETC[1:0] bits. The charge termination is still enabled (if EN_TERM = 1) when the "cool" or "warm" temperature is detected.

DETAILED DESCRIPTION (continued)

A 103AT-2 type thermistor is recommended to use for the SGM41528. Other thermistors may be used and bias network (see Figure 6) can be calculated based on the following equations:

$$R_{T2} = \frac{V_{REGN} \times R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T4}}\right)}{R_{THHOT} \times \left(\frac{V_{REGN}}{V_{T4}} - 1\right) - R_{THCOLD} \times \left(\frac{V_{REGN}}{V_{T1}} - 1\right)} \quad (1)$$

$$R_{T1} = \frac{\left(\left(\frac{V_{REGN}}{V_{T1}}\right) - 1\right)}{\left(\frac{1}{R_{T2}}\right) + \left(\frac{1}{R_{THCOLD}}\right)} \quad (2)$$

where, V_{T1}, V_{T4} and V_{REGN} are characteristics of the device and R_{THCOLD} and R_{THHOT} are thermistor resistances (R_{TH}) at desired T1 (Cold) and T4 (Hot) temperatures. Select T_{COLD} = 0℃ and T_{HOT} = 60℃ for Li-Ion or Li-polymer batteries. For a 103AT-2 type thermistor R_{THCOLD} = 27.28kΩ and R_{THHOT} = 3.02kΩ, the calculation results are: R_{T1} = 5.24kΩ and R_{T2} = 30.31kΩ.

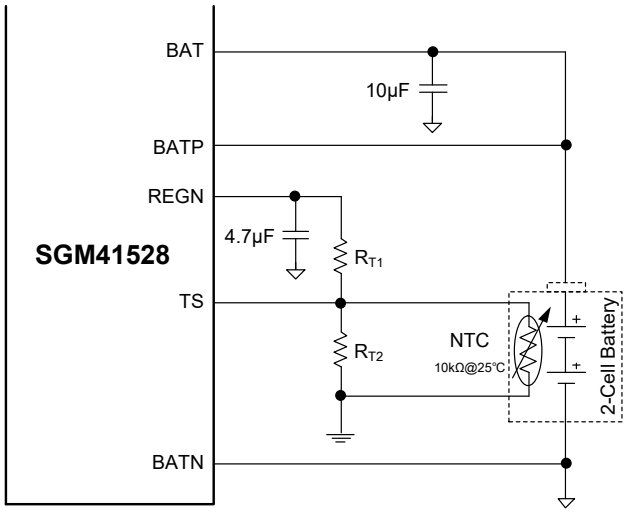


Figure 6. Battery Thermistor Connection and Bias Network

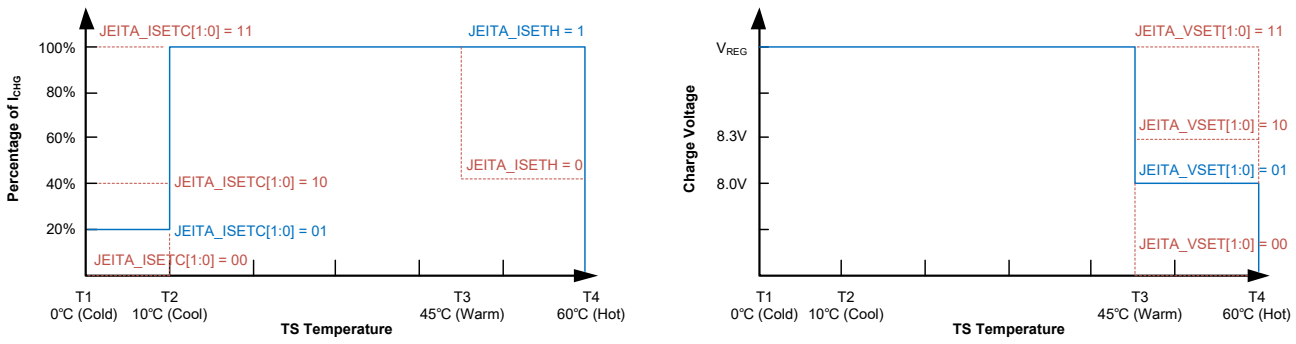


Figure 7. TS Based Current and Voltage Settings

DETAILED DESCRIPTION (continued)

OTG Buck Mode Temperature Monitoring

The device is capable to monitor the battery temperature for safety during the OTG Buck mode. The temperature must remain within the V_{BCOLDx} to V_{BHOTx} thresholds, otherwise the OTG mode will be suspended and VBUS_STAT[2:0] bits are set to 000. Moreover, TS_STAT[2:0] bits are updated to report OTG mode cold or hot condition. Once the temperature returns within the right window, the OTG Buck mode is resumed and TS_STAT[2:0] bits are cleared to 000 (normal).

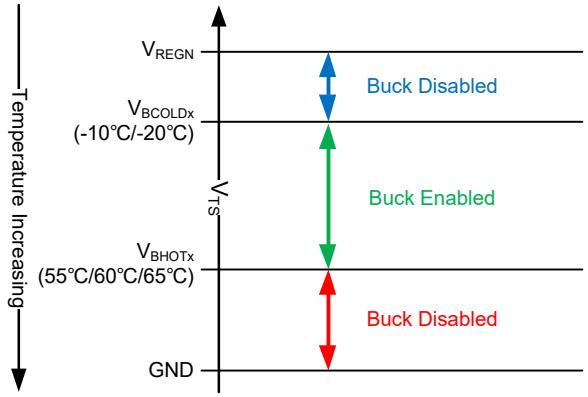


Figure 8. TS Pin Thermistor Temperature Window Settings in OTG Buck Mode

Safety Timer

Abnormal battery conditions may result in prolonged charge cycles. An internal safety timer is considered to stop charging in such conditions. If the charging safety timer timeout occurs, TMR_STAT bit is set and a negative pulse is sent to nINT pin. This feature is optional and can be disabled by setting EN_TIMER bit to 0.

The safety timer counts at half clock rate when charger is under input voltage regulation, input current regulation or thermal regulation, and the actual charge current is always decreased. As an example, if the charging safety timer is set to 7.5 hours and the charger is under input current regulation (IINDPM_STAT = 1) in the whole charge cycle, the actual safety time will be 15 hours. Clearing the TMR2X_EN bit will disable the half clock rate feature. If TMR2X_EN = 1 and SGM41528 is already in DPM or thermal regulation, writing the TMR2X_EN = 0 will not take effect.

The safety timer is paused if supplement mode occurs or a fault occurs which disables the charging. The TMR2X_EN bit also has no effect in this condition because the timer counting has stopped. It will resume once the fault condition is removed. If charging cycle is stopped and restarted by toggling nCE pin or EN_CHG bit, the timer resets and restarts a new timing.

The fast charge safety timer can be reset by the following events:

1. Stop and restart the charging cycle (change EN_CHG bit, toggle nCE pin, or charged battery falls below recharge threshold).
2. Charge status changes between pre-charge and fast charge (in default mode or host mode).

The pre-charge safety timer including both trickle charge phase and pre-charge phase is fixed 2 hours counter and runs when $V_{BAT} < V_{BAT\_LOW}$, it follows the same rules as the fast charge safety timer in terms of reset, getting suspended, and half-rate counting when TMR2X_EN is valid.

Narrow Voltage DC (NVDC) Design in SGM41528

The SGM41528 features an NVDC design using the BATFET that connects the system and battery. By using the linear region of the BATFET, the charger regulates the system bus voltage (SYS pin) above the minimum setting using Boost converter even if the battery voltage is very low. MOSFET linear mode allows the large voltage difference between SYS and BAT pins to appear as V_{DS} across the switch while conducting and charging battery. SYS_MIN[3:0] register sets the minimum system voltage (default 7V). If the system is in minimum system voltage regulation, VSYS_STAT bit is set.

The BATFET operates in linear region when the battery voltage is lower than the minimum system voltage. The system voltage is regulated at 300mV (TYP) higher than the minimum system voltage. As the battery gradually gets charged, until its voltage rises above the minimum system voltage, the BATFET changes from linear mode to fully turned-on mode, and the system voltage keeps V_{DS} of BATFET higher than the battery voltage.

The system voltage is always regulated to 100mV (TYP) above the battery voltage if:

1. The charging is terminated.
2. Charging is disabled and the battery voltage is above the minimum system voltage setting.

DETAILED DESCRIPTION (continued)

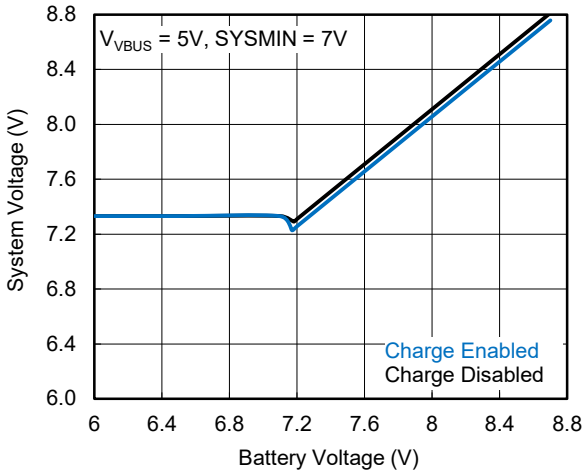


Figure 9. System Voltage vs. Battery Voltage

SGM41528 Dynamic Power Management (DPM)

The SGM41528 features a dynamic power management (DPM). To implement DPM, the device always monitors the input current and voltage to regulate power demand from the source and avoid input adapter overloading or to meet the maximum current limits specified in the USB specifications. Overloading an input power source may result in either the voltage tending to fall below the input voltage limit (V_{INDPM}) or the current trying to exceed the input current limit (I_{INDPM} or ICO_ILIM[4:0] or ILIM pin setting). With DPM, the device keeps the VSYS regulated to its minimum setting by reducing the battery charge current adequately such that the input parameter (voltage or current) does not exceed the limit. In other words, charge current is reduced to satisfy $I_{IN} \le I_{INDPM}$ or $V_{IN} \ge V_{INDPM}$ whichever occurs first. DPM can be either an I_{IN} type (IINDPM) or V_{IN} type (VINDPM), depending on which limit is reached.

Changing to the supplement mode may be required if the charge current is decreased and reached to zero while the input is still overloaded. In this case, the charger reduces the system voltage below the battery voltage to allow operation in the supplement mode and provide a portion of system power demand from the battery through the BATFET.

The IINDPM_STAT or VINDPM_STAT status bits are set during an IINDPM or VINDPM respectively. Figure 10 summarizes the DPM behavior (IINDPM type) for a design example with a 5V/3A adapter, 6.5V battery, 1.5A charge current setting and 7V minimum system voltage setting.

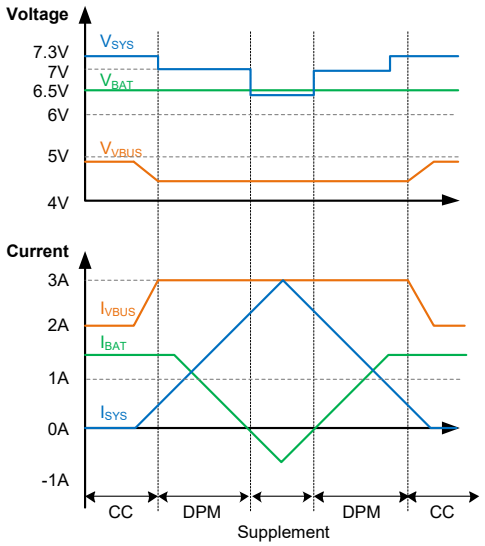


Figure 10. Input, Battery and System Voltage and Currents in DPM

Battery Supplement Mode

When the system is under heavy load, the system voltage may drop below the battery voltage, the BATFET gradually starts to turn on. At low discharge currents, the BATFET gate voltage is regulated (R_{DS} modulation). At higher currents, the BATFET will turn fully on (reaching its lowest R_{DSON}). From this point, increasing the discharge current will linearly increase the BATFET V_{DS} (determined by $R_{DSON} \times I_D$). Using the MOSFET linear mode at lower currents prevents swinging oscillation of entering and exiting the supplement mode.

BATFET gate regulation V-I characteristic is shown in Figure 11. If the battery voltage falls below its minimum depletion, the BATFET turns off and exits supplement mode.

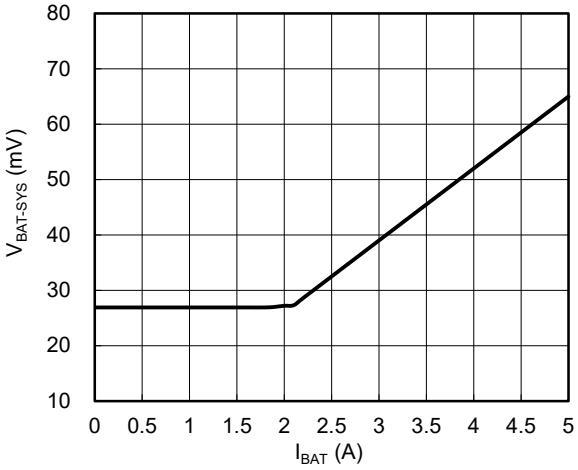


Figure 11. BATFET Gate Regulation V-I Curve

DETAILED DESCRIPTION (continued)

16-Bit ADC

The integrated 16-bit ADC in SGM41528 allows the user to get critical system information for optimizing the charger behavior. The ADC related functions are controlled by ADC control register. The ADC_EN bit gives the option to enable or disable the ADC for power save purpose. The ADC conversion behavior can be set to continuous or one-shot mode through the ADC_RATE bit. The ADC_EN bit is automatically cleared once a one-shot conversion cycle completes. Re-assert ADC_EN bit can start a new conversion.

Set ADC_EN bit to 1 to enable the ADC. The ADC can be operated when VBAT or VBUS is valid (V_{BAT} > V_{BAT_UVLOZ} or V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}). The SGM41528 will not execute the ADC under both VBAT and VBUS are invalid, and the ADC result registers will not be updated. In addition, the SGM41528 resets ADC_EN bit without sending any pulse on nINT pin. The ADC behaves the same if the ADC_EN bit is set while all ADC channels' enable bits are 0. To ensure that ADC is running a conversion, it is recommended to read back ADC_EN bit after setting it to 1. The ADC conversion is interrupted if the charger mode changes during ADC conversion running (e.g. EN_OTG bit goes to 1, EN_HIZ bit goes to 1 or an adapter plug-in). The ADC resumes with the interrupted channel when the mode change is complete.

The sample speed is programmable via ADC_SAMPLE[1:0] bits, and the ADC conversion time (t_{ADC_CONV}) for each measurement is changed according to ADC_SAMPLE[1:0] bits setting. By default, the ADC function disable register (REG0x16) is set to 0x00 and all ADC channel will be converted in both continuous and one-shot conversion modes.

If one bit of ADC function disable register (REG0x16) is set to 1 before the conversion, the corresponding channel ADC conversion data is not updated to the ADC result registers. In this case, the data host read-back from the ADC result register is from the default POR value or the last valid ADC conversion. If one bit of ADC function disable register (REG0x16) is set to 1 during the ADC conversion cycle, the SGM41528 finishes this channel conversion in this cycle, and not converts this channel in next cycle.

In continuous conversion mode, as long as the ADC_EN bit is set to 1, the ADC circuitry is active even if all ADC channel conversion is disabled by REG0x16. In one-shot mode, the ADC_EN bit is cleared automatically if all ADC channel conversion is disabled. Once one bit in REG0x16 is set to 0, the ADC conversion begins soon.

In continuous conversion mode, the ADC_DONE_STAT bit keeps 0 and ADC_DONE_FLAG bit remains unchanged. The ADC_DONE_STAT and ADC_DONE_FLAG bits are set when a one-shot conversion is completed.

To exit the ADC measurement, one of following ways is possible to do:

1. Set the ADC_EN bit to 0. The ADC measurement stops immediately. The last valid ADC measurement value can be read back into the ADC measurement result registers.
2. Set all ADC function disable bits in REG0x16 to 1. The ADC stops after the current cycle measurement is completed.
3. Set the ADC_RATE bit to 1. The ADC conversion can be set to one-shot conversion mode. The ADC stops after one cycle measurement is completed.

If an adapter is plugged in, the ADC suspends, and it resumes after SGM41528 finishes the input source detection. Other than that, ADC conversion always keeps normal operation even a fault occurs in SGM41528.

DETAILED DESCRIPTION (continued)

Status Outputs Pins (nPG and nINT)

Power Good Indication (nPG)

When a good input source is connected to VBUS and input type is detected, the PG_STAT status bit goes high and the nPG pin goes low. A good input source is detected if all the following conditions on V_{VBUS} are satisfied and input type detection is completed:

• V_{VBUS} is in the operating range: $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$.
• Input source is not poor: $V_{VBUS} > V_{BAD\_SRC}$ (3.6V TYP) when I_{BAD_SRC} (7.6mA TYP) loading is applied. (Poor source detection.)
• Completed input source type detection.

nINT Interrupt Output Pin

When a new update occurs in the charger states, a 256μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the charger device and by receiving the interrupt, it can react and check the charger situation on time. By default, each of the following events will generate a nINT pulse.

1. Good input power source detected.
   a) $V_{VBUS} < V_{VBUS\_OV}$
   b) $V_{VBUS} > V_{BAD\_SRC}$ when I_{BAD_SRC} current is applied
2. Good input power source removed.
3. Entering junction temperature regulation.
4. Entering VINDPM regulation.
5. Entering IINDPM regulation.
6. Watchdog timer expired.
7. VBUS_STAT[2:0] bits change.
8. TS_STAT[2:0] bits change.
9. CHRG_STAT[2:0] bits change, including charge complete.
10. A rising edge on any of the *_STAT bits of REG0x0B to REG0x0E.
11. Battery over-voltage detected.
12. Junction temperature shutdown.
13. VBUS over-voltage detected.
14. Charge safety timer expired, including pre-charge timer expired.

If the event mask bit is set to 1, the corresponding nINT pulse does not send out when the event happens. For each event, there are three related bits:

1. STAT bit: holding the current status.
2. FLAG bit: holding nINT event information, ignore the current status.
3. MASK bit: prevent the event from sending out nINT.

When each of the above events occurs, the SGM41528 sends out a nINT pulse and reports the event source through the corresponding FLAG registers. After the host reads the FLAG register bits, they are automatically reset to 0, and to re-assert the FLAG requires a new rising edge on STAT bit.

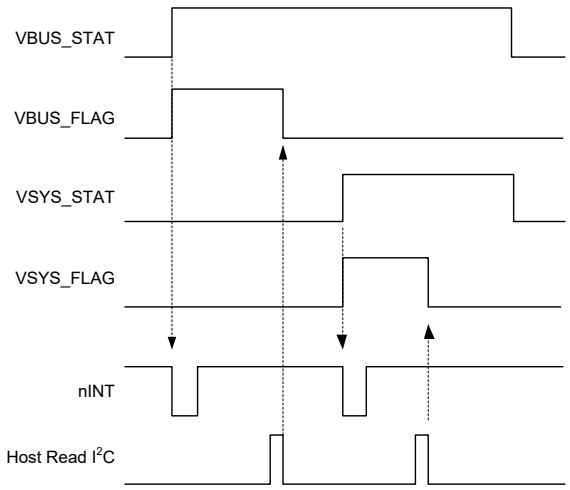


Figure 12. Example of nINT Generation Behavior

Input Current Limit on ILIM Pin

The device has an additional hardware pin on ILIM to clamp input current limit for safe operation. A resistor between ILIM pin and GND can set the clamped input current limit as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

For example, if EN_ILIM = 1 and the IINDPM[4:0] register is 3A , a 750Ω resistor is connected between ILIM and ground, the actual input current limit is clamped to 1.38A (K_{ILIM} = 1035 TYP). When ILIM pin voltage is higher than 0.8V, the SGM41528 clamps the input current and enters input current regulation. The same behavior as entering IINDPM through IINDPM[4:0] register, the IINDPM_STAT and IINDPM_FLAG bits are also set and SGM41528 reports a nINT if the IINDPM_MASK bit is 0.

DETAILED DESCRIPTION (continued)

When EN_ILIM = 1 and the input current is not clamped by ILIM pin, the ILIM pin voltage (V_{ILIM}, lower than 0.8V) is proportional to the actual input current. In this case, the input current can be monitored and calculated by:

$$I_{IN} = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8V} \quad (4)$$

For example, with a 750Ω ILIM resistor, the 0.4V ILIM voltage corresponds to 0.69A input current. If ILIM pin is shorted to GND, the ILIM won't help on limiting the input current and the limit is set by the IINDPM[4:0] register. If ILIM pin is open, the ILIM voltage will float above 0.8V, and the input current is limited to zero.

Setting EN_ILIM bit to 0 can disable the ILIM pin clamping function as well as the input current monitoring function. Either enable or disable ILIM pin function operation takes effect immediately.

SGM41528 Protection Features

Monitoring of Voltage and Current

During the converter operation, the input and system voltages (V_{VBUS} and V_{SYS}) and switch currents are constantly monitored to assure safe operation of the device in both Buck and Boost modes, as will be explained below.

Boost Mode Voltage and Current Monitoring

1. Input Under-Voltage (VBUS_UVP)

The Boost converter stops switching once VBUS voltage falls below V_{BAD_SRC} during operation. During VBUS under-voltage, the PG_STAT and PG_FLAG bits can be set, and a nINT pulse is asserted to notify the host. When the under-voltage condition disappears, the device automatically resumes switching.

2. Input Over-Voltage (VBUS_OVP)

The input voltage range for Boost mode operation is above V_{BAD_SRC} and below V_{VBUS_OV}. Converter switching will stop as soon as VBUS voltage exceeds V_{VBUS_OV} over-voltage limit. During VBUS over-voltage, the SGM41528 sets the VBUS_OVP_STAT and VBUS_OVP_FLAG bits, and reports a nINT pulse if the VBUS_OVP_MASK bit is set to 0. When the over-voltage condition disappears, the Boost converter automatically resumes switching again.

3. System Over-Voltage (SYSOVP)

During a system load transient, the device clamps the system voltage to protect the system components from over-voltage. The SYSOVP threshold is related to the battery voltage. When $V_{BAT} < V_{SYS\_MIN}$, the SYSOVP threshold is V_{SYS_MIN} + 360mV; when $V_{BAT} > V_{SYS\_MIN}$, the SYSOVP is V_{BAT} + 440mV. Once a SYSOVP occurs, switching stops to clamp any overshoot and a 16mA sink current is applied to SYS to pull the voltage down.

4. System Over-Current (SYSOCP)

To protect system from overloading or short-circuit event, the device continually compares V_{SYS} to V_{VBUS}. If the IINDPM is triggered and the heavy load further cause the SYS voltage drop to below VBUS voltage more than 250mV, the SGM41528 stops switching and automatically tries to resume from this fault condition. If 7 consecutive retry failures are detected, the EN_HIZ bit is set automatically. The SGM41528 sets the SYS_SHORT_FLAG and reports a nINT to host if the SYS_SHORT_MASK is 0.

OTG Buck Mode Voltage and Current Monitoring

In Buck mode, the QBLK (blocking FET) and LSFET (low-side switch) FET currents and VBUS voltage are monitored for protection.

1. Output Over-Voltage Protection for VBUS

In Buck mode, converter stops switching and exits Buck mode (by clearing EN_OTG bit) if VBUS voltage rises above regulation and exceeds the V_{OTG_OVP} over-voltage limit (6.03V TYP). A nINT pulse is sent and the OTG_FLAG bit is set high.

2. Output Over-Current Protection for VBUS

In OTG Buck mode, when OTG output current is higher than OTG_ILIM[3:0] bits and VBUS drops to lower than V_{BAD_SRC}, the Buck converter stops switching. The device automatically tries to resume from this fault condition. After 7 consecutive retry failures, the EN_OTG bit is cleared, the OTG_FLAG bit is set, and a nINT is pulsed to notify the host.

DETAILED DESCRIPTION (continued)

SGM41528 Thermal Regulation and Shutdown

Boost Mode Thermal Protections

Internal junction temperature (T_J) is always monitored to avoid overheating. A limit of +120℃ is considered for maximum IC surface temperature in Boost mode and if T_J intends to exceed this level, the device reduces the charge current to keep maximum temperature limited to +120℃ (thermal regulation mode) and sets the TREG_STAT bit to 1. As expected, the charging current is always lower than programmed value under thermal regulation conditions. The safety timer runs at half clock rate, and the charge termination is disabled. The thermal regulation temperature is programmable from +60℃ to +120℃ with 20℃ step.

If the junction temperature exceeds T_{SHUT} (+150℃), thermal shutdown protection arise in which the converter is turned off, the SGM41528 sets the TSHUT_STAT and TSHUT_FLAG bits, and reports a nINT pulse if the TSHUT_MASK bit is set to 0. When the device recovers and T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the converter resumes automatically.

If the charge is disabled, the thermal regulation mode doesn't work, but the thermal shutdown protection keeps work.

OTG Buck Mode Thermal Protections

Similar to Boost mode, T_J is monitored in OTG Buck mode for thermal shutdown protection. If junction temperature exceeds T_{SHUT} (+150℃), the Buck mode stops switching and the EN_OTG bit is reset to 0 automatically. Similarly, the SGM41528 sets the TSHUT_STAT and TSHUT_FLAG bits, and reports a nINT pulse if the TSHUT_MASK bit is set to 0. If T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the Buck mode can recover again by re-enabling EN_OTG bit by the host.

Battery Protections

Battery Over-Voltage Protection (BATOVP)

The over-voltage protection threshold of the battery pin is 4% above the programmed battery regulation voltage (V_{REG}) during charging phase. In case of a BATOVP, charging stops right away, the SGM41528 sets the BATOVP_STAT and BATOVP_FLAG bits, and reports a nINT pulse if the BATOVP_MASK bit is set to 0.

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM41528 parameters and get status reports. I²C is well known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41528 operates as a slave device with address 0x6B (6BH). It has 38 8-bit registers, numbered from REG0x00 to REG0x25. A register read beyond REG0x25 (0x25) returns 0xFF.

Physical Layer

The standard I²C interface of SGM41528 supports standard mode and fast mode communication speeds. The frequency of stand mode is up to 100kbits/s, while the fast mode is up to 400kbits/s. Bus lines are pulled high by weak current source or pull-up resistors are in logic high state with no clocking when the bus is free. The SDA and SCL pins are open-drain.

DETAILED DESCRIPTION (continued)

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 13. All transactions begin by the master who applies a START condition on the bus lines to take over the bus and exchange data. In the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high-to-low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. After a START and before a STOP, the bus is considered busy. BTW, only a master can send out the START and STOP signals.

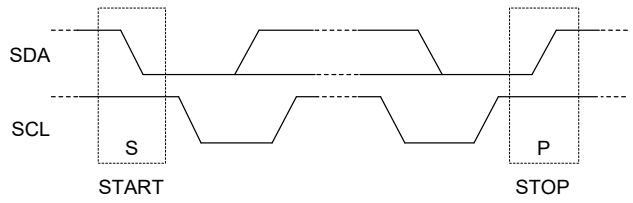


Figure 13. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

Data bit (high or low) must remain stable during clock HIGH period. The state of SDA can only change when SCL is LOW. For each data bit transmission, one clock pulse is generated by the master. Bit transfer in I²C is shown in Figure 14.

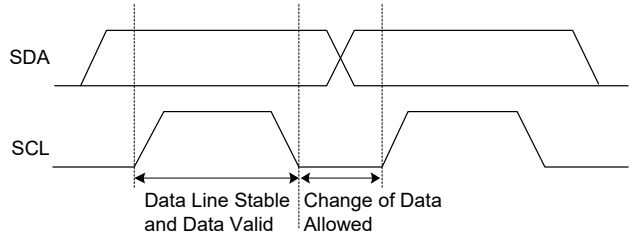


Figure 14. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 15 shows the byte transfer process with I²C interface.

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte has been received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including for the acknowledge ninth bit, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse and the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either STOP (P) to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a stop condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit ($R/\overline{W}$). $R/\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is also a WRITE, sending the register address that is supposed to be accessed in the next byte(s). The 7-bit slave address is 1101011b (0x6B). The address bit arrangement is shown below, as shown in Figure 16 and Figure 17.

DETAILED DESCRIPTION (continued)

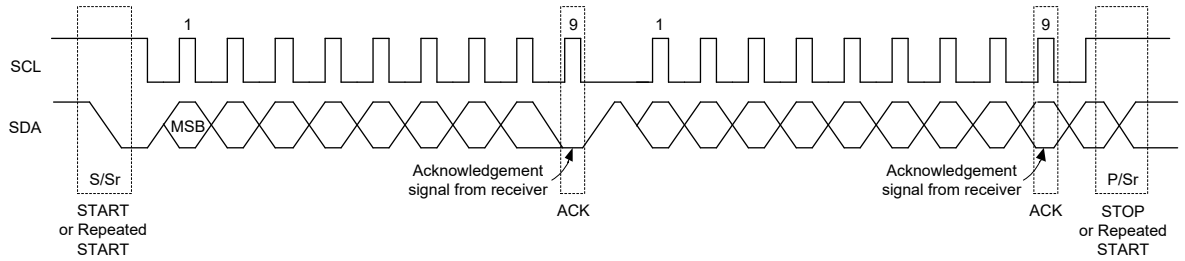


Figure 15. Byte Transfer Process

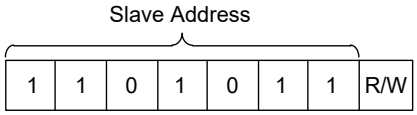


Figure 16. 7-Bit Address Format (0x6B)

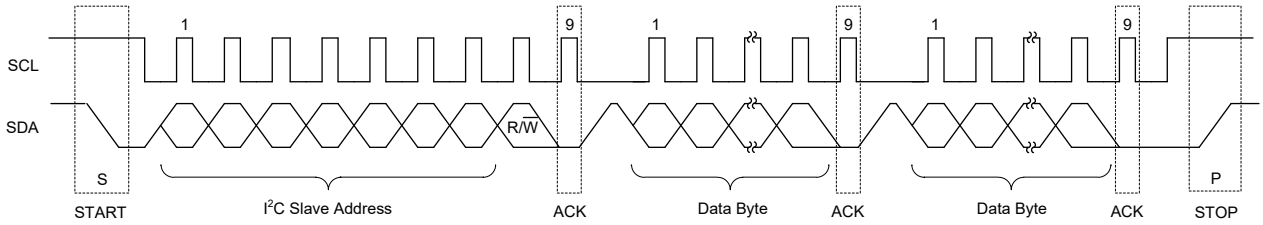


Figure 17. Data Transfer Transaction

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 18 for a single write data transfer. After receiving the ACK, the master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

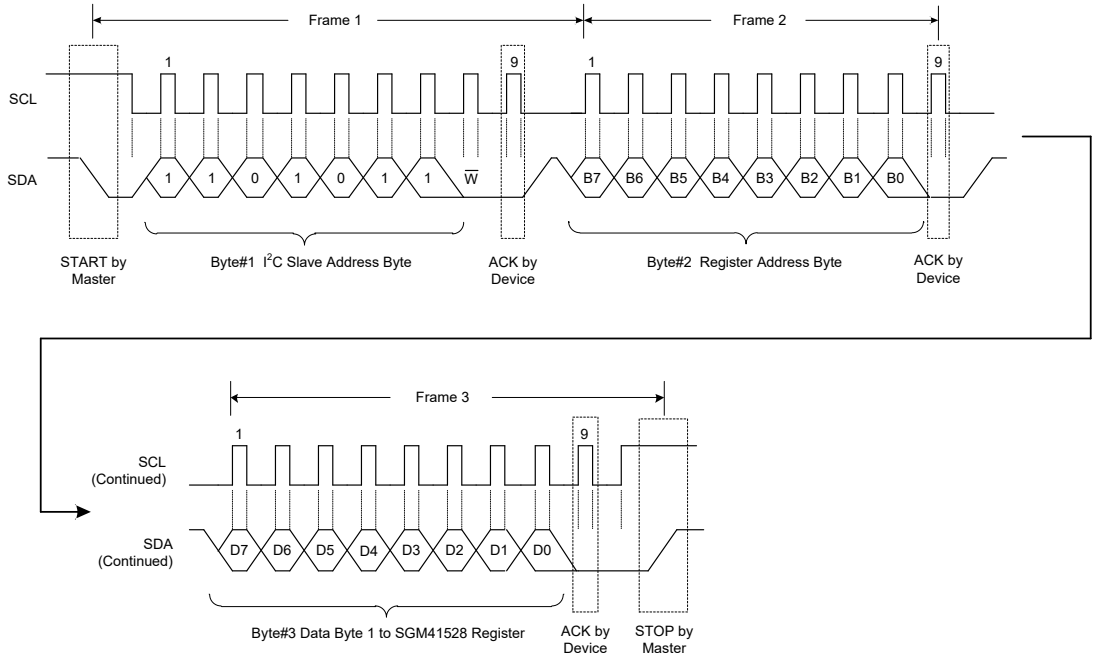


Figure 18. A Single Write Transaction

DETAILED DESCRIPTION (continued)

READ: If the master wants to read a single register (Figure 19), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, the master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

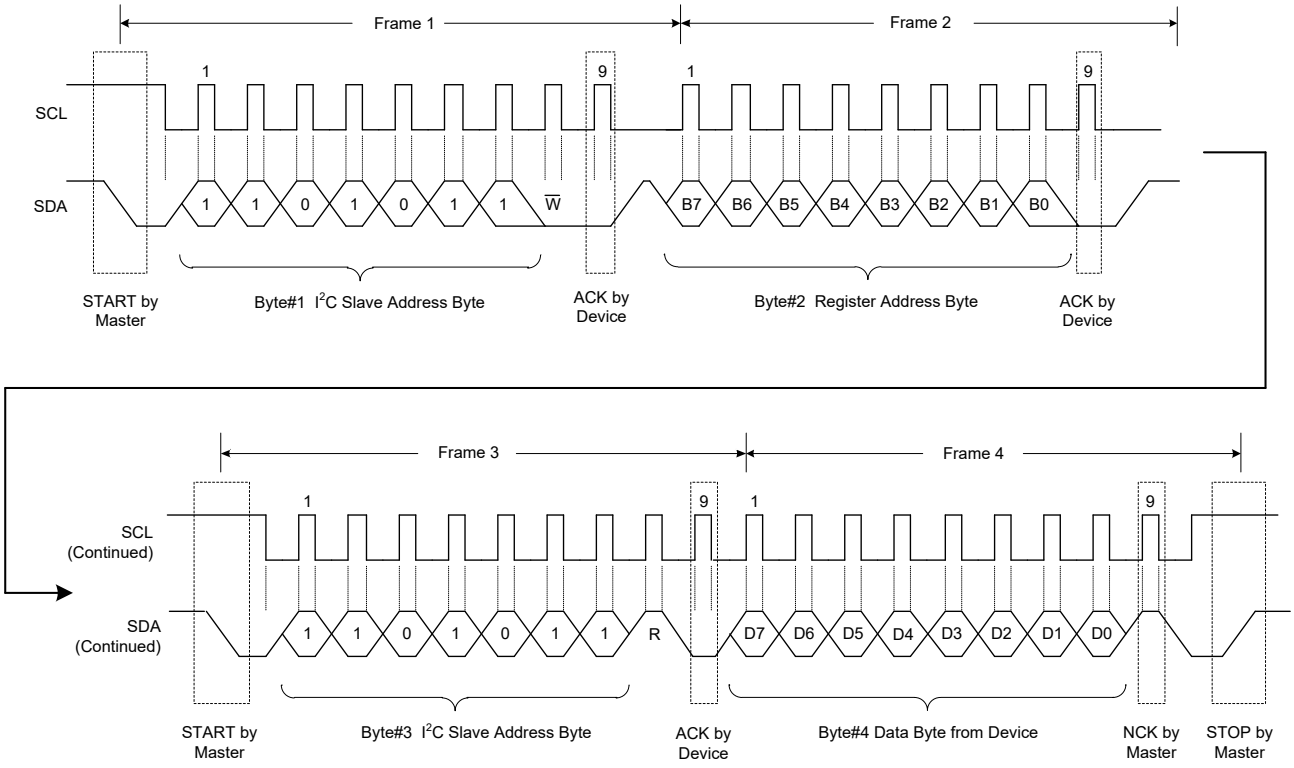


Figure 19. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41528 for REG0x00 through REG0x25 registers, as explained in Figure 20 and Figure 21.

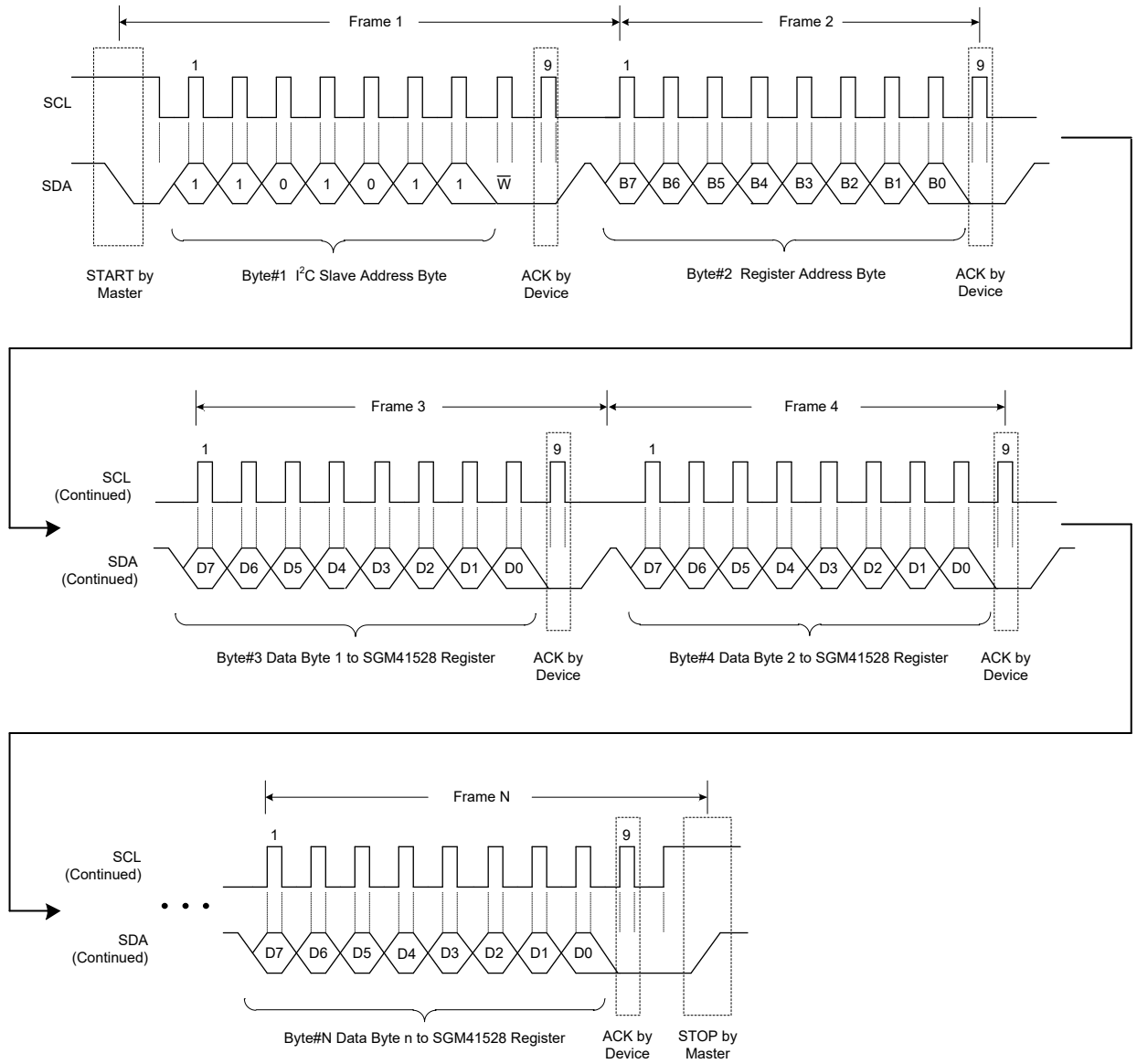


Figure 20. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

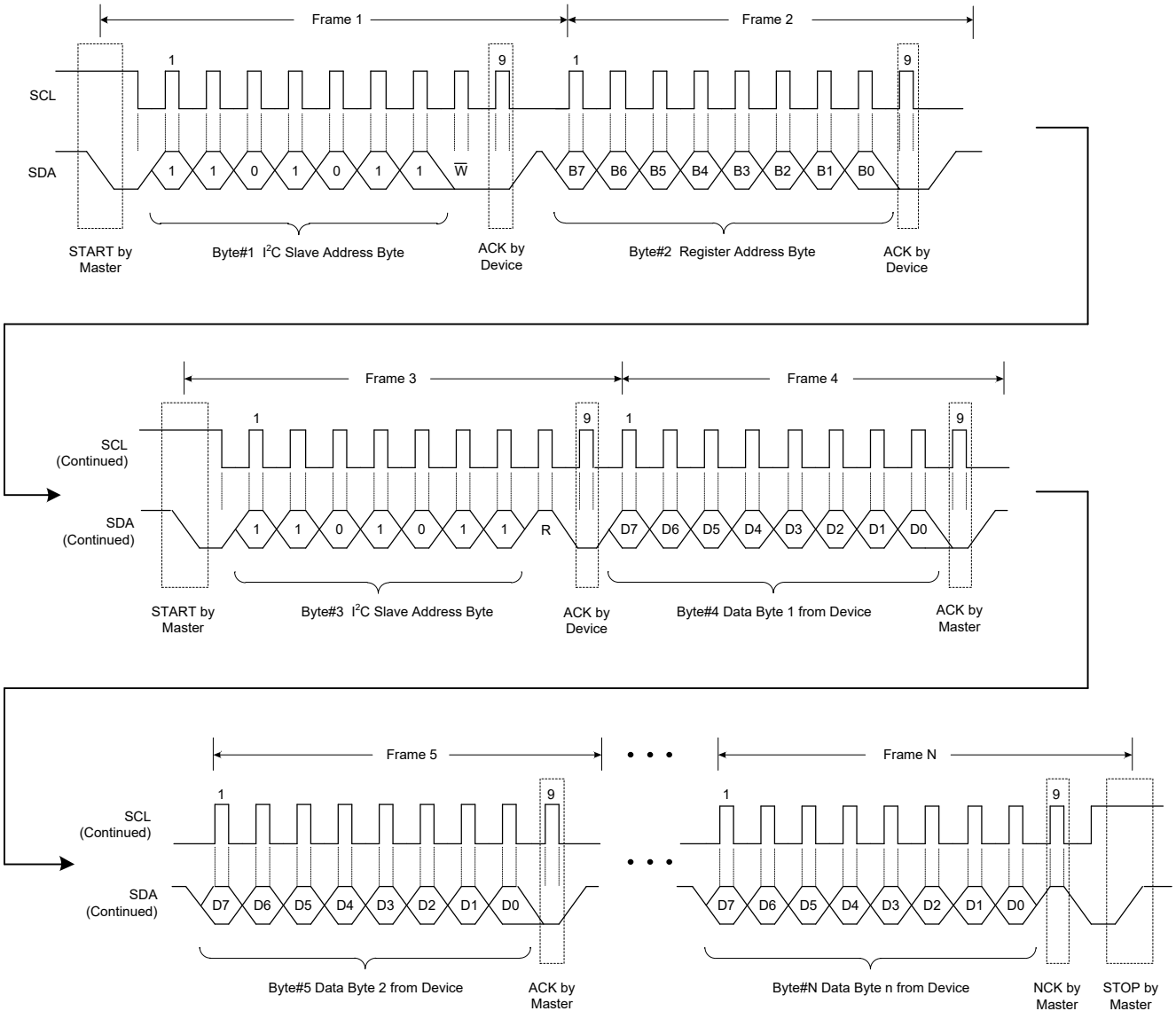


Figure 21. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Register Address Map

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE
CHARGE	0x0B[2:0]	0x0F[0]	0x12[0]	—	0x06[3]
VREG	—	—	—	0x00[7:0]	—
ICHG	—	—	—	0x01[5:0]	—
BATLOW	—	—	—	0x06[2]	—
IPRECHG	—	—	—	0x04[7:4]	—
TERM	—	—	—	0x04[3:0]	0x05[7]
VRECHG	—	—	—	0x06[1:0]	—
SAFETY TIMER	0x0E[4]	0x11[4]	0x14[4]	0x05[2:1]	0x05[3]
TOPOFF_TIMER	—	—	—	0x07[5:4]	—
TMR2X	—	—	—	—	0x05[0]
VINDPM	0x0B[5]	0x0F[5]	0x12[5]	0x02[4:0]	—
VINDPM_RST	—	—	—	—	0x02[7]
IINDPM	0x0B[6]	0x0F[6]	0x12[6]	0x03[4:0]	—
ILIM PIN	—	—	—	—	0x01[6]
ICO	0x0C[2:1]	0x10[1]	0x13[1]	—	0x03[5]
ICO_ILIM	0x0A[4:0]	—	—	—	—
FORCE_ICO	—	—	—	—	0x03[7]
FORCE_INDET	—	—	—	—	0x03[6]
AUTO_INDET	—	—	—	—	0x06[6]
VBUS_STAT	0x0C[6:4]	0x10[4]	0x13[4]	—	—
PG	0x0C[7]	0x10[7]	0x13[7]	—	—
SYS_MIN	0x0C[0]	0x10[0]	0x13[0]	0x07[3:0]	—
HIZ MODE	—	—	—	—	0x01[7]
BAT_DISCHG	—	—	—	—	0x02[6]
WATCHDOG	0x0B[3]	0x0F[3]	0x12[3]	0x05[5:4]	—
WD_RST	—	—	—	—	0x07[6]
OTG	0x0C[6:4]	0x11[0]	0x14[0]	—	0x06[7]
OTG_ILIM	—	—	—	0x09[7:4]	—
OTG_VLIM	—	—	—	0x09[3:0]	—
PFM	—	—	—	—	0x07[7]
PFM_OOA	—	—	—	—	0x02[5]
BHOT	—	—	—	0x08[7:6]	—
BCOLD	—	—	—	0x08[5]	—
JEITA_VSET	—	—	—	0x08[4:3]	—
JEITA_ISETH	—	—	—	0x08[2]	—
JEITA_ISETC	—	—	—	0x08[1:0]	—
TS_STAT	0x0D[2:0]	0x10[2]	0x13[2]	—	—
TREG	0x0B[4]	0x0F[4]	0x12[4]	0x06[5:4]	—
TSHUT	0x0E[6]	0x11[6]	0x14[6]	—	—
VBUS_OVP	0x0E[7]	0x11[7]	0x14[7]	—	—
BATOVP	0x0E[5]	0x11[5]	0x14[5]	—	—
SYS_SHORT	—	0x11[3]	0x14[3]	—	—
ADC	0x0B[7]	0x0F[7]	0x12[7]	—	0x15[7]
ADC_RATE	—	—	—	0x15[6]	—
ADC_SAMPLE	—	—	—	0x15[5:4]	—
IBUS_ADC	0x17[7], 0x17[3:0] 0x18[7:0]	—	—	—	0x16[7]
ICHG_ADC	0x19[3:0] 0x1A[7:0]	—	—	—	0x16[6]
VBUS_ADC	0x1B[4:0] 0x1C[7:0]	—	—	—	0x16[5]
VBAT_ADC	0x1D[5:0] 0x1E[7:0]	—	—	—	0x16[4]
VSYS_ADC	0x1F[5:0] 0x20[7:0]	—	—	—	0x16[3]
TS_ADC	0x21[1:0] 0x22[7:0]	—	—	—	0x16[2]
TDIE_ADC	0x23[0] 0x24[7:0]	—	—	—	0x16[0]
REG_RST	—	—	—	—	0x25[7]

REGISTER MAPS (continued)

Bit Types:

R: Read only

R/W: Read/Write

RC: Read clears the bit

R/WC: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.

REG0x00: Battery Voltage Regulation Limit Register [Reset = 0xA0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VREG[7:0]	10100000	R/W	00000000 = 6.8V 00000001 = 6.81V 00000010 = 6.82V …… 10100000 = 8.4V (default) …… 10111110 = 8.7V …… 11001000 = 8.8V …… 11101110 = 9.18V 11101111 = 9.19V 11110000 = 9.2V Note: V_{REG} setting range is 6.8V to 9.2V. Setting V_{REG} > 9.2V will be ignored.	REG_RST or Watchdog

REG0x01: Charge Current Limit Register [Reset = 0x54]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_HIZ	0	R/W	0 = Disable HIZ mode (default) 1 = Enable HIZ mode	REG_RST or Watchdog
D[6]	EN_ILIM	1	R/W	0 = Disable ILIM pin function 1 = Enable ILIM pin function (default)	REG_RST or Watchdog
D[5:0]	ICHG[5:0]	010100	R/W	000010 = 100mA 000011 = 150mA 000100 = 200mA …… 010100 = 1000mA (default) …… 101010 = 2100mA 101011 = 2150mA 101100 = 2200mA Note: I_{CHG} setting range is 100mA to 2200mA. Setting I_{CHG} > 2.2A or I_{CHG} < 100mA will be ignored.	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x02: Input Voltage Limit Register [Reset = 0x85]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_VINDPM_RST	1	R/W	Enable VINDPM Reset to Default upon Adapter Plug-in 0 = Disable VINDPM reset when adapter is plugged in 1 = Enable VINDPM reset when adapter is plugged in (VINDPM resets to default 4.4V) (default)	REG_RST or Watchdog
D[6]	EN_BAT_DISCHG	0	R/W	Enable BAT Pin Discharge Load (I_{BAT_DISCHG}) 0 = Disable BAT discharge load (default) 1 = Enable BAT discharge load	REG_RST or Watchdog
D[5]	PFM_OOA_DIS	0	R/W	PFM Out-of-Audio (OOA) Mode Disable 0 = Out-of-audio mode enabled while converter is in PFM (default) 1 = Out-of-audio mode disabled while converter is in PFM	REG_RST
D[4:0]	VINDPM[4:0]	00101	R/W	VINDPM Threshold Setting Bits 00000 = 3.9V 00001 = 4.0V 00010 = 4.1V …… 00101 = 4.4V (default) …… 01110 = 5.3V 01111 = 5.4V 10000 = 5.5V Note: V_{INDPM} setting range is 3.9V to 5.5V. Setting V_{INDPM} > 5.5V will be ignored.	REG_RST

REG0x03: Input Current Limit Register [Reset = 0x39]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FORCE_ICO	0	R/W	Force Start Input Current Optimizer (ICO) 0 = Do not force ICO (default) 1 = Force ICO start Note: The bit can only be set and automatically returns 0 after ICO starts. The bit only valid when EN_ICO = 1.	REG_RST or Watchdog
D[6]	FORCE_INDET	0	R/W	Force D+/D- Detection 0 = Not in D+/D- detection (default) 1 = Force D+/D- detection	REG_RST or Watchdog
D[5]	EN_ICO	1	R/W	Input Current Optimization (ICO) Algorithm Control 0 = Disable ICO 1 = Enable ICO (default)	REG_RST
D[4:0]	IINDPM[4:0]	11001	R/W	IINDPM Threshold Setting Bits 00000 = 500mA 00001 = 600mA 00010 = 700mA …… 11001 = 3000mA (default) 11010 = 3100mA 11011 = 3200mA 11100 = 3300mA Note: I_{INDPM} setting range is 0.5A to 3.3A. Setting I_{INDPM} > 3.3A will be ignored.	REG_RST

REGISTER MAPS (continued)

REG0x04: Pre-Charge and Termination Current Limit Register [Reset = 0x22]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	IPRECHG[3:0]	0010	R/W	Pre-Charge Current Limit 0000 = 50mA 0001 = 100mA 0010 = 150mA (default) …… 1101 = 700mA 1110 = 750mA 1111 = 800mA	REG_RST or Watchdog
D[3:0]	ITERM[3:0]	0010	R/W	Termination Current Limit 0000 = 50mA 0001 = 100mA 0010 = 150mA (default) …… 1101 = 700mA 1110 = 750mA 1111 = 800mA	REG_RST or Watchdog

REG0x05: Charger Control 1 Register [Reset = 0x9D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_TERM	1	R/W	Charging Termination Enable 0 = Disable termination 1 = Enable termination (default)	REG_RST or Watchdog
D[6]	Reserved	0	R/W	Reserved.	N/A
D[5:4]	WATCHDOG[1:0]	01	R/W	I²C Watchdog Timer Setting 00 = Disable watchdog timer 01 = 40s (default) 10 = 80s 11 = 160s Note: Writing a different value will reset the internal counter.	REG_RST or Watchdog
D[3]	EN_TIMER	1	R/W	Charge Safety Timer Enable 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[2:1]	CHG_TIMER[1:0]	10	R/W	Fast Charge Timer Setting 00 = 7.5h 01 = 12h 10 = 16.5h (default) 11 = 21h Note: Writing a different value will reset the internal counter.	REG_RST or Watchdog
D[0]	TMR2X_EN	1	R/W	Enable Half Clock Rate Safety Timer 0 = Disable 1 = Safety timer slow down (by a factor of 2) during DPM or thermal regulation (default)	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x06: Charger Control 2 Register [Reset = 0x7D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_OTG	0	R/W	Buck (OTG) Mode Control 0 = Disable OTG (default) 1 = Enable OTG Note: EN_CHG has higher priority than EN_OTG if they are set at the same time.	REG_RST or Watchdog
D[6]	AUTO_INDET_EN	1	R/W	Automatic Input Source Detection Enable 0 = Disable D+/D- detection when VBUS plugs in 1 = Enable D+/D- detection when VBUS plugs in (default)	REG_RST or Watchdog
D[5:4]	TREG[1:0]	11	R/W	Thermal Regulation Threshold 00 = +60℃ 01 = +80℃ 10 = +100℃ 11 = +120℃ (default)	REG_RST or Watchdog
D[3]	EN_CHG	1	R/W	Charger Enable Configuration 0 = Charge disable 1 = Charge enable (default) Note: EN_CHG has higher priority than EN_OTG if they are set at the same time.	REG_RST or Watchdog
D[2]	BATLOW	1	R/W	Battery Pre-Charge to Fast Charge Threshold 0 = 5.6V 1 = 6.0V (default)	REG_RST or Watchdog
D[1:0]	VRECHG[1:0]	01	R/W	Battery Recharge Threshold Setting 00 = 100mV 01 = 200mV (default) 10 = 300mV 11 = 400mV	REG_RST

REG0x07: Charger Control 3 Register [Reset = 0x0A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PFM_DIS	0	R/W	Enable PFM Mode 0 = Enable PFM operation (default) 1 = Disable PFM operation	REG_RST
D[6]	WD_RST	0	R/W	I²C Watchdog Timer Reset 0 = Normal (default) 1 = Reset (bit goes back to 0 after timer reset)	REG_RST or Watchdog
D[5:4]	TOPOFF_TIMER[1:0]	00	R/W	Top-Off Timer 00 = Disabled (default) 01 = 15min 10 = 30min 11 = 45min	REG_RST or Watchdog
D[3:0]	SYS_MIN[3:0]	1010	R/W	Minimum System Voltage Limit 0000 = 6.0V 0001 = 6.1V 0010 = 6.2V …… 1010 = 7.0V (default) …… 1101 = 7.3V 1110 = 7.4V 1111 = 7.5V	REG_RST

REGISTER MAPS (continued)

REG0x08: Charger Control 4 Register [Reset = 0x0D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	BHOT[1:0]	00	R/W	TS Hot Temperature Threshold in OTG Mode 00 = V_{BHOT1} threshold (34.45%) (default) 01 = V_{BHOT0} threshold (37.75%) 10 = V_{BHOT2} threshold (31.35%) 11 = Disable OTG mode thermal protection	REG_RST or Watchdog
D[5]	BCOLD	0	R/W	TS Cold Temperature Threshold in OTG Mode 0 = V_{BCOLD0} threshold (77%) (default) 1 = V_{BCOLD1} threshold (80%)	REG_RST or Watchdog
D[4:3]	JEITA_VSET[1:0] (45℃ - 60℃)	01	R/W	JEITA High Temperature Voltage Setting 00 = Charge suspend 01 = Set V_{REG} to 8V (default) 10 = Set V_{REG} to 8.3V 11 = V_{REG} unchanged	REG_RST or Watchdog
D[2]	JEITA_ISETH (45℃ - 60℃)	1	R/W	JEITA High Temperature Current Setting 0 = 40% of I_{CHG} 1 = 100% of I_{CHG} (default)	REG_RST or Watchdog
D[1:0]	JEITA_ISETC[1:0] (0℃ - 10℃)	01	R/W	JEITA Low Temperature Current Setting 00 = Charge suspend 01 = 20% of I_{CHG} (default) 10 = 40% of I_{CHG} 11 = 100% of I_{CHG}	REG_RST or Watchdog

REG0x09: OTG Control Register [Reset = 0xF6]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	OTG_ILIM[3:0]	1111	R/W	Buck (OTG) Mode Current Limit 0000 = 0.5A 0001 = 0.6A 0010 = 0.7A …… 1101 = 1.8A 1110 = 1.9A 1111 = 2.0A (default)	REG_RST or Watchdog
D[3:0]	OTG_VLIM[3:0]	0110	R/W	Buck (OTG) Mode Regulation Voltage 0000 = 4.5V 0001 = 4.6V 0010 = 4.7V …… 0110 = 5.1V (default) 0111 = 5.2V 1000 = 5.3V 1001 = 5.4V 1010 = 5.5V Note: OTG_VLIM[3:0] setting range is 4.5V to 5.5V. Setting OTG_VLIM[3:0] > 5.5V will be ignored.	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x0A: ICO Current Limit Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved.	N/A
D[4:0]	ICO_ILIM[4:0]	xxxxx	R	Actual Input Current Limit 00000 = 500mA 00001 = 600mA 00010 = 700mA …… 11010 = 3100mA 11011 = 3200mA 11100 = 3300mA Note: The maximum input current limit is 3300mA.	N/A

REG0x0B: Charger Status 1 Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_DONE_STAT	x	R	ADC Conversion Status (in One-Shot Mode Only) 0 = Conversion not complete 1 = Conversion complete Note: Always reads 0 in continuous mode.	N/A
D[6]	IINDPM_STAT	x	R	Input Current Regulation (Dynamic Power Management) 0 = Not in IINDPM regulation 1 = In IINDPM regulation (ILIM pin or IINDPM[4:0] register)	N/A
D[5]	VINDPM_STAT	x	R	Input Voltage Regulation (Dynamic Power Management) 0 = Not in VINDPM regulation 1 = In VINDPM regulation	N/A
D[4]	TREG_STAT	x	R	IC Thermal Regulation Status 0 = Normal 1 = In thermal regulation	N/A
D[3]	WD_STAT	x	R	I²C Watchdog Timer Status Bit 0 = Normal 1 = Watchdog timer expired	N/A
D[2:0]	CHRG_STAT[2:0]	xxx	R	Charge Status Bits 000 = Not charging 001 = Trickle charge (V_{BAT} < V_{BAT_SHORT}) 010 = Pre-charge (V_{BAT_SHORT} < V_{BAT} < V_{BAT_LOW}) 011 = Fast charge (CC mode) 100 = Taper charge (CV mode) 101 = Top-off timer active charging 110 = Charge termination done 111 = Reserved	N/A

REGISTER MAPS (continued)

REG0x0C: Charger Status 2 Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PG_STAT	x	R	Input Power Status (VBUS in Good Voltage Range and Not Poor) 0 = Input power source is not good 1 = Input power source is good	N/A
D[6:4]	VBUS_STAT[2:0]	xxx	R	VBUS Status Register 000 = No input 001 = USB host SDP (500mA) 010 = USB CDP (1.5A) 011 = USB DCP (3.0A) 100 = POORSRC detected 7 consecutive times 101 = Unknown adapter (500mA/1000mA) 110 = Non-standard adapter (1A/2A/2.1A/2.4A) 111 = OTG	N/A
D[3]	Reserved	0	R	Reserved.	N/A
D[2:1]	ICO_STAT[1:0]	xx	R	Input Current Optimizer (ICO) Status 00 = ICO disabled 01 = ICO optimization is in progress 10 = Maximum input current detected 11 = Reserved	N/A
D[0]	VSYS_STAT	x	R	System Voltage Regulation Status 0 = Not in SYS_MIN regulation (V_{BAT} > V_{SYS_MIN}) 1 = In SYS_MIN regulation (V_{BAT} < V_{SYS_MIN})	N/A

REG0x0D: NTC Status Register [Reset = 0x0X]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	00000	R	Reserved.	N/A
D[2:0]	TS_STAT[2:0]	xxx	R	NTC (TS) Status 000 = Normal 010 = TS warm 011 = TS cool 101 = TS cold 110 = TS hot	N/A

REG0x0E: FAULT Status Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_OVP_STAT	x	R	Input Over-Voltage Status 0 = Normal 1 = Device in over-voltage protection	N/A
D[6]	TSHUT_STAT	x	R	Temperature Shutdown Status 0 = Normal 1 = Device in thermal shutdown protection	N/A
D[5]	BATOVP_STAT	x	R	Battery Over-Voltage Status 0 = Normal 1 = BATOVP (V_{BAT} > V_{BATOVP})	N/A
D[4]	TMR_STAT	x	R	Charge Safety Timer Status 0 = Normal 1 = Charge safety timer expired	N/A
D[3:0]	Reserved	0000	R	Reserved.	N/A

REGISTER MAPS (continued)

REG0x0F: Charger Flag 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_DONE_FLAG	0	RC	One-Shot Mode ADC Conversion Flag 0 = Conversion not complete (default) 1 = Conversion complete Note: Always reads 0 in continuous mode.	REG_RST
D[6]	IINDPM_FLAG	0	RC	IINDPM Regulation INT Flag 0 = Normal (default) 1 = IINDPM signal rising edge detected	REG_RST
D[5]	VINDPM_FLAG	0	RC	VINDPM Regulation INT Flag 0 = Normal (default) 1 = VINDPM signal rising edge detected	REG_RST
D[4]	TREG_FLAG	0	RC	IC Temperature Regulation INT Flag 0 = Normal (default) 1 = TREG signal rising edge detected	REG_RST
D[3]	WD_FLAG	0	RC	I²C Watchdog INT Flag 0 = Normal (default) 1 = WD_STAT signal rising edge detected	REG_RST
D[2:1]	Reserved	00	R	Reserved.	N/A
D[0]	CHRG_FLAG	0	RC	Charge Status INT Flag 0 = Normal (default) 1 = CHRG_STAT[2:0] bits changed	REG_RST

REG0x10: Charger Flag 2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PG_FLAG	0	RC	Power Good INT Flag 0 = Normal (default) 1 = PG signal toggle detected	REG_RST
D[6:5]	Reserved	00	R	Reserved.	N/A
D[4]	VBUS_FLAG	0	RC	VBUS Status INT Flag 0 = Normal (default) 1 = VBUS_STAT[2:0] bits changed	REG_RST
D[3]	Reserved	0	R	Reserved.	N/A
D[2]	TS_FLAG	0	RC	TS Status INT Flag 0 = Normal (default) 1 = TS_STAT[2:0] bits changed	REG_RST
D[1]	ICO_FLAG	0	RC	Input Current Optimizer (ICO) INT Flag 0 = Normal (default) 1 = ICO_STAT[1:0] changed	REG_RST
D[0]	VSYS_FLAG	0	RC	System Voltage Regulation INT Flag 0 = Normal (default) 1 = Entered or exited SYS_MIN regulation	REG_RST

REGISTER MAPS (continued)

REG0x11: FAULT Flag Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_OVP_FLAG	0	RC	Input Over-Voltage INT Flag 0 = Normal (default) 1 = Entered VBUS_OVP fault	REG_RST
D[6]	TSHUT_FLAG	0	RC	IC Temperature Shutdown INT Flag 0 = Normal (default) 1 = Entered TSHUT fault	REG_RST
D[5]	BATOVP_FLAG	0	RC	Battery Over-Voltage INT Flag 0 = Normal (default) 1 = Entered BATOVP fault	REG_RST
D[4]	TMR_FLAG	0	RC	Charge Safety Timer Fault INT Flag 0 = Normal (default) 1 = Charge safety timer expired rising edge detected	REG_RST
D[3]	SYS_SHORT_FLAG	0	RC	System Short INT Flag 0 = Normal (default) 1 = Stopped switching due to Boost converter overload	REG_RST
D[2:1]	Reserved	00	R	Reserved.	N/A
D[0]	OTG_FLAG	0	RC	OTG Buck Mode Fault INT Flag 0 = Normal (default) 1 = VBUS overloaded in OTG, or VBUS OVP, or battery below V_{OTG_BAT}	REG_RST

REG0x12: Charger Mask 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_DONE_MASK	0	R/W	ADC Conversion INT Mask Flag 0 = ADC_DONE produce INT pulse (default) 1 = ADC_DONE does not produce INT pulse Note: Only one-shot mode.	REG_RST
D[6]	IINDPM_MASK	0	R/W	IINDPM Regulation INT Mask 0 = IINDPM entry produces INT pulse (default) 1 = IINDPM entry does not produce INT pulse	REG_RST
D[5]	VINDPM_MASK	0	R/W	VINDPM Regulation INT Mask 0 = VINDPM entry produces INT pulse (default) 1 = VINDPM entry does not produce INT pulse	REG_RST
D[4]	TREG_MASK	0	R/W	IC Temperature Regulation INT Mask 0 = TREG entry produces INT pulse (default) 1 = TREG entry does not produce INT pulse	REG_RST
D[3]	WD_MASK	0	R/W	I²C Watchdog Timer INT Mask 0 = WD_STAT bit rising edge produces INT pulse (default) 1 = WD_STAT bit rising edge does not produce INT pulse	REG_RST
D[2:1]	Reserved	00	R/W	Reserved.	N/A
D[0]	CHRG_MASK	0	R/W	Charge Status INT Mask 0 = CHRG_STAT[2:0] bits change produces INT pulse (default) 1 = CHRG_STAT[2:0] bits change does not produce INT pulse	REG_RST

REGISTER MAPS (continued)

REG0x13: Charger Mask 2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PG_MASK	0	R/W	Power Good INT Mask 0 = PG toggle produces INT pulse (default) 1 = PG toggle does not produce INT pulse	REG_RST
D[6:5]	Reserved	00	R/W	Reserved.	N/A
D[4]	VBUS_MASK	0	R/W	VBUS Status INT Mask 0 = VBUS_STAT[2:0] bits change produces INT pulse (default) 1 = VBUS_STAT[2:0] bits change does not produce INT pulse	REG_RST
D[3]	Reserved	0	R/W	Reserved.	N/A
D[2]	TS_MASK	0	R/W	TS Status INT Mask 0 = TS_STAT[2:0] bits change produces INT pulse (default) 1 = TS_STAT[2:0] bits change does not produce INT pulse	REG_RST
D[1]	ICO_MASK	0	R/W	Input Current Optimizer (ICO) INT Mask 0 = ICO_STAT rising edge produces INT pulse (default) 1 = ICO_STAT rising edge does not produce INT pulse	REG_RST
D[0]	VSYS_MASK	0	R/W	System Voltage Regulation INT Mask 0 = Entering or exiting SYS_MIN produces INT pulse (default) 1 = Entering or exiting SYS_MIN does not produce INT pulse	REG_RST

REG0x14: Fault Mask Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_OVP_MASK	0	R/W	Input Over-Voltage INT Mask 0 = VBUS_OVP rising edge produces INT pulse (default) 1 = VBUS_OVP rising edge does not produce INT pulse	REG_RST
D[6]	TSHUT_MASK	0	R/W	Thermal Shutdown INT Mask 0 = TSHUT rising edge produces INT pulse (default) 1 = TSHUT rising edge does not produce INT pulse	REG_RST
D[5]	BATOVP_MASK	0	R/W	Battery Over-Voltage INT Mask 0 = BATOVP rising edge produces INT pulse (default) 1 = BATOVP rising edge does not produce INT pulse	REG_RST
D[4]	TMR_MASK	0	R/W	Charge Safety Timer Fault INT Mask 0 = Timer expired rising edge produces INT pulse (default) 1 = Timer expired rising edge does not produce INT pulse	REG_RST
D[3]	SYS_SHORT_MASK	0	R/W	System Short Fault INT Mask 0 = System short rising edge produces INT pulse (default) 1 = System short rising edge does not produce INT pulse	REG_RST
D[2:1]	Reserved	00	R/W	Reserved.	N/A
D[0]	OTG_MASK	0	R/W	OTG Buck Mode Fault INT Mask 0 = OTG Buck mode fault event produces INT pulse (default) 1 = OTG Buck mode fault event does not produce INT pulse	REG_RST

REGISTER MAPS (continued)

REG0x15: ADC Control Register [Reset = 0x30]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_EN	0	R/W	ADC Control 0 = Disable ADC (default) 1 = Enable ADC	REG_RST or Watchdog
D[6]	ADC_RATE	0	R/W	0 = Continuous conversion (default) 1 = One-shot conversion	REG_RST
D[5:4]	ADC_SAMPLE[1:0]	11	R/W	Sample Speed of ADC 00 = 15-bit effective resolution 01 = 14-bit effective resolution 10 = 13-bit effective resolution 11 = 12-bit effective resolution (default)	REG_RST
D[3:0]	Reserved	0000	R/W	Reserved.	N/A

REG0x16: ADC Function Disable Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_ADC_DIS	0	R/W	0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[6]	ICHG_ADC_DIS	0	R/W	0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[5]	VBUS_ADC_DIS	0	R/W	0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[4]	VBAT_ADC_DIS	0	R/W	0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[3]	VSYS_ADC_DIS	0	R/W	0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[2]	TS_ADC_DIS	0	R/W	0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[1]	Reserved	0	R/W	Reserved.	N/A
D[0]	TDIE_ADC_DIS	0	R/W	0 = Enable conversion (default) 1 = Disable conversion	REG_RST

REG0x17: IBUS ADC 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_POL	0	R	Polarity of IBUS 0 = Positive (positive means flow into VBUS pin) (default) 1 = Negative (negative means flow out of VBUS pin)	REG_RST
D[6:4]	Reserved	000	R	Reserved	N/A
D[3:0]	IBUS_ADC[11:8]	0000	R	Higher 4 Bits of the 12-Bit ADC IBUS Data (1mA Resolution) MSB<3:0>: 2048mA, 1024mA, 512mA, 256mA Note: IBUS reading range: 0A - 4A.	REG_RST

REGISTER MAPS (continued)

REG0x18: IBUS ADC 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUS_ADC[7:0]	00000000	R	Lower Bits of the 12-Bit ADC IBUS Data (1mA Resolution) LSB<7:0>: 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA Note: IBUS reading range: 0A - 4A.	REG_RST

REG0x19: ICHG ADC 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved.	N/A
D[3:0]	ICHG_ADC[11:8]	0000	R	Higher 4 Bits of the 12-Bit ADC ICHG Data (1mA Resolution) MSB<3:0>: 2048mA, 1024mA, 512mA, 256mA Note: ICHG reading range: 0A - 4A.	REG_RST

REG0x1A: ICHG ADC 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	ICHG_ADC[7:0]	00000000	R	Lower Bits of the 12-Bit ADC ICHG Data (1mA Resolution) LSB<7:0>: 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA Note: ICHG reading range: 0A - 4A.	REG_RST

REG0x1B: VBUS ADC 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved.	N/A
D[4:0]	VBUS_ADC[12:8]	00000	R	Higher 5 Bits of the 13-Bit ADC VBUS Data (1mV Resolution) MSB<4:0>: 4096mV, 2048mV, 1024mV, 512mV, 256mV Note: VBUS reading range: 0V - 6.5V. And ADC_EN bit is cleared when V_{VBUS}>V_{VBUS_OV}.	REG_RST

REG0x1C: VBUS ADC 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUS_ADC[7:0]	00000000	R	Lower Bits of the 13-Bit ADC VBUS Data (1mV Resolution) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV Note: VBUS reading range: 0V - 6.5V. And ADC_EN bit is cleared when V_{VBUS}>V_{VBUS_OV}.	REG_RST

REGISTER MAPS (continued)

REG0x1D: VBAT ADC 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved.	N/A
D[5:0]	VBAT_ADC[13:8]	000000	R	Higher 6 Bits of the 14-Bit ADC VBAT Data (1mV Resolution) MSB<5:0>: 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV Note: VBAT reading range: 0V - 10V.	REG_RST

REG0x1E: VBAT ADC 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT_ADC[7:0]	00000000	R	Lower Bits of the 14-Bit ADC VBAT Data (1mV Resolution) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV Note: VBAT reading range: 0V - 10V.	REG_RST

REG0x1F: VSYS ADC 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved.	N/A
D[5:0]	VSYS_ADC[13:8]	000000	R	Higher 6 Bits of the 14-Bit ADC VSYS Data (1mV Resolution) MSB<5:0>: 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV Note: VSYS reading range: 0V - 10V.	REG_RST

REG0x20: VSYS ADC 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VSYS_ADC[7:0]	00000000	R	Lower Bits of the 14-Bit ADC VSYS Data (1mV Resolution) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV Note: VSYS reading range: 0V - 10V.	REG_RST

REGISTER MAPS (continued)

REG0x21: TS ADC 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	000000	R	Reserved.	N/A
D[1:0]	TS_ADC[9:8]	00	R	Higher 2 Bits of the 10-Bit ADC TS Data (0.098% Resolution) MSB<1:0>: 50%, 25% Note: TS as percentage of REGN valid reading range: 10% - 90%. Accuracy is not guaranteed beyond this range.	REG_RST

REG0x22: TS ADC 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TS_ADC[7:0]	00000000	R	Lower Bits of the 10-Bit ADC TS Data (0.098% Resolution) LSB<7:0>: 12.5%, 6.25%, 3.125%, 1.563%, 0.781%, 0.391%, 0.195%, 0.098% Note: TS as percentage of REGN valid reading range: 10% - 90%. Accuracy is not guaranteed beyond this range.	REG_RST

REG0x23: TDIE ADC 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	Reserved	0000000	R	Reserved.	N/A
D[0]	TDIE_ADC[8]	0	R	Higher 1 Bit of the 9-Bit ADC TDIE Data (0.5℃ Resolution) MSB<0>: 128℃ Note: TDIE (IC Temperature) reading range: 0℃ - 128℃.	REG_RST

REG0x24: TDIE ADC 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIE_ADC[7:0]	00000000	R	Lower Bits of the 9-Bit ADC TDIE Data (0.5℃ Resolution) LSB<7:0>: 64℃, 32℃, 16℃, 8℃, 4℃, 2℃, 1℃, 0.5℃ Note: TDIE (IC Temperature) reading range: 0℃ - 128℃.	REG_RST

REG0x25: Part Information Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/WC	Register Reset 0 = No effect (keep current register settings) (default) 1 = Reset R/W bits of all registers to the default and reset safety timer (It also resets itself to 0 after register reset is completed)	REG_RST
D[6:3]	PN[3:0]	0000	R	Part ID 0000 = SGM41528	N/A
D[2:0]	DEV_REV[2:0]	000	R	Revision: 000	N/A

APPLICATION INFORMATION

The SGM41528 is typically used as a charger with power path management in smart phones, tablets and other portable devices. In the design, it comes along with a host controller (a processor with I²C interface) and a 2-cell Li-Ion or Li-polymer battery.

Detailed Design Procedure

Inductor Selection

The inductor selection mainly considers the inductance, the saturation current and heat rating current. The saturation current and heat rating current are better to higher than the possible maximum current considering the inductor current ripple as following formula:

$$I_{SAT} > I_{IN} + \frac{\Delta I}{2} \quad (5)$$

The inductor ripple current (ΔI) depends on input voltage (V_{VBUS}), output voltage (V_{SYS}), inductor (L) and switching frequency (f_{SW}):

$$\Delta I = \frac{V_{VBUS} \times (V_{SYS} - V_{VBUS})}{V_{SYS} \times f_{SW} \times L} \quad (6)$$

An inductor with a larger value results in less ripple current and a lower peak inductor current, reducing stress on the power MOSFET. However, the larger value inductor has a larger physical size, a higher series resistance, and a lower saturation current. To trade off between the inductor power loss and size, it is recommended to choose the inductor ripple current to be approximated 20% - 40% of the maximum input current.

VBUS and PMID Capacitor

The effective capacitance of VBUS and PMID should be enough to absorb the VBUS input switching ripple current. The equation below shows the input capacitor RMS current I_{CIN} calculation.

$$I_{CIN} = \frac{\Delta I}{2 \times \sqrt{3}} \approx 0.29 \times \Delta I \quad (7)$$

Low ESR ceramic capacitors are recommended for input capacitor. The input capacitor voltage ripple can be calculated as follow:

$$\Delta V_{IN} = \frac{V_{IN}}{8 \times f_{SW}^{\ 2} \times L \times C_{IN}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (8)$$

VSYS Capacitor

The VSYS output current of the Boost converter is discontinuous and therefore requires an output capacitor (C_{SYS}) to supply AC current to the load. Ripple current rating of VSYS output capacitor should be higher than the maximum output ripple. The output capacitor RMS current can be calculated by below equation and the maximum value occurs at 50% duty cycle.

$$I_{COUT} = I_{IN} \times \sqrt{D \times (1 - D)} \quad (9)$$

For the best performance, low ESR ceramic capacitors are recommended. The output voltage ripple can be estimated as follow:

$$\Delta V_{SYS} = \frac{I_{OUT} \times D}{f_{SW} \times C_{SYS}} \quad (10)$$

Layout Guidelines

The switching node (SW) creates very high frequency noises, which are several times higher than f_{SW} (1.5MHz) due to sharp rise and fall of the voltage and current in the switches. To reduce the ringing issues and noise generation, it is important to design a proper layout for minimizing the current path impedance and loop area. The following considerations can help to make a better layout.

1. Place all the output capacitors as close as possible to SYS and BAT pins. The capacitors ground pins need to be connected to the IC ground with GND plane or short copper trace connections.

2. Place the input capacitor between PMID and GND pins as close as possible to the chip with shortest copper connections (avoid vias). Choose the smallest capacitor size.

3. Connect one pin of the inductor as close as possible to the SW pin of the device and minimize the copper area connected to the SW node to reduce capacitive coupling from SW area to nearby signal traces. This decreases the noise induced through parasitic stray capacitances and displacement currents to other conductors. SW connection should be wide enough to carry the charging current. Keep other signals and traces away from SW if possible.

APPLICATION INFORMATION (continued)

4. Place output capacitor GND pin as close as possible to the GND pin of the device and the GND pin of input capacitor C_{IN}. It is better to avoid using vias for these connections and keep the high frequency current paths short enough and on the same layer. A GND copper layer under the component layer helps to reduce noise emissions. Pay attention to the DC current and AC current paths in the layout and keep them short and decoupled as much as possible.

5. For analog signals, it is better to use a separate analog ground (AGND) branched only at one point from GND pin. To avoid high current flow through the AGND path, it should be connected to GND only at one point (preferably the GND pin).

6. Place decoupling capacitors close to the IC pins with the shortest copper connections.

7. Solder the exposed thermal pad of the package to the PCB ground planes. Ensure that there are enough thermal vias directly under the IC, connecting to the ground plane on the other layers for better heat dissipation and cooling of the device.

8. Select proper sizes for the vias and ensure enough copper is available to carry the current for a given current path. Vias usually have some considerable parasitic inductance and resistance.

9. Route the feedback signal BATP and BATN away from SW node.

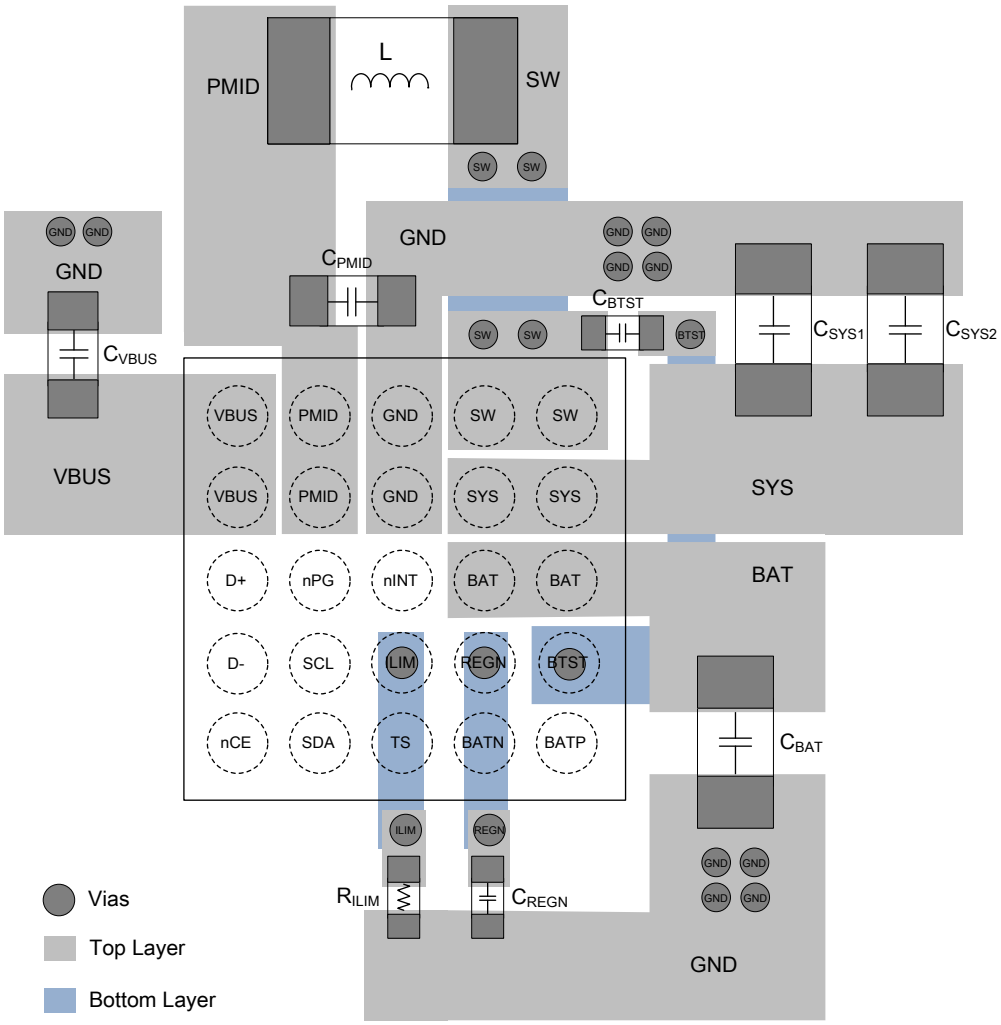


Figure 22. Layout Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

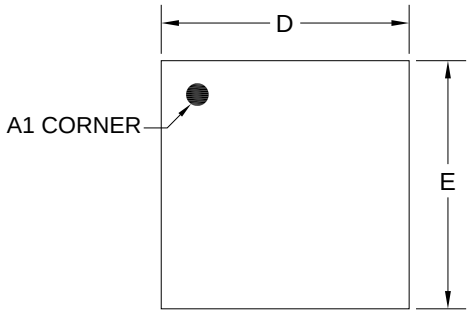
SEPTEMBER 2022 – REV.A.1 to REV.A.2	Page
Updated Typical Application Circuit section	18
Updated Detailed Description section	26

JUNE 2022 – REV.A to REV.A.1	Page
Updated Detailed Description section	26

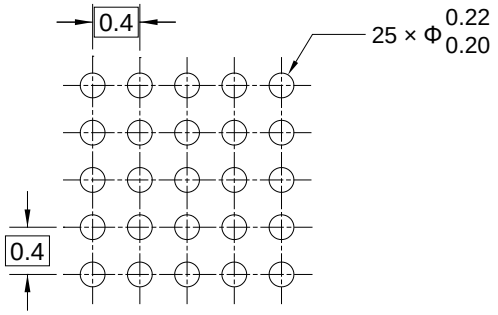
Changes from Original (MAY 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

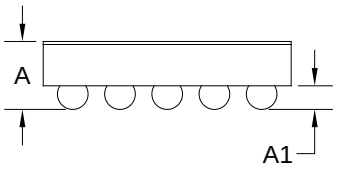
WLCSP-2.1×2.1-25B



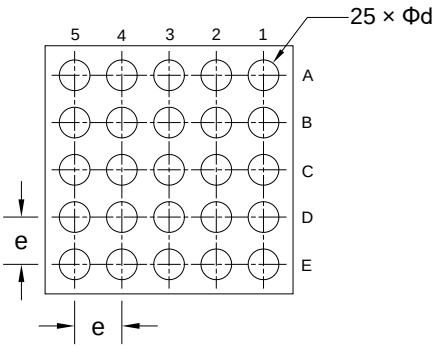
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



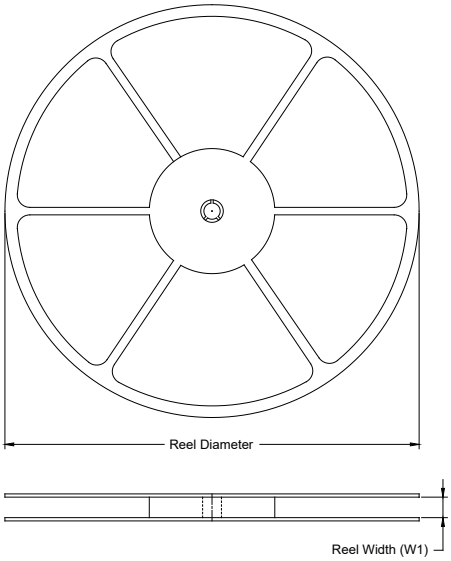
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.525	0.575	0.625
A1	0.180	0.200	0.220
D	2.070	2.100	2.130
E	2.070	2.100	2.130
d	0.230	0.260	0.290
e	0.400 BSC		

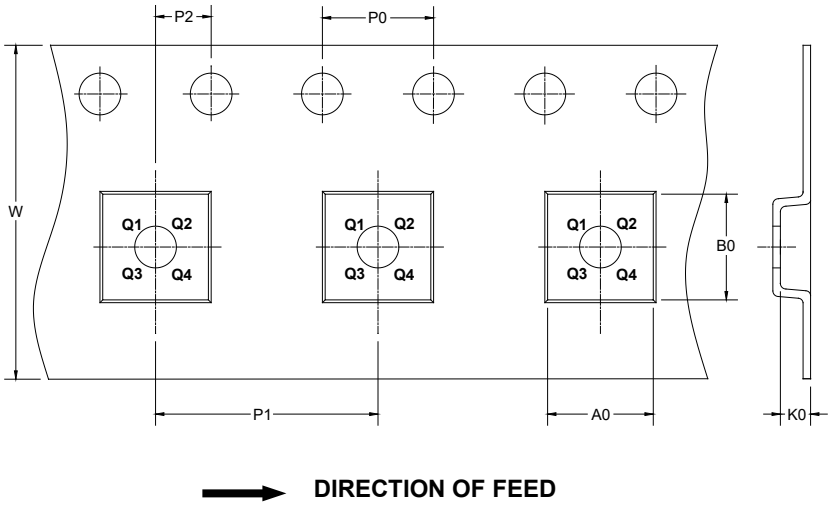
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

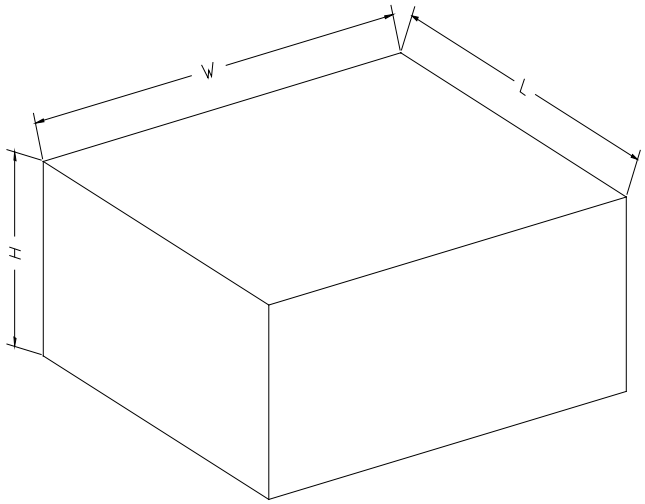
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.1×2.1-25B	7″	9.0	2.24	2.24	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002