



# PCA9614

## 2-channel multipoint Fast-mode Plus differential I<sup>2</sup>C-bus buffer

Rev. 2 — 21 September 2021

Product data sheet

### 1 General description

The PCA9614 is a Fast-mode Plus (Fm+) SMBus/I<sup>2</sup>C-bus buffer that extends the normal single-ended SMBus/I<sup>2</sup>C-bus through electrically noisy environments using a differential SMBus/I<sup>2</sup>C-bus (dI<sup>2</sup>C) physical layer, which is transparent to the SMBus/I<sup>2</sup>C-bus protocol layer. It consists of two single-ended to differential driver channels for the SCL (serial clock), SDA (serial data).

The use of differential transmission lines between identical dI<sup>2</sup>C bus buffers removes electrical noise and common-mode offsets that are present when signal lines must pass between different voltage domains, are bundled with hostile signals, or run adjacent to electrical noise sources, such as high energy power supplies and electric motors.

The SMBus/I<sup>2</sup>C-bus was conceived as a simple slow speed digital link for short runs, typically on a single PCB or between adjacent PCBs with a common ground connection. Applications that extend the bus length or run long cables require careful design to preserve noise margin and reject interference.

The dI<sup>2</sup>C-bus buffers were designed to solve these problems and are ideally suited for rugged high noise environments and/or longer cable applications, allow multiple targets, and operate at bus speeds up to 1 MHz clock rate. Cables can be extended to at least three meters (3 m), or longer cable runs at lower clock speeds. The dI<sup>2</sup>C-bus buffers are compatible with existing SMBus/I<sup>2</sup>C-bus devices and can drive Standard, Fast-mode, and Fast-mode Plus devices on the single-ended side.

Signal direction is automatic and requires no external control. To prevent bus latch-up the I<sup>2</sup>C-bus side employs static level offset. Take care when connecting the PCA9614 to other SMBus/I<sup>2</sup>C-bus buffers that do not operate with other static level offset bus buffers.

These devices are a bridge between the normal 2-wire single-ended wired-OR SMBus/I<sup>2</sup>C-bus and the 4-wire dI<sup>2</sup>C-bus.

The PCA9614 has two supply voltages,  $V_{DD(A)}$  and  $V_{DD(B)}$ .  $V_{DD(A)}$ , the card side supply, only serves as a reference and ranges from 2.3 V to 5.5 V.  $V_{DD(B)}$ , the line side supply, serves as the majority supply for circuitry, and ranges from 3.0 V to 5.5 V.



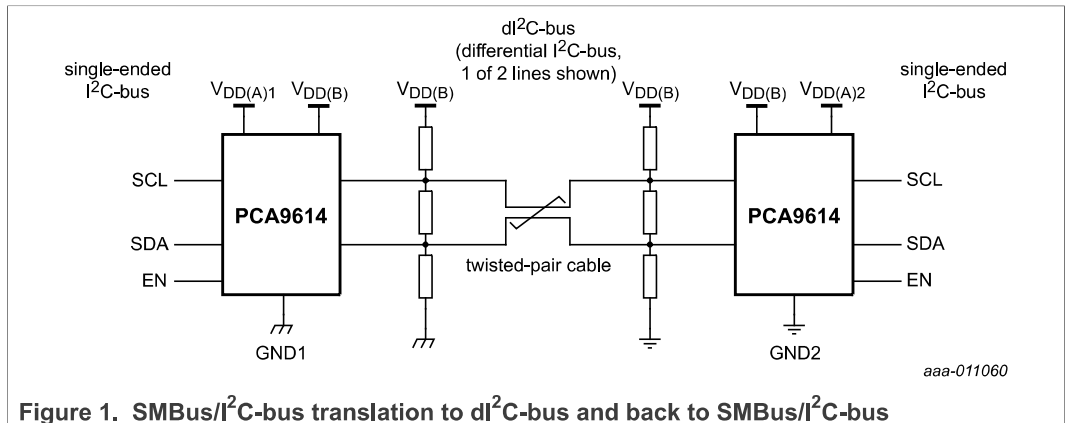


Figure 1. SMBus/I<sup>2</sup>C-bus translation to dI<sup>2</sup>C-bus and back to SMBus/I<sup>2</sup>C-bus

## 2 Features and benefits

- New dI<sup>2</sup>C-bus buffers offer improved resistance to system noise and ground offset up to 1/2 of supply voltage
- 2 channel dI<sup>2</sup>C (differential I<sup>2</sup>C) to Fm+ single-ended buffer operating up to 1 MHz with 30 mA SDA/SCL drive capability
- Compatible with I<sup>2</sup>C-bus Standard/Fast-mode and SMBus, Fast-mode Plus up to 1 MHz
- Active HIGH (internal pull-up resistor) Enable disables devices to high-impedance state
- Single-ended I<sup>2</sup>C-bus on card side up to 540 pF
- Differential I<sup>2</sup>C-bus on cable side supporting multi-drop bus
  - Maximum cable length: 3 m (approximately 10 feet) (longer at lower frequency)
  - dI<sup>2</sup>C output: 1.5 V differential output with nominal terminals
  - Differential line impedance (user defined): 100 Ω nominal suggested
  - Receive input sensitivity: ±200 mV
  - Hysteresis: ±30 mV typical
  - Input impedance: high-impedance (1 MΩ typical)
  - Receive input voltage range: -0.5 V to +5.5 V
- Lock-up free operation
- Supports arbitration and clock stretching across the dI<sup>2</sup>C-bus buffers
- Powered-off and powering-up high-impedance I<sup>2</sup>C-bus pins
- Operating supply voltage (V<sub>DD(A)</sub>) range of 2.3 V to 5.5 V with single-ended side 5.5 V tolerant
- Differential I<sup>2</sup>C-bus operating supply voltage (V<sub>DD(B)</sub>) range of 3.0 V to 5.5 V with 5.5 V tolerant. Best operation is at 5 V.
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offering: TSSOP10

### 3 Applications

- Monitor remote temperature/leak detectors in harsh environment
- Control of power supplies in high noise environment
- Transmission of I<sup>2</sup>C-bus between equipment cabinets
- Commercial lighting and industrial heating/cooling control
- Any application that requires long I<sup>2</sup>C-bus runs in electrically noisy environments
- Any application with multiple power suppliers and the potential for ground offsets up to 2.5 V

### 4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9614DP	P9614	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1

#### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method <sup>[1]</sup>	Minimum order quantity	Temperature range
PCA9614DP	PCA9614DP,118 <sup>[2]</sup>	TSSOP10	Reel 13" Q1 NDP	2500	T <sub>amb</sub> = -40 °C to +85 °C
PCA9614DP	PCA9614DPZ	TSSOP10	Reel 13" Q1 NPD SSB <sup>[3]</sup>	2500	T <sub>amb</sub> = -40 °C to +85 °C

[1] Standard packing quantities and other packaging data are available at [www.nxp.com/packages/](http://www.nxp.com/packages/)

[2] Discontinued Notice 202104010DN - PCA9614DPZ is drop in replacement in accordance with PCN 202104008A

[3] This packing method uses a Static Shielding Bag (SSB) solution. Material should be kept in the sealed bag between uses.

5 Functional diagram

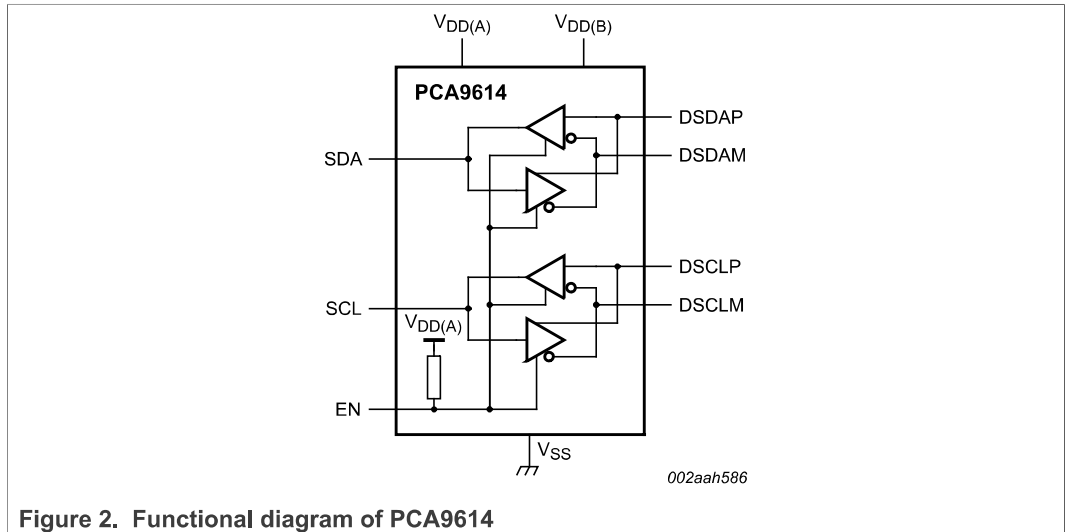


Figure 2. Functional diagram of PCA9614

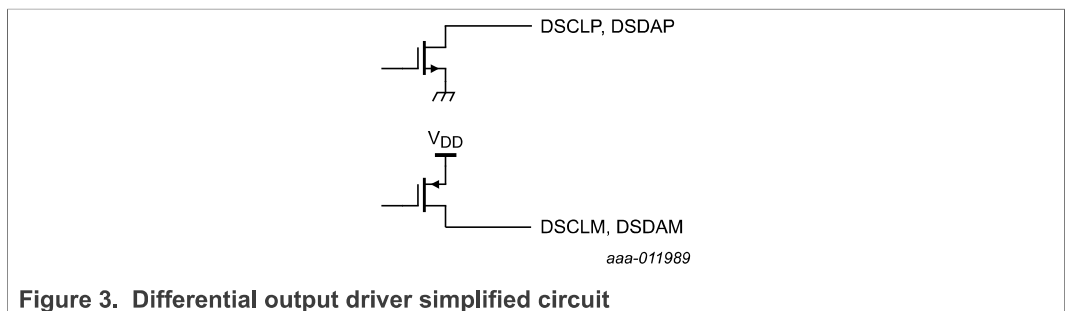


Figure 3. Differential output driver simplified circuit

## 6 Pinning information

### 6.1 Pinning

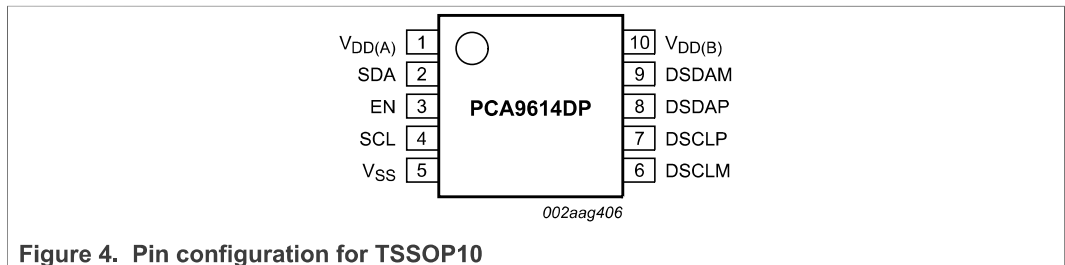


Figure 4. Pin configuration for TSSOP10

### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
V <sub>DD(A)</sub>	1	I <sup>2</sup> C-bus side power supply (2.3 V to 5.5 V)
SDA	2	card side open-drain serial data input/output
EN	3	enable input (active HIGH); internal pull-up resistor to V <sub>DD(A)</sub>
SCL	4	card side open-drain serial clock input/output
V <sub>SS</sub>	5	ground supply voltage (0 V)
DSCLM	6	line side differential open-drain clock minus input/output
DSCLP	7	line side differential open-drain clock plus input/output
DSDAP	8	line side differential open-drain data plus input/output
DSDAM	9	line side differential open-drain data minus input/output
V <sub>DD(B)</sub>	10	differential side power supply (3.0 V to 5.5 V)

## 7 Functional description

Refer to [Figure 2](#).

The PCA9614 is used at each node of the dI<sup>2</sup>C-bus signal path, to provide conversion from the dI<sup>2</sup>C-bus signal format to conventional I<sup>2</sup>C-bus/SMBus, allowing the connection of existing I<sup>2</sup>C-bus/SMBus devices as targets or the bus controller. Because the signal voltages on the I<sup>2</sup>C-bus/SMBus bus side may be different from the dI<sup>2</sup>C-bus side, there are two power supply pins and a common ground. Static offset is employed by the I<sup>2</sup>C-bus/SMBus side to prevent bus latch up. Signal direction is determined by the I<sup>2</sup>C-bus/SMBus bus protocol, and does not require a direction signal, as these bus buffers automatically set signal flow direction. An enable pin (EN) is provided to disable the bus buffer, and is useful for fault finding, power-up sequencing, or reconfiguration of a large bus system by isolating sections not needed at all times.

Construction of the differential transmission line is not device-dependent. PCB traces, open wiring, twisted-pair cables, or a combination of these may be used. Twisted-pair cables offer the best performance. A typical twisted-pair transmission line cable has a characteristic impedance of 'about 100 Ω' and must be terminated at both ends in 100 Ω to prevent unwanted signal reflections. Multiple nodes (each using a dI<sup>2</sup>C-bus buffer) may be connected at any point along this transmission line, however, the stub length degrades the bus performance, and should therefore be minimized.

### 7.1 I<sup>2</sup>C-bus/SMBus side

The I<sup>2</sup>C-bus/SMBus side of the PCA9614 differential bus buffer is connected to other I<sup>2</sup>C-bus/SMBus devices and requires pull-up resistors on each of the SCL and SDA signals. The value of the resistor should be chosen based on the bus capacitance and desired data speed, being careful not to overload the driver current rating of 3 mA for Standard and Fast modes, 30 mA for Fast-mode Plus (Fm+). The I<sup>2</sup>C-bus/SMBus side of the PCA9614 is powered from the V<sub>DD(A)</sub> supply pin.

### 7.2 dI<sup>2</sup>C-bus side differential pair

In previous I<sup>2</sup>C-bus/SMBus designs, the nodes (Controller and one or more Targets) are connected by wired-OR in combination with a single pull-up resistor. This simple arrangement is not suited for long distances more than one meter (1 m) or about three feet (3 ft), due to ringing and reflections on the unterminated bus. The use of a transmission line with correct termination eliminates this problem, and is further improved by differential signaling used in the dI<sup>2</sup>C-bus scheme. Each node acts as both a driver and a receiver to allow bidirectional signal flow, but not at the same time. Switching from transmit to receive is done automatically.

The dI<sup>2</sup>C-bus side of the PCA9614 is powered from the V<sub>DD(B)</sub> supply pin. The dI<sup>2</sup>C-bus is also biased to an idle state (D+ more positive than D-) to be compatible with the I<sup>2</sup>C-bus/SMBus wired-OR scheme, when not transmitting traffic (data). This allows every node to receive broadcast messages from the Controller, and return ACK/NACK and data in response. Biasing is done with additional resistors, connected to V<sub>DD(B)</sub> and V<sub>SS</sub> (the local ground), as shown in [Figure 5](#). The transmission line is terminated in the characteristic impedance of the cable, typically 100 Ω. This is the value defined by three resistors, the other two resistors providing the idle condition bias to the twisted pair.

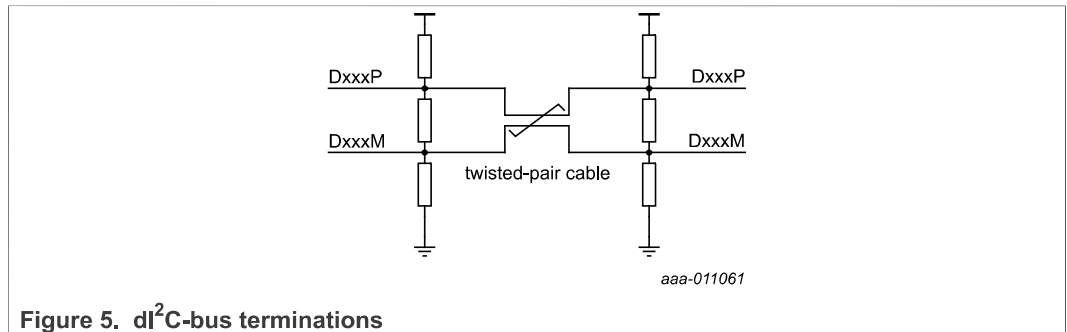


Figure 5. dl<sup>2</sup>C-bus terminations

### 7.2.1 Noise rejection

Impulse noise coupled into the I<sup>2</sup>C-bus/SMBus signals can prevent the I<sup>2</sup>C-bus/SMBus bus from operating reliably. The hostile signals may appear on the SCL line, SDA line, or both. Impulse noise may also enter the common ground connection, or be caused by current in the ground path caused by DC power supplies, or other signals sharing the common ground return path. This problem is removed by using a differential transmission line, in place of the I<sup>2</sup>C-bus/SMBus signal path. The dl<sup>2</sup>C-bus receiver (at each dl<sup>2</sup>C-bus node) subtracts the signals on the two differential lines (D+ and D-), and eliminates any common-mode noise that is coupled into the dl<sup>2</sup>C-bus. The receiver amplifies the signals which are also attenuated by the bulk resistance of the transmission line cable connection, and does not rely on a common ground connection at each node.

### 7.2.2 Rejection of ground offset voltage

Hostile signals interfere with the I<sup>2</sup>C-bus/SMBus bus through the common ground connection between each node. Current in this ground path causes an offset that may cause false data or push the I<sup>2</sup>C-bus/SMBus signals outside of an acceptable range. Unwanted ground offset can be caused by heavy DC current in the ground path, or injection of ground current from AC signals, either of which may show up as false signals.

Because the dl<sup>2</sup>C-bus node's receiver responds only to the difference between the two dl<sup>2</sup>C-bus transmission lines, common-mode signals are ignored. There is no need to have a ground connection between each of the nodes, which may be powered locally. Nodes may also be powered by extra conductors (for V<sub>DD</sub> and ground) run with the dl<sup>2</sup>C-bus signals. Voltage offsets caused by DC current in these additional wires are ignored by the dl<sup>2</sup>C-bus receiver, which subtracts the two differential signals (D+ and D-).

## 7.3 EN pin

The EN pin places the PCA9614 in an idle state, effectively stopping transmission of I<sup>2</sup>C-bus/SMBus traffic (data) over the dl<sup>2</sup>C-bus. An internal pull-up holds the device enabled. The enable pin is used to isolate a badly behaved target on power-up until after the system power-up reset. It should never change state during an I<sup>2</sup>C-bus/SMBus operation because disabling during a bus operation hangs the bus and enabling part way through a bus cycle could confuse the I<sup>2</sup>C-bus/SMBus parts being enabled. The EN pin should only change state when the global bus and the buffer port are in an idle state to prevent system failures. The EN pin turns on or off both channels.

## 8 Application design-in information

### 8.1 I<sup>2</sup>C-bus

As with the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels on the single-ended buffered bus (standard open-drain configuration of the I<sup>2</sup>C-bus). The size of these pull-up resistors depends on the system. The device is designed to work with Standard-mode, Fast-mode and Fast-mode Plus I<sup>2</sup>C-bus devices in addition to SMBus devices. Standard-mode and Fast-mode I<sup>2</sup>C-bus and SMBus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I<sup>2</sup>C-bus system where Standard-mode devices and multiple controllers are possible. When only Fast-mode Plus devices are used, then higher termination currents can be used due to their 30 mA sink capability.

### 8.2 Differential I<sup>2</sup>C-bus application

See [Figure 6](#) through [Figure 8](#).

The simple application ([Figure 6](#)) shows an existing SMBus/I<sup>2</sup>C-bus being extended over a section of dI<sup>2</sup>C-bus transmission line, containing a dedicated twisted pair for SCL and SDA. At one end of the transmission line, a resistor network (R1-R2-R1) terminates the twisted-pair cable and biases D+ positive with respect to D-. An identical resistor network at the other end of the transmission line terminates the twisted-pair cable. DC power for each end of the transmission line and the V<sub>DD(B)</sub> of each PCA9614 bus buffer can be from separate and isolated power supplies, or use the same supply and ground run in separate wires along the same path as the dI<sup>2</sup>C-bus signal twisted pairs.

Telecom category 5 ('CAT 5') data cable is well suited for this task, but loose wires may also be used, with a reduction in performance. Assuming V<sub>DD(B)</sub> is 5 V, and using CAT 5 cable, R2 is 120 Ω, R1 is 600 Ω. The parallel combination yields a termination of 100 Ω at each end of the twisted pairs. Either side of the dI<sup>2</sup>C-bus buffer pair is connected to standard SMBus/I<sup>2</sup>C buses, which require their own pull-up resistors to V<sub>DD(A)</sub> of the PCA9614 bus buffers. V<sub>DD(A)</sub> and V<sub>DD(B)</sub> can be the same supply, however, making them different voltages enables the PCA9614 bus buffers to level translate between the SMBus/I<sup>2</sup>C-bus and dI<sup>2</sup>C-bus sections of the bus, or to have different supply voltages and level translate at either end of the dI<sup>2</sup>C-bus and SMBus/I<sup>2</sup>C-bus system.

For example, the left-hand bus controller (and local target) may operate on a 3.3 V supply and SMBus/I<sup>2</sup>C-bus while the dI<sup>2</sup>C-bus transmission lines are at 5 V, and the right-hand target is operated from a different 3.3 V supply and SMBus/I<sup>2</sup>C-bus, or even a different bus voltage other than 3.3 V.

Depending upon the timing from the system controller, clock toggle rates can vary from 10 kHz for the SMBus (or less for SMBus/I<sup>2</sup>C-bus protocol) up to 100 kHz (Standard mode), 400 kHz (Fast mode), or up to 1 MHz (Fast-mode Plus).

The bus path is bidirectional. Assume that the left side SMBus/I<sup>2</sup>C-bus becomes active. A START condition (SDA goes LOW while SDA is HIGH) is sent. This upsets the idle condition on the dI<sup>2</sup>C-bus section of the bus, because D+ was more positive than D- and now they are reversed. The right side bus buffer sees the differential lines change polarity and in turn pulls SDA LOW on the SMBus/I<sup>2</sup>C-bus side of the bus buffer, transmitting the START condition to the target on that section of the SMBus/I<sup>2</sup>C-bus.

If the data clocked out by the left side controller contains a valid address of the right side target, that target responds by pulling SDA LOW on the ninth clock. This condition is transmitted across the dI<sup>2</sup>C-bus section that has now changed flow direction, and



received by the left side bus buffer (again, D+ was more positive than D- and now they are reversed).

This sequence continues until the controller sends the STOP condition (SCL HIGH while SDA goes HIGH), placing the active target (on the right side) back to idle. When idle, the normal SMBus/I<sup>2</sup>C-bus (both left and right sections) are pulled up by their respective pull-ups. In turn, the dI<sup>2</sup>C-bus section of the bus rests with D+ more positive than D-.

The idle condition can be changed by any node on either SMBus/I<sup>2</sup>C-bus section or an additional dI<sup>2</sup>C-bus node, if present, on the dI<sup>2</sup>C-bus section of the system. This allows the existing SMBus/I<sup>2</sup>C-bus protocol to operate transparently over a mix of SMBus/I<sup>2</sup>C and dI<sup>2</sup>C bus segments.

Due to the SMBus/I<sup>2</sup>C-bus handshake protocol (ACK/NACK on the ninth clock pulse), the direction of the SMBus/I<sup>2</sup>C-bus is reversed often. The 'time of flight' for the signals to pass through each bus buffer and for the target to respond defines the maximum speed of the bus, regardless of how fast the clock toggles. The dI<sup>2</sup>C-bus section of the bus requires two additional PCA9614 bus buffers, further delaying the SMBus/I<sup>2</sup>C-bus traffic. If the dI<sup>2</sup>C-bus transmission line section is made longer, the bus operates much slower, regardless of the clock toggle speed.

It is not necessary to have a ground connection between each end of the dI<sup>2</sup>C section of the bus. The dI<sup>2</sup>C-bus receiver responds to reversal of the polarity of the D+ and D- signals, and ignores the common-mode voltage that may be present.

Ideally, the common-mode voltage is the same at each end of the twisted pairs, and no current flows along the twisted pair when the bus is idle, because the D+ and D- dI<sup>2</sup>C-bus drivers are both high-impedance, the bus is biased by R1-R2-R1 at each end. If the common-mode voltage is not 0 V, current flows along the twisted pair, returning through the common ground, or common power supply connection if present.

If both ends of the twisted pair are powered by the same V<sub>DD(B)</sub> supply and one end is remote, there is a common-mode offset between them. This is ignored by the dI<sup>2</sup>C-bus receivers, which only respond to the difference between D+ and D-.

However, a large common-mode offset voltage forces the D+ and D- signals out of the range of the receiver, and data are lost. The PCA9614 bus buffers use standard ESD protection networks to protect the external pins, and therefore should not be biased above or below the V<sub>DD(B)</sub> and V<sub>SS</sub> pins respectively. This limits the common-mode range to approximately  $0.5 \times V_{DD(B)}$ .

DC resistance of the transmission line attenuates the signals, more so over longer distances. The loss of signal amplitude is made up by the gain of the dI<sup>2</sup>C-bus receiver. There is a limit to how long the dI<sup>2</sup>C-bus section can be made, as it is necessary for the driver to overcome the bias on the transmission line, in order to signal a polarity change (D+ and D- reversal) at the receiver end.

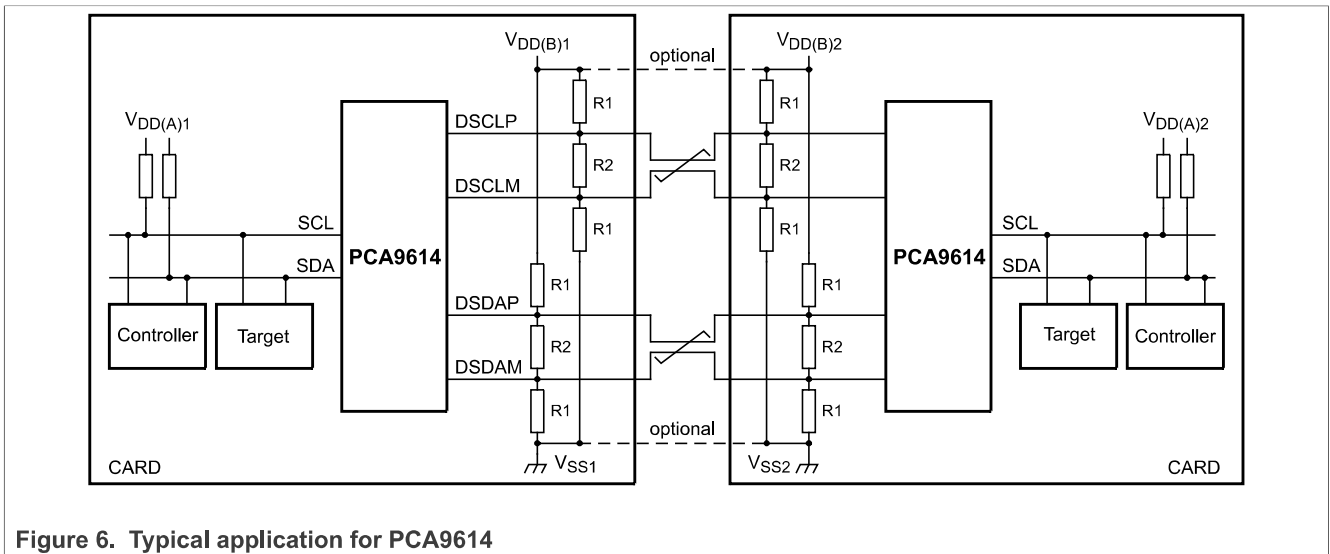
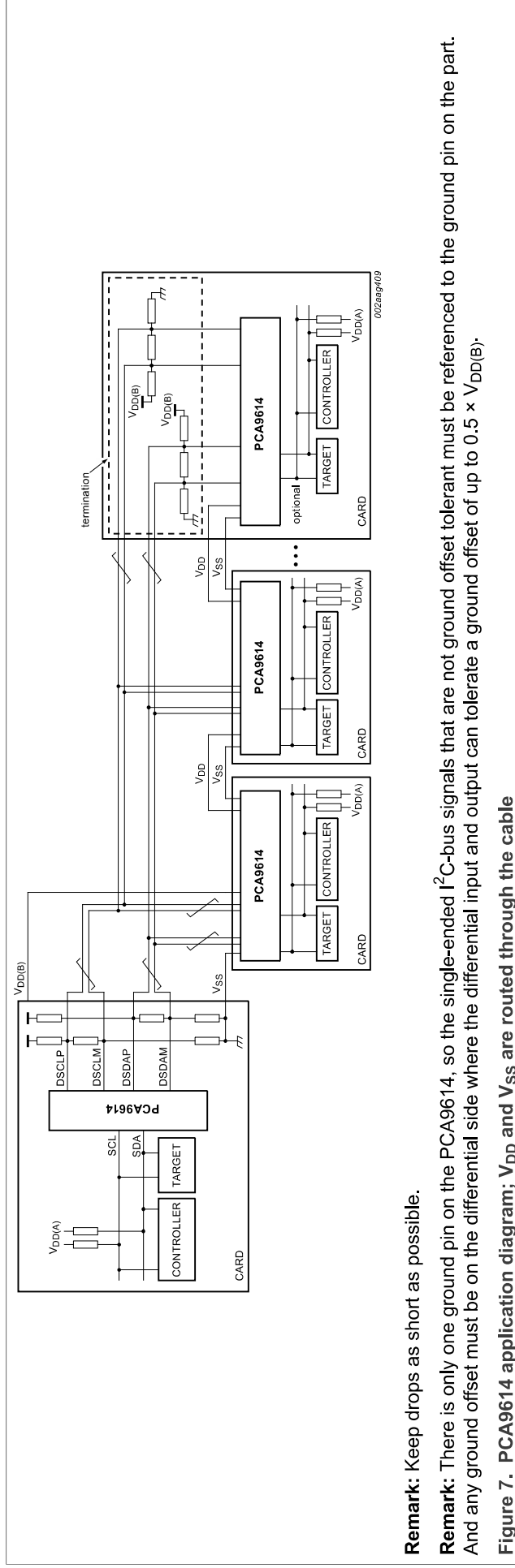


Figure 6. Typical application for PCA9614

2-channel multipoint Fast-mode Plus differential I<sup>2</sup>C-bus buffer

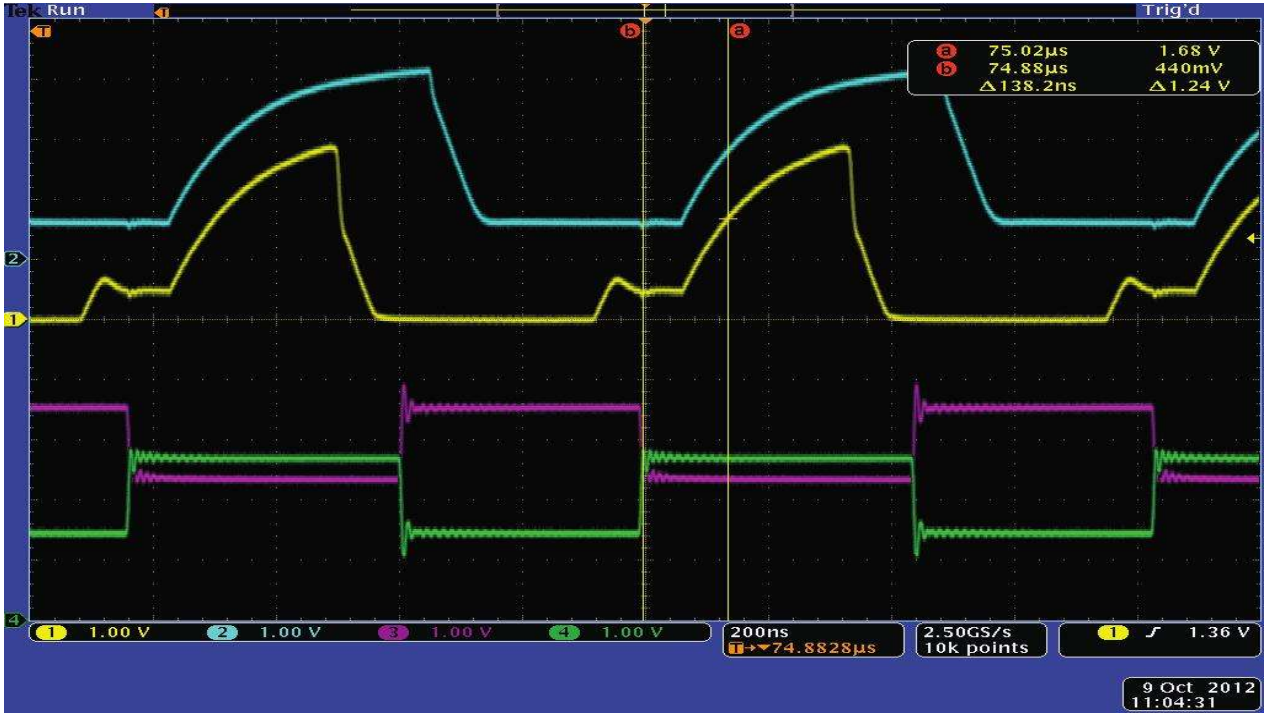


**Remark:** Keep drops as short as possible.

**Remark:** There is only one ground pin on the PCA9614, so the single-ended I<sup>2</sup>C-bus signals that are not ground offset tolerant must be referenced to the ground pin on the part. And any ground offset must be on the differential side where the differential input and output can tolerate a ground offset of up to 0.5 × V<sub>DD(B)</sub>.

Figure 7. PCA9614 application diagram; V<sub>DD</sub> and V<sub>SS</sub> are routed through the cable





aaa-011062

Figure 9. Differential bus waveform

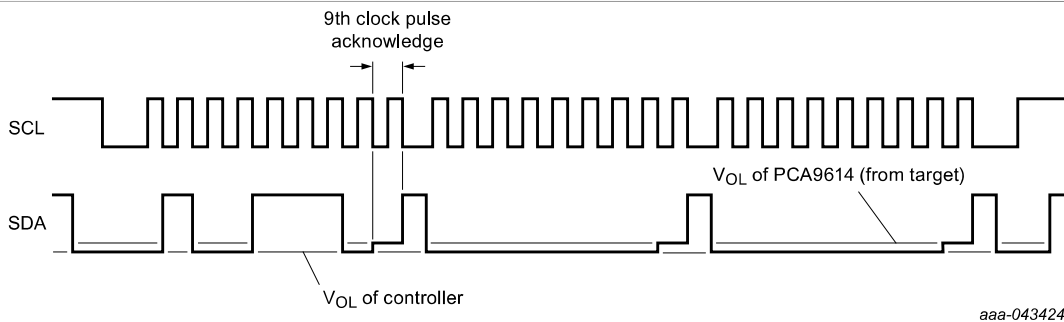


Figure 10. Single-ended bus waveform (controller side of bus)

## 9 Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD(B)</sub>	supply voltage port B	differential bus; 3.0 V to 5.5 V	-0.5	+6	V
V <sub>DD(A)</sub>	supply voltage port A	single-ended bus	-0.5	+6	V
V <sub>O(dif)</sub>	differential output voltage		-0.5	+6	V
V <sub>bus</sub>	bus voltage	voltage on I <sup>2</sup> C-bus B side, or enable (EN)	-0.5	+6	V
I <sub>I/O</sub>	input/output current	SDA, SCL, Dxxxx	-	80	mA
I <sub>DD(B)</sub>	supply current port B		-	160	mA
P <sub>tot</sub>	total power dissipation		-	100	mW
T <sub>stg</sub>	storage temperature		-55	+125	°C
T <sub>amb</sub>	ambient temperature	operating in free air	-40	+85	°C
T <sub>j</sub>	junction temperature		-	125	°C

## 10 Static characteristics

**Table 5. Static characteristics**

$V_{DD(B)} = 3.0\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
$V_{DD(B)}$	supply voltage port B	differential bus	3.0	-	5.5	V
$V_{DD(A)}$	supply voltage port A	single-ended bus <sup>[1]</sup>	2.3	-	5.5	V
$I_{DD(VDDA)}$	supply current on pin $V_{DD(A)}$		-	-	16	$\mu\text{A}$
$I_{DDH(B)}$	port B HIGH-level supply current	both channels HIGH; $V_{DD(B)} = 5.5\text{ V}$ ; $SDAn = SCLn = V_{DD(A)} = 5.5\text{ V}$	-	0.7	1.4	mA
$I_{DDL(B)}$	port B LOW-level supply current	both channels LOW; $V_{DD(B)} = 5.5\text{ V}$ ; $SDA$ and $SCL = V_{SS}$ ; differential I/Os open	-	1	1.7	mA
		driving termination; 2 channels	-	70	91	mA
<b>Input and output SDA and SCL</b>						
$V_{IH}$	HIGH-level input voltage		$0.7 \times V_{DD(A)}$	-	5.5	V
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.4	V
$V_{IK}$	input clamping voltage	$I_I = -18\text{ mA}$	-1.5	-	0	V
$I_{LI}$	input leakage current	$V_I = V_{DD(A)}$	-	-	$\pm 2$	$\mu\text{A}$
$I_{IL}$	LOW-level input current	$SDA, SCL$ ; $V_I = 0.2\text{ V}$	-	-	12	$\mu\text{A}$
$V_{OL}$	LOW-level output voltage	$I_{OL} = 200\ \mu\text{A}$ or $30\text{ mA}$	0.47	0.52	0.6	V
$V_{OL}-V_{IL}$	difference between LOW-level output and LOW-level input voltage	guaranteed by design	-	-	90	mV
$I_{LOH}$	HIGH-level output leakage current	$V_O = V_{DD(A)}$	-	-	$\pm 2$	$\mu\text{A}$
$C_{io}$	input/output capacitance	$V_I = V_{DD(A)}$ or $0\text{ V}$ ; disabled or $V_{DD(A)} = 0\text{ V}$	-	7	10	pF
<b>Input and output DSDAP/DSDAM and DSCLP/DSCLM</b>						
$V_{cm}$	common-mode voltage		0	-	$V_{DD(B)}$	V
$I_{LI}$	input leakage current	$V_I = V_{DD(B)}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{IL}$	LOW-level input current	$V_I = 0.2\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$V_{th(dif)}$	differential receiver threshold voltage	$0\text{ V} \leq V_{cm} \leq V_{DD(B)}$	-200	-	+200	mV
$V_{I(hys)}$	hysteresis of input voltage	receiver; $0\text{ V} \leq V_{cm} \leq V_{DD(B)}$	-	30	-	mV
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	single-ended input LOW				
		no load	$-V_{DD(B)}$	-	-	V
		$R_L = 54\ \Omega$ at $V_{DD(B)} = 5\text{ V}$	-5.0	-1.5	-1.0	V
$C_{io}$	input/output capacitance	$V_I = V_{DD(B)}$ or $0\text{ V}$ ; disabled or $V_{DD(B)} = 0\text{ V}$	-	7	10	pF

2-channel multipoint Fast-mode Plus differential I<sup>2</sup>C-bus buffer

**Table 5. Static characteristics...continued**

$V_{DD(B)} = 3.0\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input EN</b>						
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD(A)}$	-	5.5	V
$V_{IL}$	LOW-level input voltage		-0.5	-	$+0.3V_{DD(A)}$	V
$I_{LI}$	input leakage current	$V_I = V_{DD(B)}$	-1	-	+1	$\mu\text{A}$
$I_{IL(EN)}$	LOW-level input current on pin EN	$V_I = 0.2\text{ V}$ , EN; $V_{DD(A)} = 5.5\text{ V}$	-	-20	-54	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{DD(A)}$	-	6	10	pF
$R_{PU}$	pull-up resistance	internal pull-up resistor connected to $V_{DD(A)}$ rail	-	300	-	k $\Omega$

[1] LOW-level supply voltage.

## 11 Dynamic characteristics

**Table 6. Dynamic characteristics**

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.<sup>[1][2]</sup>

Symbol	Parameter	Conditions	Min	Typ <sup>[3]</sup>	Max	Unit
$t_{PLH}$	LOW to HIGH propagation delay	single-ended side to differential side; <a href="#">Figure 13</a>	<sup>[4]</sup> -140	-120	-	ns
$t_{PLH2}$	LOW to HIGH propagation delay 2	single-ended side to differential side; <a href="#">Figure 13</a>	-	-	100	ns
$t_{PHL}$	HIGH to LOW propagation delay	single-ended side to differential side; <a href="#">Figure 11</a>	<sup>[5]</sup> -	-	120	ns
$SR_r$	rising slew rate	differential side; <a href="#">Figure 11</a>	-	-	1	V/ns
$SR_f$	falling slew rate	differential side; <a href="#">Figure 11</a>	<sup>[5]</sup> -	-	1	V/ns
$t_{PLH}$	LOW to HIGH propagation delay	differential side to single-ended side; <a href="#">Figure 12</a>	<sup>[6]</sup> -	-	150	ns
$t_{PHL}$	HIGH to LOW propagation delay	differential side to single-ended side; <a href="#">Figure 12</a>	<sup>[6]</sup> -	-	150	ns
$SR_f$	falling slew rate	single-ended side; <a href="#">Figure 12</a>	-	-	0.1	V/ns
$t_{en}$	enable time	EN HIGH to enable	<sup>[7]</sup> -	-	200	ns
$t_{dis}$	disable time	EN LOW to disable	<sup>[7]</sup> -	-	200	ns

[1] Times are specified with loads of 1.35 k $\Omega$  pull-up resistance and 50 pF load capacitance on the A side, and 50  $\Omega$  termination network resistance and 50 pF load capacitance on the B side. Different load resistance and capacitance alters the RC time constant, thereby changing the propagation delay and transition times.

[2] Pull-up voltages are  $V_{DD(A)}$  on the A side and termination network on the B side.

[3] Typical values were measured with  $V_{DD(A)} = 3.3\text{ V}$  at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted.

[4] The  $t_{PLH}$  delay data from B side to A side is measured at 0 V differential on the B side to  $0.5V_{DD(A)}$  on the A side.

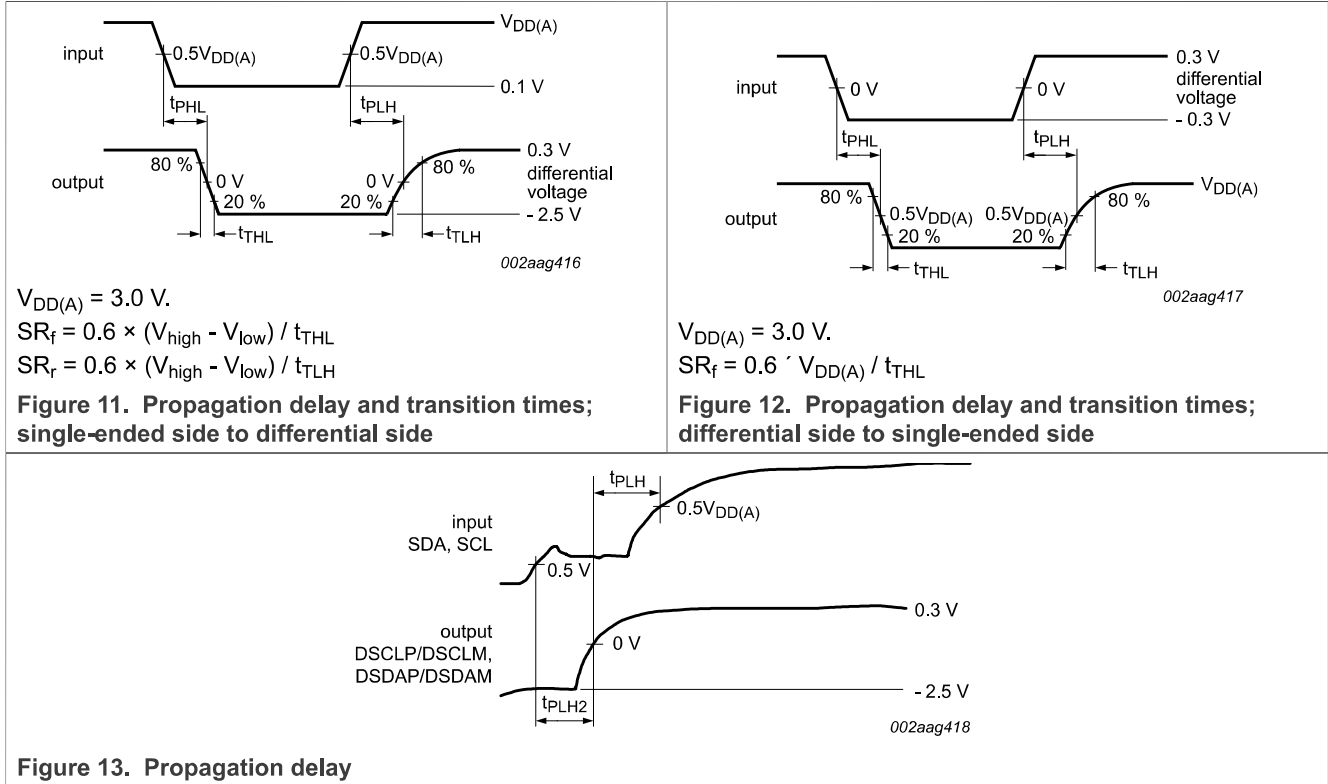
[5] Typical value measured with  $V_{DD(A)} = 3.3\text{ V}$  at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[6] The proportional delay data from A side to B side is measured at  $0.5V_{DD(A)}$  on the A side to 0 V on the B side.

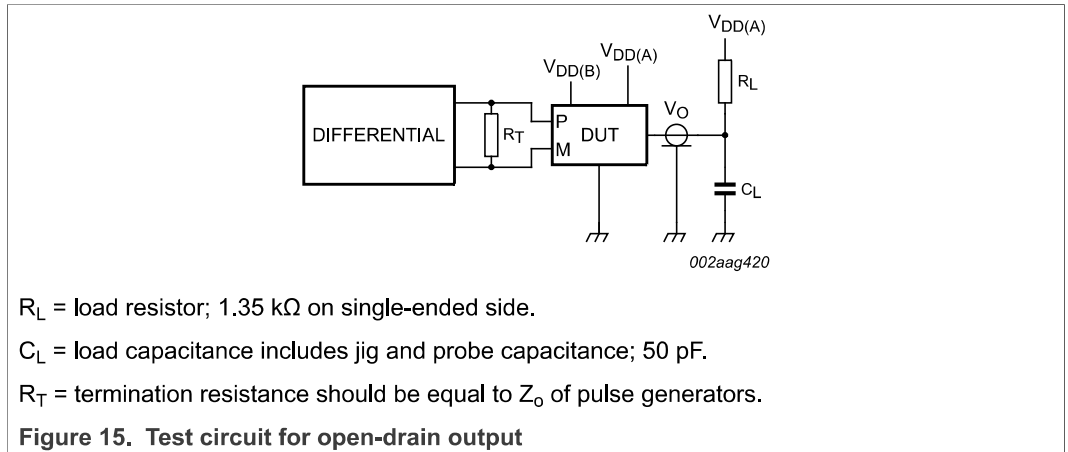
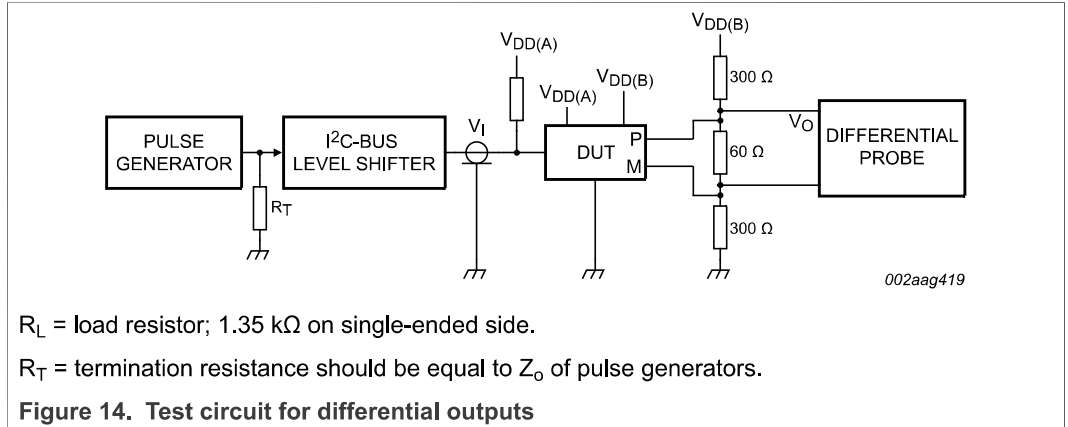
[7] The enable pin (EN) should only change state when the global bus and the repeater port are in an idle state.



11.1 AC waveforms



12 Test information



13 Package outline

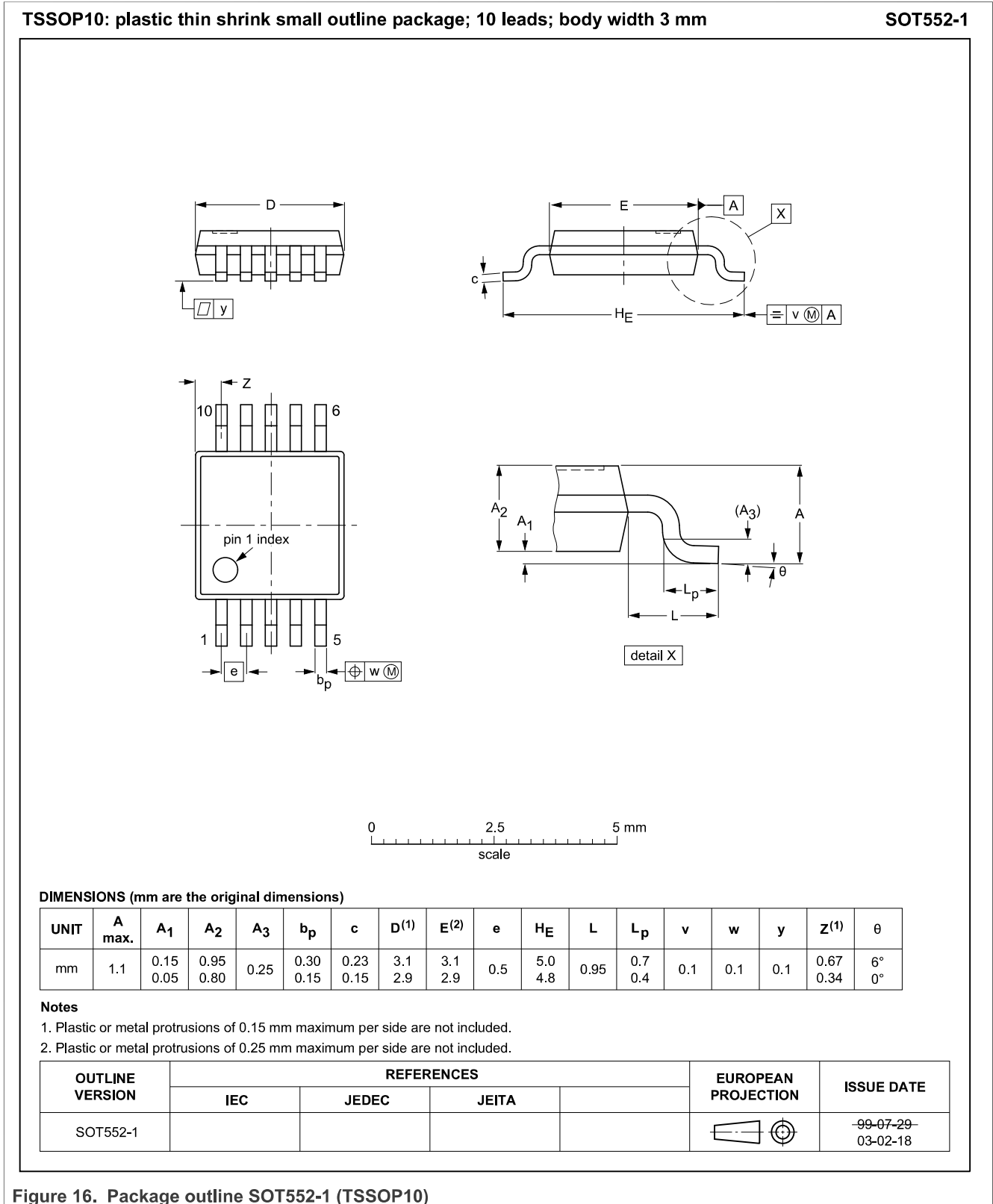


Figure 16. Package outline SOT552-1 (TSSOP10)

## 14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks, and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 17](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 7](#) and [Table 8](#)

**Table 7. SnPb eutectic process (from J-STD-020D)**

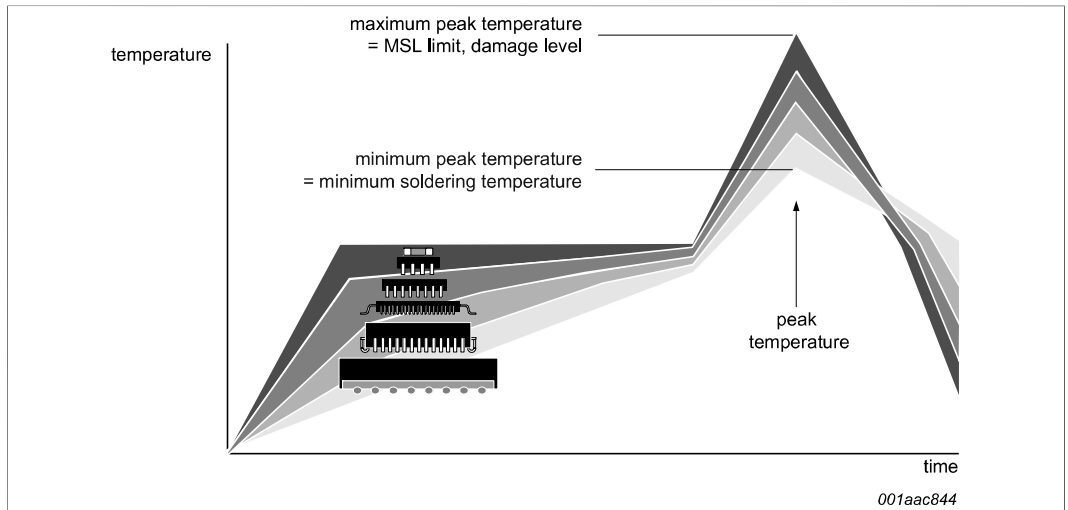
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 8. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 17](#).



MSL: Moisture Sensitivity Level

Figure 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

15 Soldering: PCB footprints

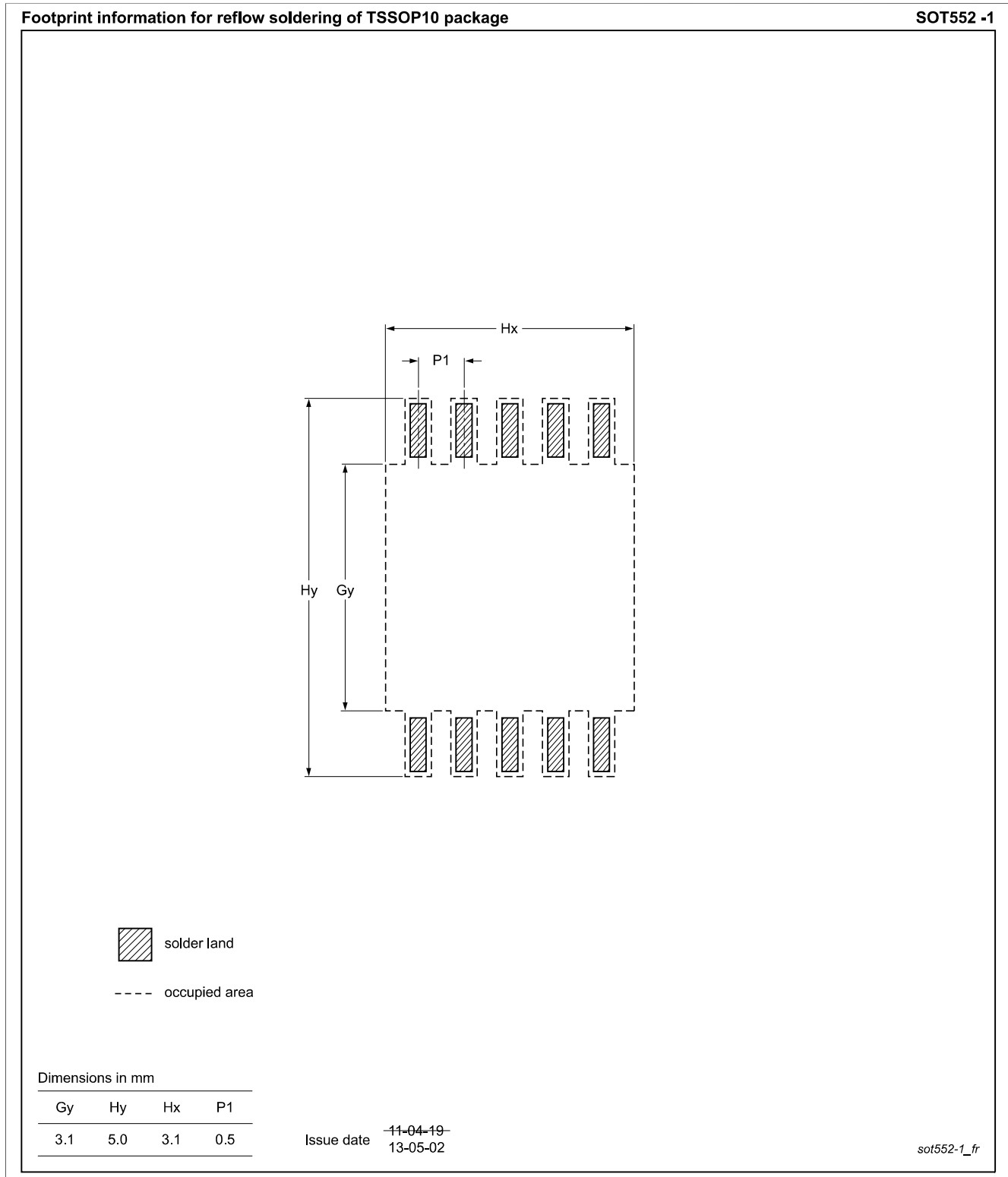


Figure 18. PCB footprint for SOT552-1 (TSSOP10); reflow soldering

## 16 Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged-Device Model
dI <sup>2</sup> C-bus	differential Inter-Integrated Circuit bus
ESD	ElectroStatic Discharge
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
SMBus	System Management Bus

## 17 Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9614 v.2	20210921	Product data sheet	PCN 202104008A	PCA9614 v.1
Modifications	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors, N.V. Legal texts have been adapted to the new company name where appropriate.</li> <li>Global changes, revised as follows:               <ul style="list-style-type: none"> <li>"Master" or "master": revised to "Controller" or "controller" to conform with NXP inclusive language guidelines.</li> <li>"Slave" or "slave": revised to "Target" or "target" to conform with NXP inclusive language guidelines.</li> </ul> </li> <li><a href="#">Section 4.1</a>. revised <a href="#">Table 2</a>. added footnote on the heading "Packing method", a second footnote on "PCA9614DP, 118", revised the description, and inserted new part number PCA9614DPZ.</li> </ul>			
PCA9614 v.1	20140411	Product data sheet	—	—



## 18 Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 18.2 Definitions

**Draft** — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 18.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

---

**2-channel multipoint Fast-mode Plus differential I<sup>2</sup>C-bus buffer**

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

**Security** — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

## 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP B.V.

**NXP** — wordmark and logo are trademarks of NXP B.V.

## Tables

Tab. 1.	Ordering information .....	3	Tab. 6.	Dynamic characteristics .....	16
Tab. 2.	Ordering options .....	3	Tab. 7.	SnPb eutectic process (from J-STD-020D) .....	21
Tab. 3.	Pin description .....	5	Tab. 8.	Lead-free process (from J-STD-020D) .....	21
Tab. 4.	Limiting values .....	14	Tab. 9.	Abbreviations .....	24
Tab. 5.	Static characteristics .....	15	Tab. 10.	Revision history .....	24

## Figures

Fig. 1.	SMBus/I2C-bus translation to dI2C-bus and back to SMBus/I2C-bus .....	2	Fig. 11.	Propagation delay and transition times; single-ended side to differential side .....	17
Fig. 2.	Functional diagram of PCA9614 .....	4	Fig. 12.	Propagation delay and transition times; differential side to single-ended side .....	17
Fig. 3.	Differential output driver simplified circuit .....	4	Fig. 13.	Propagation delay .....	17
Fig. 4.	Pin configuration for TSSOP10 .....	5	Fig. 14.	Test circuit for differential outputs .....	18
Fig. 5.	dI2C-bus terminations .....	7	Fig. 15.	Test circuit for open-drain output .....	18
Fig. 6.	Typical application for PCA9614 .....	10	Fig. 16.	Package outline SOT552-1 (TSSOP10) .....	19
Fig. 7.	PCA9614 application diagram; VDD and VSS are routed through the cable .....	11	Fig. 17.	Temperature profiles for large and small components .....	22
Fig. 8.	PCA9614 application diagram; VDD and VSS are not routed through the cable .....	12	Fig. 18.	PCB footprint for SOT552-1 (TSSOP10); reflow soldering .....	23
Fig. 9.	Differential bus waveform .....	13			
Fig. 10.	Single-ended bus waveform (controller side of bus) .....	13			

## Contents

---

<b>1</b>	<b>General description .....</b>	<b>1</b>
<b>2</b>	<b>Features and benefits .....</b>	<b>2</b>
<b>3</b>	<b>Applications .....</b>	<b>3</b>
<b>4</b>	<b>Ordering information .....</b>	<b>3</b>
4.1	Ordering options .....	3
<b>5</b>	<b>Functional diagram .....</b>	<b>4</b>
<b>6</b>	<b>Pinning information .....</b>	<b>5</b>
6.1	Pinning .....	5
6.2	Pin description .....	5
<b>7</b>	<b>Functional description .....</b>	<b>6</b>
7.1	I <sup>2</sup> C-bus/SMBus side .....	6
7.2	dI <sup>2</sup> C-bus side differential pair .....	6
7.2.1	Noise rejection .....	7
7.2.2	Rejection of ground offset voltage .....	7
7.3	EN pin .....	7
<b>8</b>	<b>Application design-in information .....</b>	<b>8</b>
8.1	I <sup>2</sup> C-bus .....	8
8.2	Differential I <sup>2</sup> C-bus application .....	8
<b>9</b>	<b>Limiting values .....</b>	<b>14</b>
<b>10</b>	<b>Static characteristics .....</b>	<b>15</b>
<b>11</b>	<b>Dynamic characteristics .....</b>	<b>16</b>
11.1	AC waveforms .....	17
<b>12</b>	<b>Test information .....</b>	<b>18</b>
<b>13</b>	<b>Package outline .....</b>	<b>19</b>
<b>14</b>	<b>Soldering of SMD packages .....</b>	<b>20</b>
14.1	Introduction to soldering .....	20
14.2	Wave and reflow soldering .....	20
14.3	Wave soldering .....	20
14.4	Reflow soldering .....	21
<b>15</b>	<b>Soldering: PCB footprints .....</b>	<b>23</b>
<b>16</b>	<b>Abbreviations .....</b>	<b>24</b>
<b>17</b>	<b>Revision history .....</b>	<b>24</b>
<b>18</b>	<b>Legal information .....</b>	<b>25</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© NXP B.V. 2021.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 21 September 2021  
Document identifier: PCA9614