

### **General Description**

The WSD46N10DN56 is the highest performance SGT Dual N-Ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSD46N10DN56 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

#### **Features**

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

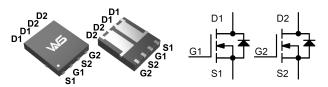
### **Product Summery**

BVDSS	RDSON	ID
100V	14mΩ	40A

## **Applications**

- DC-DC Converter.
- Motor Control.

### **DFN5X6C-8-EP2 Pin Configuration**



### **Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25℃	Continuous Drain Current, V <sub>GS</sub> @ 10V	40	Α
I <sub>D</sub> @T <sub>C</sub> =100℃	Continuous Drain Current, V <sub>GS</sub> @ 10V	33	Α
I <sub>DM</sub> a	Pulsed Drain Current	120	Α
E <sub>AS</sub> <sup>b</sup>	Single Pulse Avalanche Energy	57	mJ
I <sub>AS</sub> <sup>b</sup>	Avalanche Current	26	Α
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation	71	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	$^{\circ}$ C
$T_J$	Operating Junction Temperature Range	-55 to 150	$^{\circ}$ C

#### **Thermal Data**

Symbol	Parameter	Тур.	Max.	Unit	
R <sub>θJA</sub> <sup>c</sup>	Thermal Resistance Junction-ambient		25	°C/W	
$R_{ heta JC}$	Thermal Resistance Junction-Case		1.7	°C/W	

Note a: Pulse width limited by max. junction temperature.

Note b: UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature T<sub>i</sub>=25°C).

Note c: Surface Mounted on 1in<sup>2</sup> pad area.

**Dual N-Ch MOSFET** 

# Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	100			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25℃ , I <sub>D</sub> =1mA		0.098		V/°C
R <sub>DS(ON)</sub> d	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =10A		14	20	mΩ
R <sub>DS(ON)</sub> d	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =7A		18	30	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.5	2.5	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	VGS-VDS , ID -250UA		-5.52		mV/℃
	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =25℃			1		
I <sub>DSS</sub>	Drain-Source Leakage Current	$V_{DS}$ =80V , $V_{GS}$ =0V , $T_J$ =55 $^{\circ}\mathrm{C}$			30	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}$ = $\pm 20V$ , $V_{DS}$ = $0V$			±100	nA
R <sub>g</sub> e	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		1.2		Ω
Qg <sup>e</sup>	Total Gate Charge (10V)	V <sub>DS</sub> =50V , V <sub>GS</sub> =10V , I <sub>D</sub> =5A		17		
Q <sub>gs</sub> e	Gate-Source Charge			2.8		nC
$Q_{gd}^e$	Gate-Drain Charge			4.1		
T <sub>d(on)</sub> e	Turn-On Delay Time			16		
T <sub>r</sub> e	Rise Time	$V_{DD}$ =30V , $V_{GEN}$ =10V , $R_G$ =6 $\Omega$		3.8		
T <sub>d(off)</sub> e	Turn-Off Delay Time	I <sub>D</sub> =1A ,RL=30Ω		75		ns
T <sub>f</sub> e	Fall Time			46		
C <sub>iss</sub> e	Input Capacitance			1010		
C <sub>oss</sub> e	Output Capacitance	V <sub>DS</sub> =50V , V <sub>GS</sub> =0V , f=1MHz		185		pF
C <sub>rss</sub> <sup>e</sup>	Reverse Transfer Capacitance			12		

## **Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			30	Α
$V_{SD}^d$	Diode Forward Voltage	$V_{GS}$ =0V , $I_{S}$ =1A , $T_{J}$ =25 $^{\circ}$ C			1.2	V
t <sub>rr</sub>	Reverse Recovery Time	Is=1A,dl/dt=100A/µs		49		nS
Q <sub>rr</sub>	Reverse Recovery Charge	,		62		nC

Note d : Pulse test ; pulse width $\leq 300 \mu s$ , duty cycle $\leq 2\%$ .

Note e: Guaranteed by design, not subject to production testing.



## **Typical Characteristics**

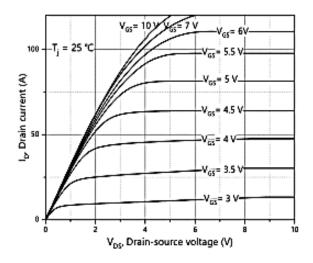


Figure 1, Typ. output characteristics

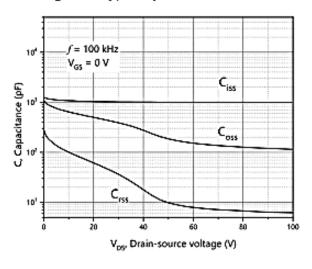


Figure 3, Typ. capacitances

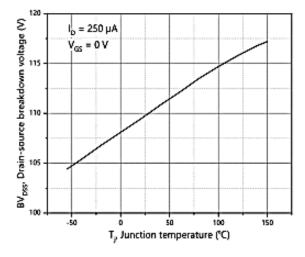


Figure 5, Drain-source breakdown voltage

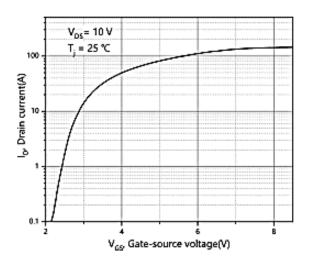


Figure 2, Typ. transfer characteristics

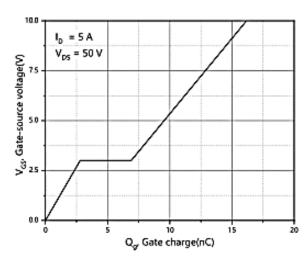


Figure 4, Typ. gate charge

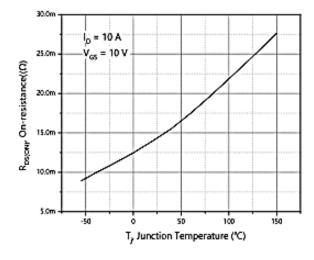


Figure 6, Drain-source on-state resistance



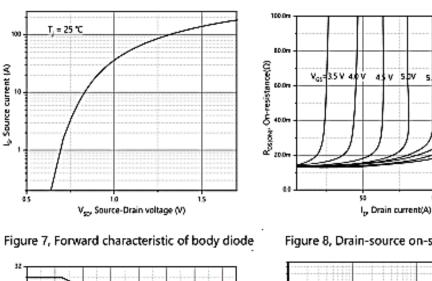


Figure 8, Drain-source on-state resistance

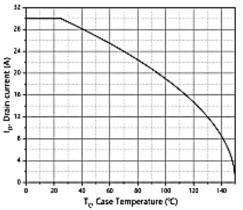


Figure 9, Drain current

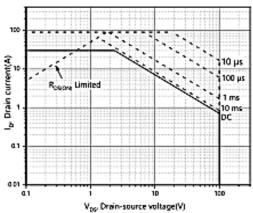
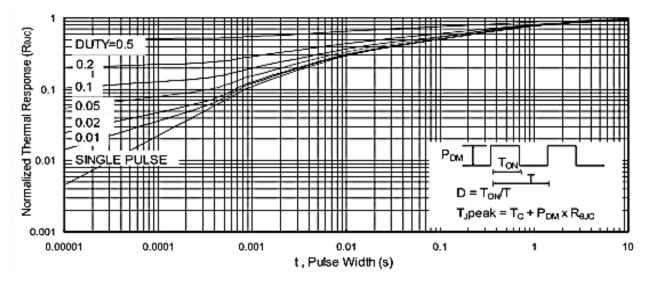


Figure 10, Safe operation area Tc=25 \*C



Figu11. Normalized Maximum Transient Thermal Impedance



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