

• General Description

The AGM402D combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

• Features

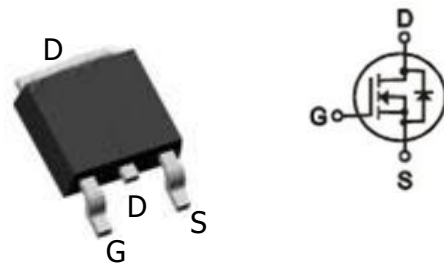
- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

• Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
40V	2.1mΩ	120A

TO-252 Pin Configuration

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM402D	AGM402D	TO-252	--mm	--mm	2500

Table 1. Absolute Maximum Ratings (T_A=25°C)

Symbol	Parameter	Value	Unit
V _{DS}	Drain-Source Voltage (V _{GS} =0V)	40	V
V _{GS}	Gate-Source Voltage (V _{DS} =0V)	±20	V
I _D	Drain Current-Continuous(T _c =25°C) ^(Note 1)	120	A
	Drain Current-Continuous(T _c =100°C)	68	A
I _{DM (pulse)}	Drain Current-Continuous@ Current-Pulsed (Note 2)	520	A
P _D	Maximum Power Dissipation(T _c =25°C)	125	W
	Maximum Power Dissipation(T _c =100°C)	62	W
E _{AS}	Avalanche energy ^(Note 3)	550	mJ
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
R _{θJA}	Thermal Resistance Junction-ambient (Steady State) ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	1.2	°C/W

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)
Typical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	45	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current (T _j =125°C)	V _{DS} =40V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.7	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ^③	V _{GS} =10V, I _D =40A	--	2.1	2.9	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ^③	V _{GS} =4.5V, I _D =20A	--	3.1	5	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz		3040		pF
C _{oss}	Output Capacitance			395		pF
C _{rss}	Reverse Transfer Capacitance			320		pF
R _g	Gate Resistance	f=1MHz		2		Ω
Q _g	Total Gate Charge	V _{DS} =20V, I _D =40A, V _{GS} =10V	--	73	--	nC
Q _{gs}	Gate-Source Charge		-	15	--	nC
Q _{gd}	Gate-Drain Charge		-	15	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	12.7	--	nS
t _r	Turn-on Rise Time		-	6.3	--	nS
t _{d(off)}	Turn-Off Delay Time		-	51	--	nS
t _f	Turn-Off Fall Time		-	12	--	nS
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A, V _{GS} =0V	--	0.8	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{SD} =30A, V _{GS} =0V di/dt=500A/μs	--	16	--	nS
Q _{rr}	Reverse Recovery Charge		41			nC

Notes 1. The maximum current rating is package limited.

Notes 2. Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3. EAS condition: T_j=25°C, V_{DD}=15V, V_G=10V, R_G=25Ω

Typical Characteristics

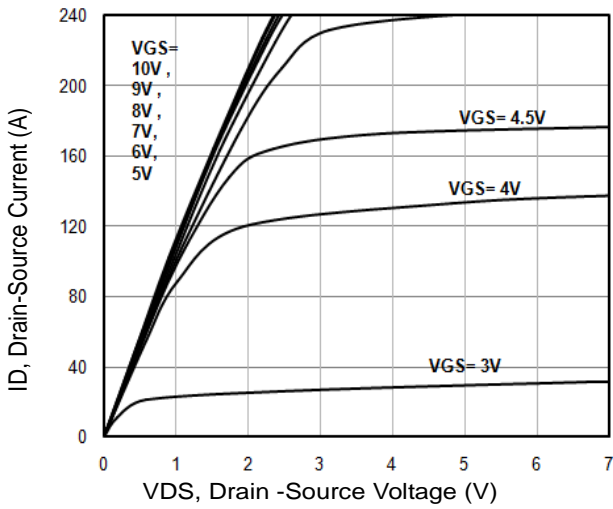


Fig1. Typical Output Characteristics

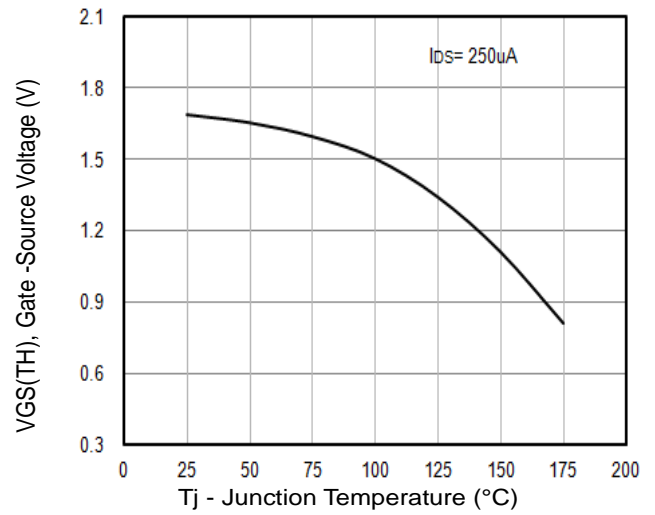


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

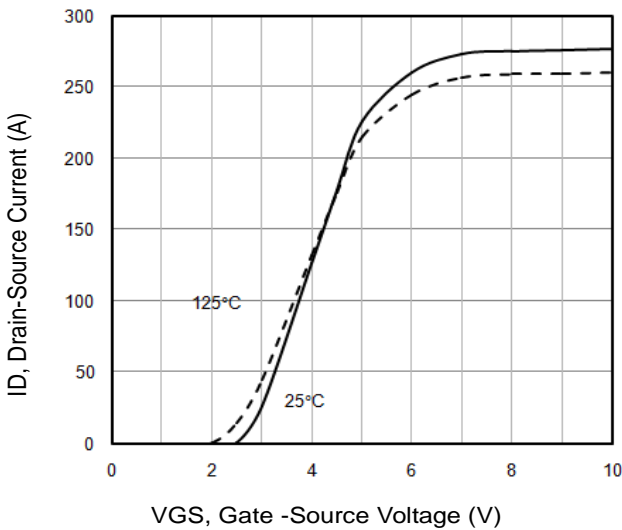


Fig3. Typical Transfer Characteristics

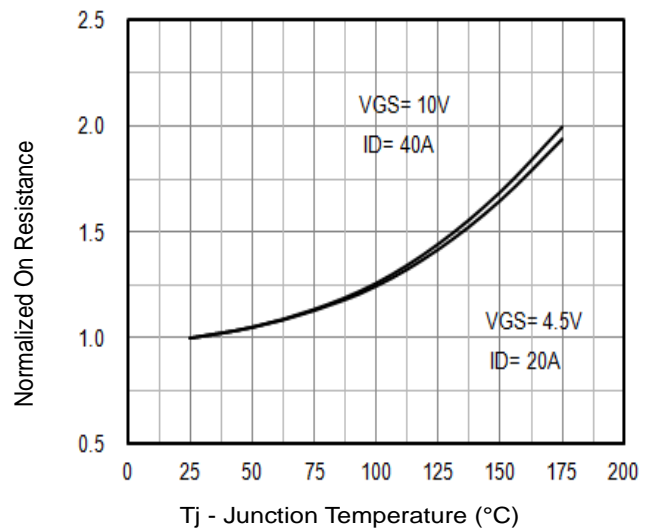


Fig4. Normalized On-Resistance Vs. Temperature

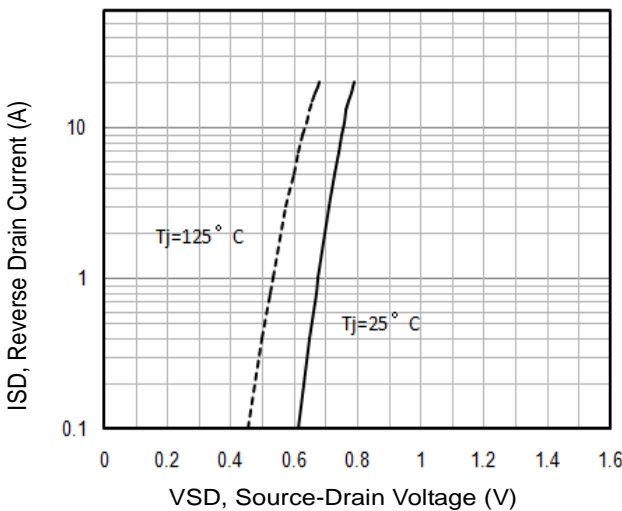


Fig5. Typical Source-Drain Diode Forward Voltage

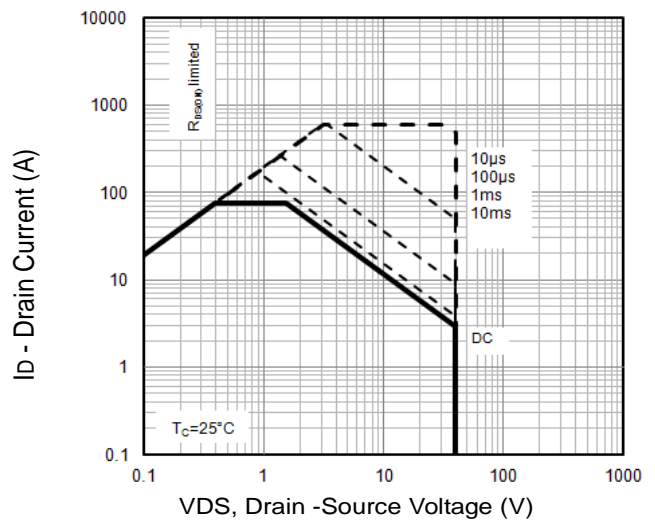


Fig6. Maximum Safe Operating Area

Typical Characteristics

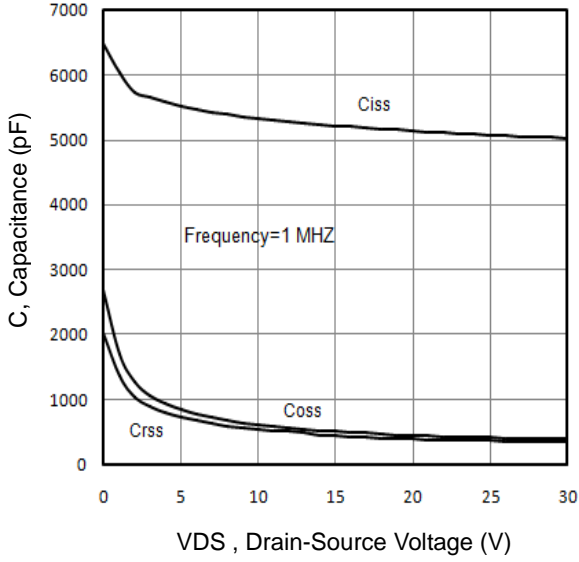


Fig7. Typical Capacitance Vs.Drain-Source Voltage

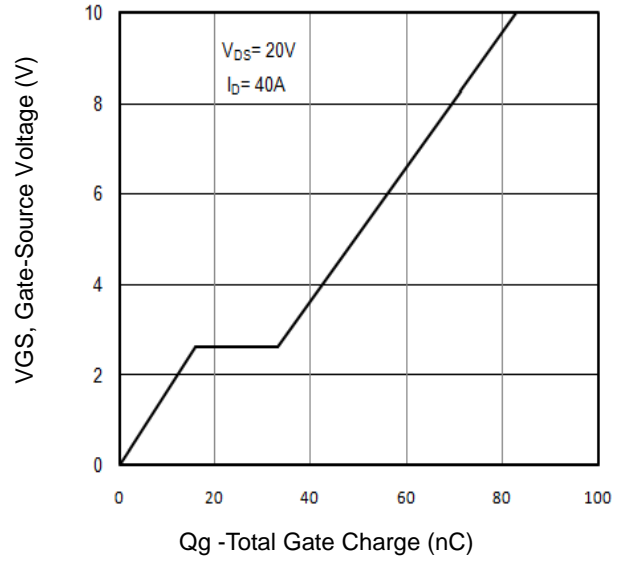


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

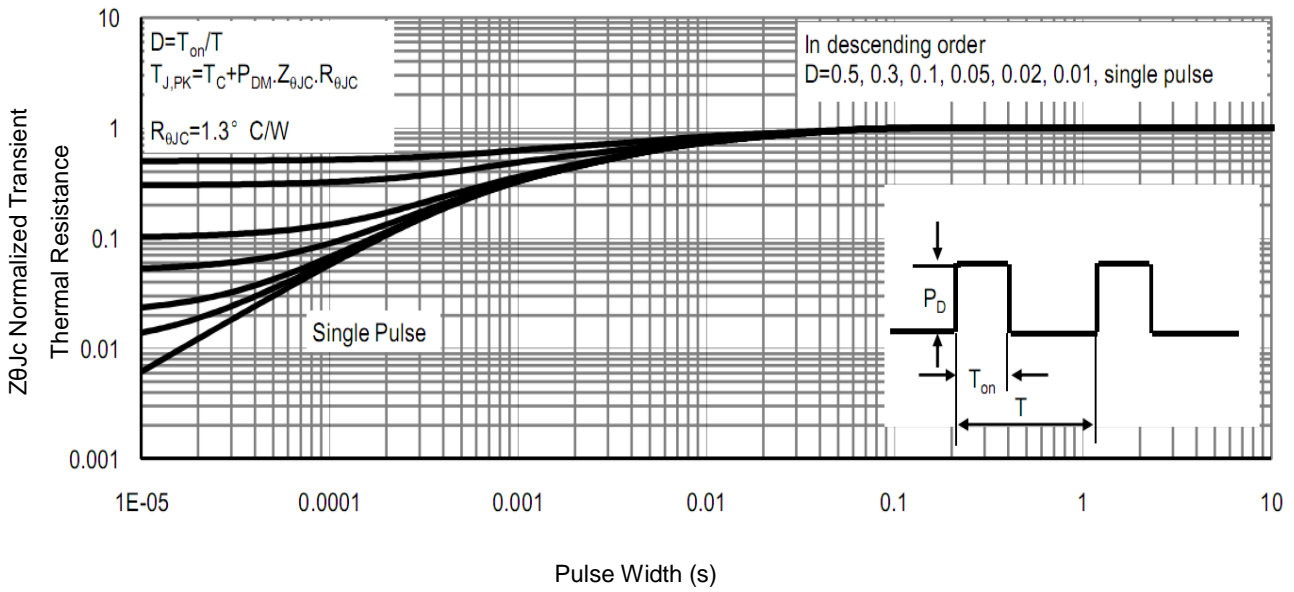


Fig9 . Normalized Maximum Transient Thermal Impedance

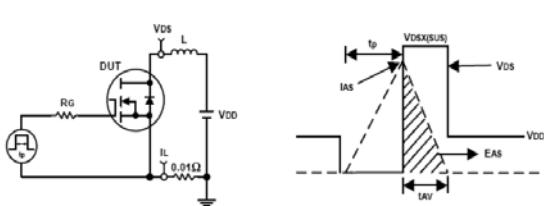


Fig10. Unclamped Inductive Test Circuit and waveforms

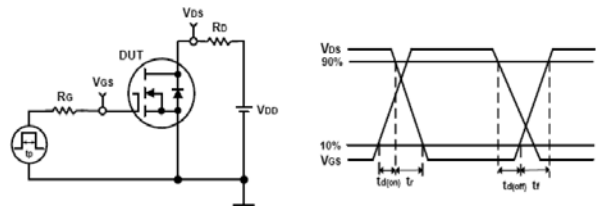
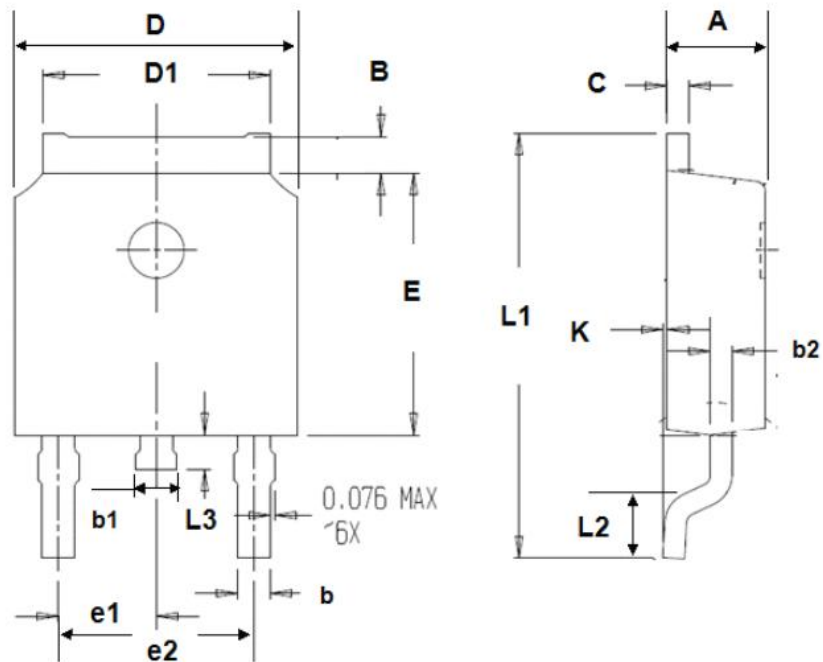


Fig11. Switching Time Test Circuit and waveforms

•Dimensions

SYMBOL	min	max	SYMBOL	min	max
A	2.10	2.50	B	0.85	1.25
b	0.50	0.80	b1	0.50	0.90
b2	0.45	0.70	C	0.45	0.70
D	6.30	6.75	D1	5.10	5.50
E	5.30	6.30	e1	2.25	2.35
L1	9.20	10.60	e2	4.45	4.75
L2	0.90	1.75	L3	0.60	1.10
K	0.00	0.23			




Disclaimer:

The information provided in this document is believed to be accurate and reliable. however, Shenzhen Core Control Electronics Technology Co., Ltd. does not assume any responsibility for the following consequences Do not consider the use of such information or use beyond its scope.

The information mentioned in this document may be changed at any time without notice.

The products and information provided in this document do not infringe patents. Shenzhen Core Control Electronics Technology Co., Ltd. assumes no responsibility for any infringement of any other rights of third parties. The result of using such products and information.

This document is the second version issued on October 10, 2019. This document replaces and Replace all previously provided information.

 It is a registered trademark of Shenzhen Core Control Electronics Technology Co., Ltd.

Copyright © 2017 Shenzhen Core Control Electronics Technology Co., Ltd. all rights reserved.